

```
Copy to Drive
                                           + Code + Text
                                 \square \times
    Table of contents
            DSLX
                                            [ ] %%bash -c "cat > test.py; make"
Q
                                                 import cocotb
         Convert to Hardware IR
                                                 from cocotb.triggers import ClockCycles, RisingEdge
{X}
                                                 from cocotb.clock import Clock
         Generate RTL
                                                 @cocotb.test()
Run the OpenLane flow
                                                 async def test test(dut):
                                                     c = Clock(dut.clk, 1, 'ns')
            Configuration
                                                     cocotb.start soon(c.start())
            Synthesis
                                                     # TODO(YOU): update with the 8-input to user_module
                                                     dut.user module tb.io in.value = NaN
               Preview
                                                     # pipeline stage 0: fetch
                                                     await ClockCycles(dut.clk, 2)
            Floorplan
                                                     # TODO(YOU): verify that the input value propagate to stage #0
                                                     assert dut.user module tb.p0 io in == NaN
               Preview
                                                     # pipeline stage 1: slice
            Placement
                                                     await ClockCycles(dut.clk, 2)
                                                     # TODO(YOU): update `p1 bit slice *` names to match the wire in the gene
               Preview
                                                     # TODO(YOU): verify that the input value is sliced into 4-bit umul opera
                                                     assert dut.user module tb.pl bit slice TODO == NaN
            Routing
                                                     assert dut.user module tb.pl bit slice TODO == NaN
               Preview
                                                     # pipeline stage 2: multiply
                                                     await ClockCycles(dut.clk, 2)
            Sign off
                                                     # TODO(YOU): verify that the output value match the multiplication resul
                                                     assert dut.user module tb.out == NaN
<>
               Preview
```