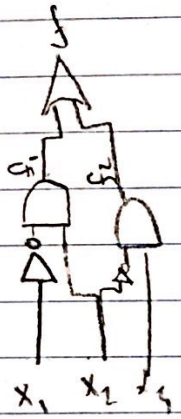
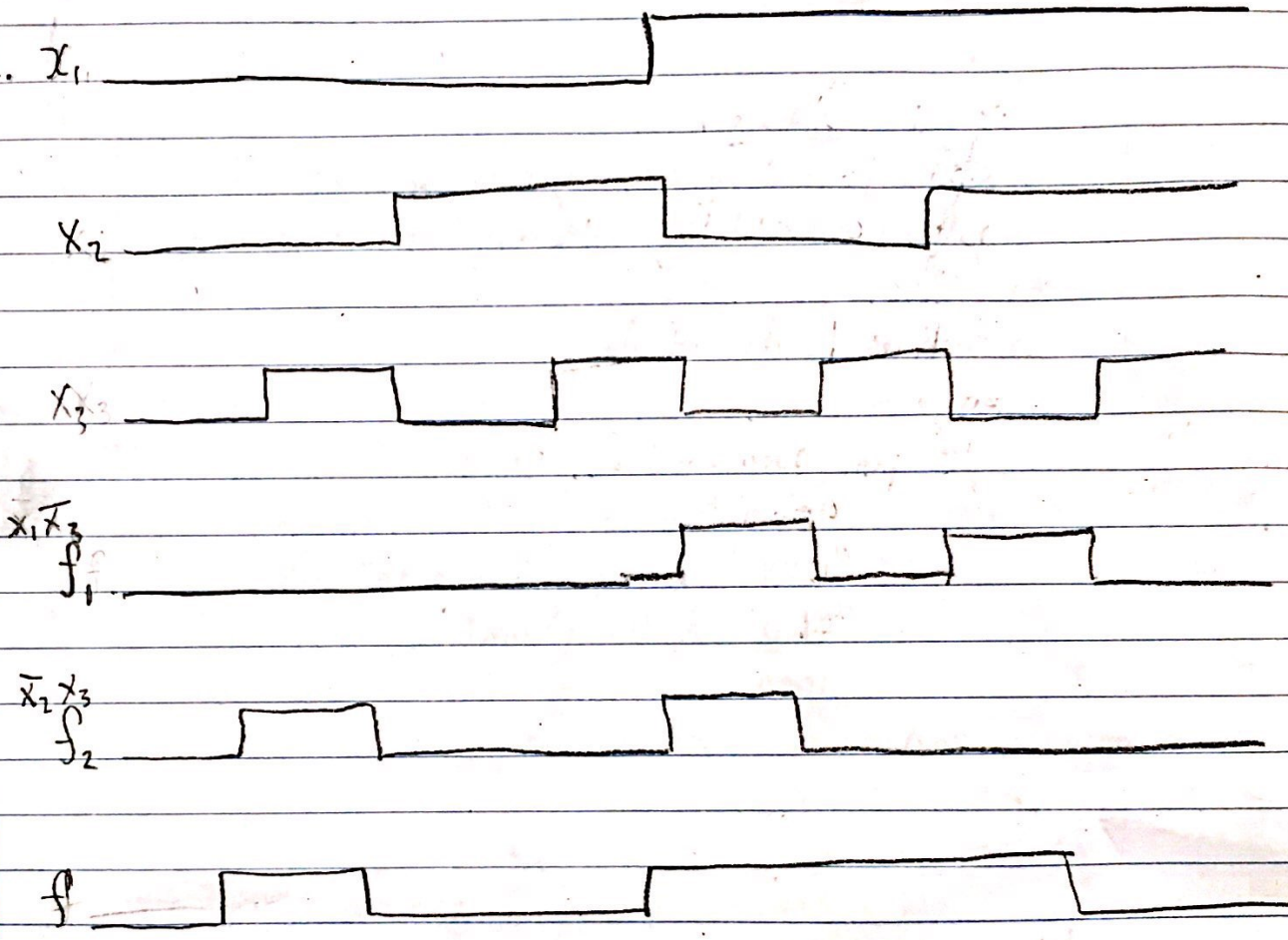
3000 12511 Eric Dam

$\bar{x}_1\ \bar{x}_2\ \bar{x}_3$

CEG 3155 A1

1.





2. $f = x_1x_3 + x_1\bar{x}_2 + \bar{x}_1x_2x_3 + \bar{x}_1\bar{x}_2\bar{x}_3$

$= (x_1x_3)(x_2+\bar{x}_2) + x_1\bar{x}_2(x_3+\bar{x}_3) + \bar{x}_1x_2x_3 + \bar{x}_1\bar{x}_2\bar{x}_3$

$= x_1x_3x_2 + x_1\bar{x}_2x_3 + x_1\bar{x}_2x_3 + x_1\bar{x}_2\bar{x}_3 + \bar{x}_1x_2x_3 + \bar{x}_1\bar{x}_2\bar{x}_3$

$= x_1x_3x_2 + x_1\bar{x}_2x_3 + x_1\bar{x}_2\bar{x}_3 + \bar{x}_1x_2x_3 + \bar{x}_1\bar{x}_2\bar{x}_3$ (complement)

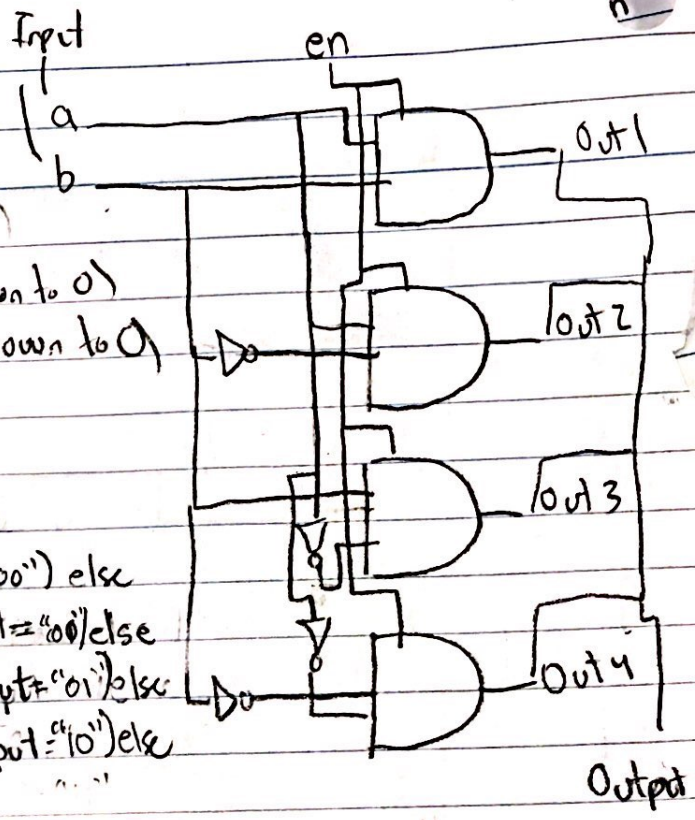
$x_1x_3(x_2+\bar{x}_2) + \bar{x}_2\bar{x}_3(x_1+\bar{x}_1) + \bar{x}_1x_2x_3$

$x_1x_3 + \bar{x}_2\bar{x}_3 + \bar{x}_1x_2x_3$

$x_3(\bar{x}_1x_2 + x_1) + \bar{x}_2\bar{x}_3$

$x_3x_2 + x_1x_3 + \bar{x}_2\bar{x}_3$

```
library ieee;
use ieee.std_logic_1164.all;
3. entity dec is
port(
en: in std_logic;
input: in std_logic_vector; (1 down to 0)
output: out std_logic_vector; (3 down to 0)
end dec;
architecture Logicfunc of dec is
begin;
  output: "0000" when (en=0) and (input="00") else
          "0001" when (en=1) and (input="00") else
          "0010" when (en=1) and (input="01") else
          "0100" when (en=1) and (input="10") else
          "1000"
end;
```




```
4. entity dec2 is
port(
   a: in std_logic_vector; (7 down to 0)
   b: in std_logic_vector; (7 down to 0)
   agtb: out std_logic;
end dec2;
architecture Logicfunc of dec2 is
begin
   agtb: '1' when (unsigned(a) > unsigned(b)) else '0'
end
```

```
library ieee;
use ieee.std_logic_1164.all;
5. entity pbx is
port (
    pb: in std_logic;
    led1: out std_logic;
    led2: out std_logic;
    led3: out std_logic;
    led4: out std_logic);
end dec3;
architecture Logicfunc of dec3 is
  begin
    Process(PB)
      begin
        if(pb="0") then
          led1<="1";
          led2<="0";
          led3<="1";
          led4<="0";
        else
          led1<="0";
          led2<="1";
          led3<="0";
          led4<="1";
        end if;
      end process
    end pbx
```