# Xilinx Kria™ System-on-Module Product Series Introduction

XILINX.

# Agenda

- Xilinx Kria™ System-on-Module — K26
  - What is SOM ?
  - Architecture
  - Compare with NVIDIA Jetson Series
  - Example: Automatic Number Plate Recognition (ANPR)
- AI Starter Kit — Kria KV260
  - Architecture
  - Design Path
  - Vitis AI
  - Example: Smart Model Select
- Robotics Starter Kit — Kria KR260
  - Architecture
  - Design Path
  - Kria Robotics Stack (KRS)

# Xilinx Kria™ System-on-Module — K26

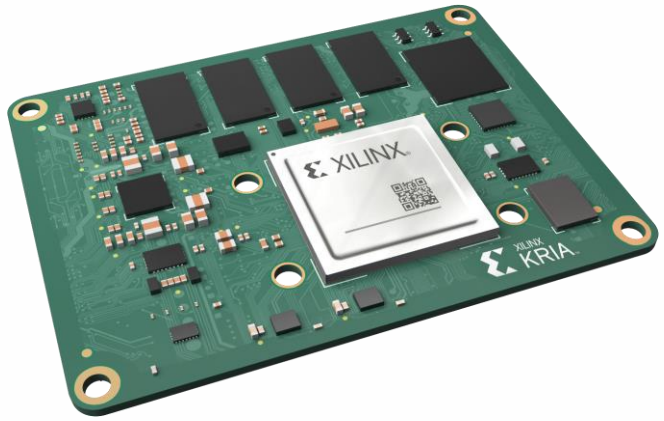
XILINX.

# What is SOM ?

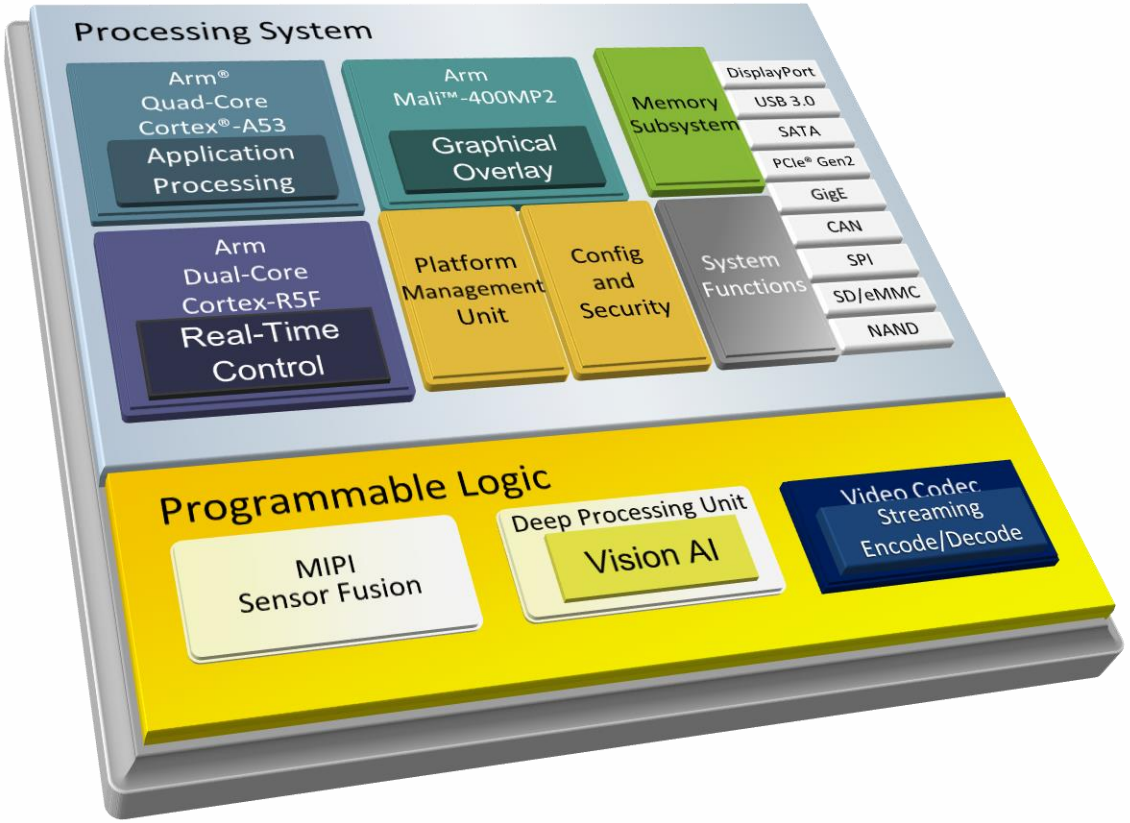
- It consists of components including CPU, GPU, memory, power management, high-speed interface, etc.

**K26**

Production SOM Module

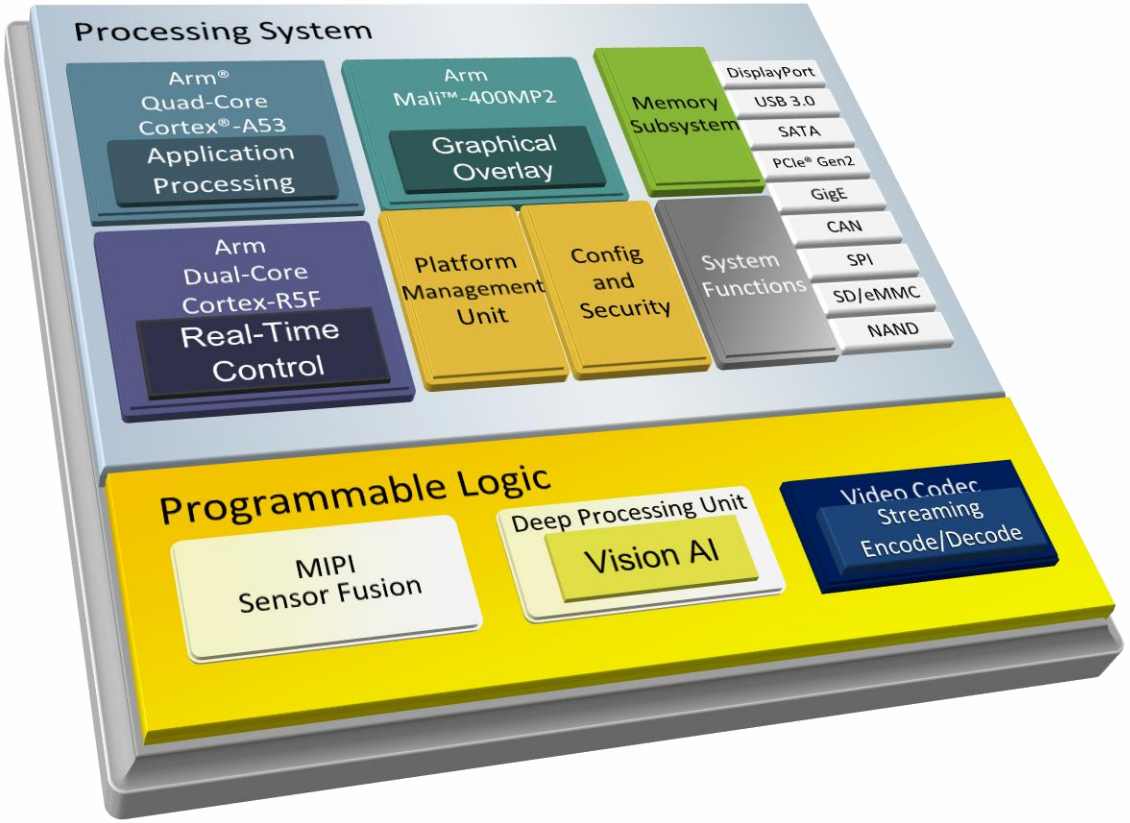



*Based on the Zynq® UltraScale+™ MPSoC Architecture*



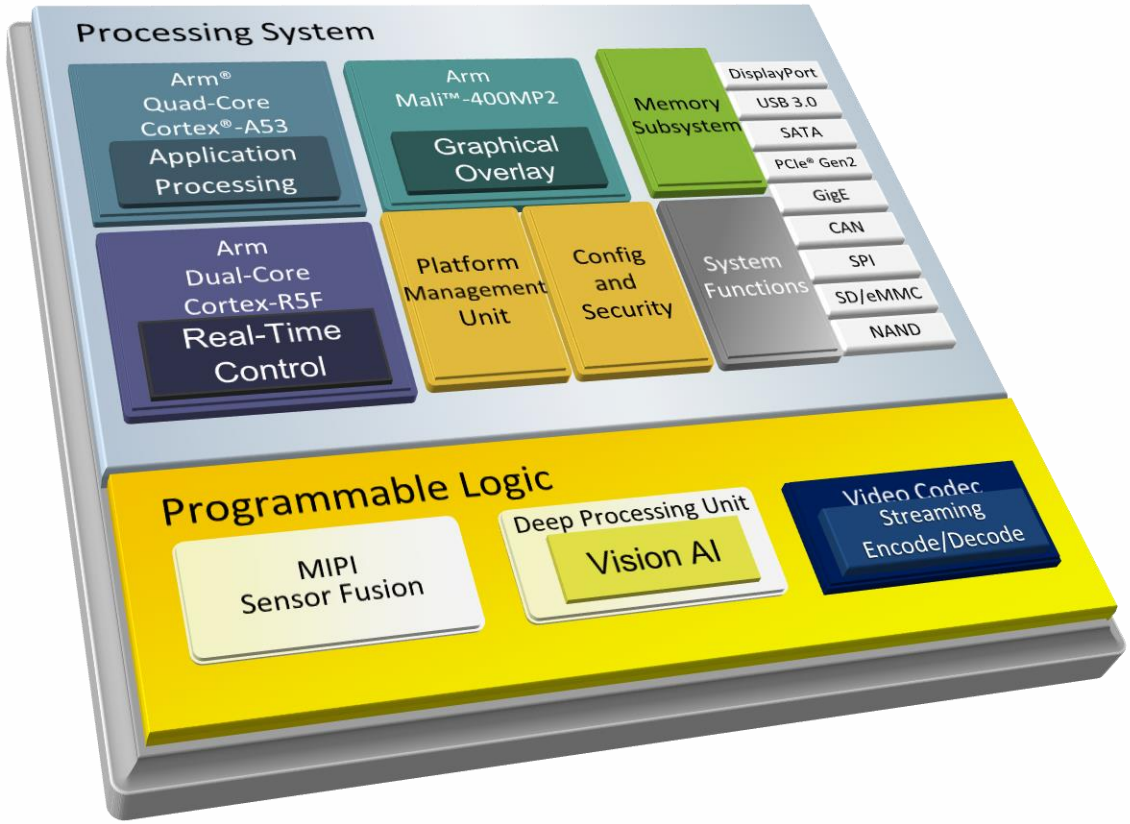
# At the Heart of the K26 SOM: Zynq® UltraScale+™ MPSoC

| COMPUTE | |
|---|---|
| **Application Processor** | 64-bit Quad-Core Arm® Cortex®-A53 |
| **Real-Time Processor** | 32-bit Dual-Core Arm Cortex-R5F |
| **Graphics Processor** | Arm Mali™-400MP2 |
| **Programmable Logic** | 256K System Logic Cells |
| **Deep Learning Processor** | 4K INT8 (upgradable to INT4) |
| **Video Codec (H.264/H.265)** | Up to 32 Streams (total resolution ≤ 4Kp60) |
| **Memory** | 26.6Mb On-Chip SRAM |
| **Security** | IEC62443 Security w/HW Root-of-Trust |



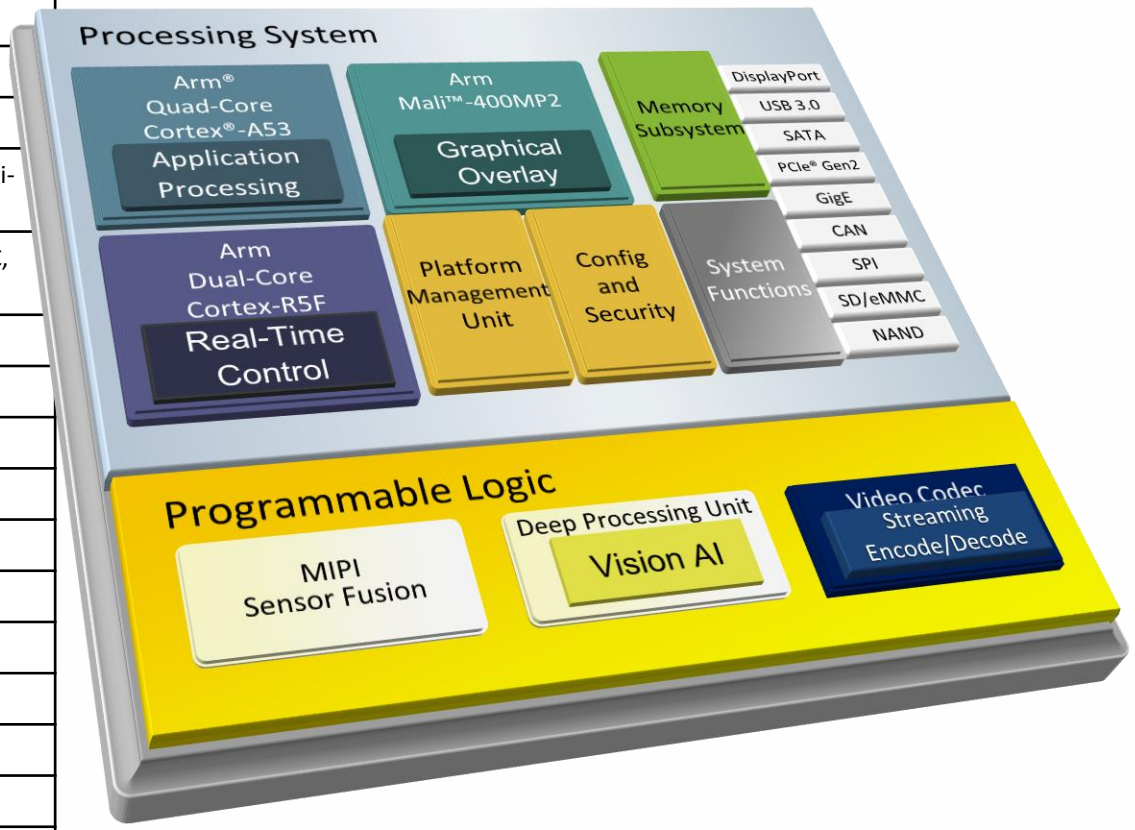
# At the Heart of the K26 SOM: Zynq® UltraScale+™ MPSoC

| INTERFACES | |
|---|---|
| **Camera** | 11 x4 Full MIPI or sub-LVDS Interfaces<br>1 x4 SLVS-EC Interfaces |
| **USB** | 4x USB 2.0 / 3.0 |
| **Multi-Media** | DisplayPort, HDMI |
| **Network** | 1Gb up to 40Gb Ethernet (w/GigE Vision) |
| **Memory Interface** | 4GB 64-bit DDR4 |
| **Transceivers** | 4x 12.5Gb/s, 4x 6Gb/s |
| **Mechanical** | 77 x 60 x 11mm w/ dual 240-pin connectors |



# At the Heart of the K26 SOM: Zynq® UltraScale+™ MPSoC

| | | |
|---|---|---|
| **Processor Unit & Acceleration** | Application Processor | Quad-core Arm® Cortex®-A53 MPCore™ up to 1.5GHz |
| | Real-Time Processor | Dual-core Arm Cortex-R5F MPCore up to 600MHz |
| | Graphics Processing Unit | Mali™-400 MP2 up to 667MHz |
| | Video Codec Unit (VCU) | 1 - up to 32 streams (total resolution ≤ 4Kp60) |
| | Trusted Platform Module (TPM) | Infineon 2.0 |
| **Memory** | On-Chip* | 26.6Mb On-Chip SRAM |
| | On-SOM | 4GB 64-bit DDR4 (non-ECC) and 16GB eMMC |
| **Connectivity** | High-Speed PS Connectivity (GTR) | PCIe® Gen2 x4, 2x USB3.0, SATA 3.1, DisplayPort, 4x Tri-mode Gigabit Ethernet |
| | General PS Connectivity (MIO) | 2x USB 2.0, 2x SD/SDIO, 2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO |
| **Transceivers** | GTH 12.5Gb/s Transceivers | 4 (PCIe Gen3 x4, SLVS-EC, HDMI 2.0, DisplayPort 1.4) |
| | GTR 6Gb/s Transceivers | 4 |
| **I/O Count** | PS MIO (1.8V) | 52 |
| | PL High-density (HD) I/O (3.3V) | 69 |
| | PL High-performance (HP) I/O (1.8V) | 116 |
| **Programmable Logic** | System Logic Cells (K) | 256 |
| | DSP Slices | 1,248 |
| **Power & Thermal** | Typical Power | 7.5W |
| | Maximum Power** | 15W |
| | Thermal Interface | Passive (Heat spreader) |
| **Speed and Temp Grade** | Commercial | -2 speed grade, low voltage and 0 to 85°C temperature range |
| | Industrial | -2 speed grade, low voltage and –40 to 100°C temperature range |




XILINX.

# Ruggedization for Extreme Operating Conditions Including Industrial Applications

- Built for indoor/outdoor and low/high temperature ranges
- Meets country-specific compliance / certification requirements
- Ruggedized connectors for shock-resistance


## Meeting Reliability Requirements

| | Kria K26 SOM | |
|---|---|---|
| | C-Grade | I-Grade[1] |
| Shock | 40G, 11ms | 40G, 11ms |
| Vibration | 1.9g RMS | 5g RMS |
| Temp Range at module TTP | 0°C to 85°C | –40°C to 100°C |
| Humidity | 85°C / 80% RH | 85°C / 80% RH |
| Operating Life[2] | 5 years | 10 years |
| Availability[3] | 10 years | 10 years |
| Warranty (Production SOM)[4] | 2 years | 3 years |

1: I-grade specs are tentative and subject to change
2: Operating Life – Suitable for deployment in a production environment
3: Availability – Time period SOM product will be available for purchase
4: Kria KV260 Starter Kits are not intended for production use and come with a 90-day warranty

## Certifications

| Country | Certification |
|---|---|
| US ; Canada | FCC, UL ; IC |
| EU | CE, ROHS 10 |
| China | CC, ROHS 10 |
| Vietnam | ICT |
| Japan ; Korea | VCCI ; KCC |
| Malaysia | ST CoA, SIRIM |
| Singapore | SPRING Safety |
| South Africa | SABS EMC, NRSC |



AMD XILINX

# Accessible Vision Applications for SW & AI Developers


Security Cameras


Smart City

Retail Analytics

Machine Vision

Vision-Guided Robotics

# K26 SOM as an Edge Device

1. Compute Power

* DPU (Deep Learning Processing Unit)

| | DPU B3136 | DPU B4096 | Jetson Nano<br>NVIDIA Maxwell architecture with 128 NVIDIA CUDA® cores |
|---|---|---|---|
| Compute Power | 0.94 TOPS | 1.22 TOPS | 0.472 TOPS |

| DPU Configuration | LUTs | Registers | BRAM | DSP |
|---|---|---|---|---|
| B256 (8x4x4) | 16132 | 25064 | 43 | 66 |
| B256 (2x8x8) | 15286 | 22624 | 53.5 | 50 |
| B288 (4x6x6) | 15812 | 23689 | 46 | 62 |
| B512 (4x8x8) | 20177 | 31782 | 69.5 | 98 |
| B1024 (8x8x8) | 27377 | 46241 | 101.5 | 194 |
| B1152 (4x12x12) | 28698 | 46906 | 117.5 | 194 |
| B1600 (8x10x10) | 30877 | 56267 | 123 | 282 |
| B2304 (8x12x12) | 34379 | 67481 | 161.5 | 386 |
| B3136 (8x14x14) | 38555 | 79867 | 203.5 | 506 |
| B4096 (8x16x16) | 40865 | 92630 | 249.5 | 642 |

# K26 SOM as an Edge Device

1. Compute Power

* DPU (Deep Learning Processing Unit)

| | DPU B3136 | DPU B4096 | Jetson Nano<br>NVIDIA Maxwell architecture with 128 NVIDIA CUDA® cores |
|---|---|---|---|
| Compute Power | 0.94 TOPS | 1.22 TOPS | 0.472 TOPS |

| Convolution Architecture | Pixel Parallelism (PP) | Input Channel Parallelism (ICP) | Output Channel Parallelism (OCP) | Peak Ops (operations/per clock) |
|---|---|---|---|---|
| B512 | 4 | 8 | 8 | 512 |
| B800 | 4 | 10 | 10 | 800 |
| B1024 | 8 | 8 | 8 | 1024 |
| B1152 | 4 | 12 | 12 | 1150 |
| B1600 | 8 | 10 | 10 | 1600 |
| B2304 | 8 | 12 | 12 | 2304 |
| B3136 | 8 | 14 | 14 | 3136 |
| B4096 | 8 | 16 | 16 | 4096 |

In each clock cycle, the convolution array performs a multiplication and an accumulation, which are counted as two operations.
Thus, the peak number of operations per cycle is equal to PP*ICP*OCP*2.

Work at 300MHz:

- B3136 $8 \times 14 \times 14 \times 2 \times 3 \times 10^8 = 0.9408 \times 10^{12}$
- B4096 $8 \times 16 \times 16 \times 2 \times 3 \times 10^8 = 1.2288 \times 10^{12}$

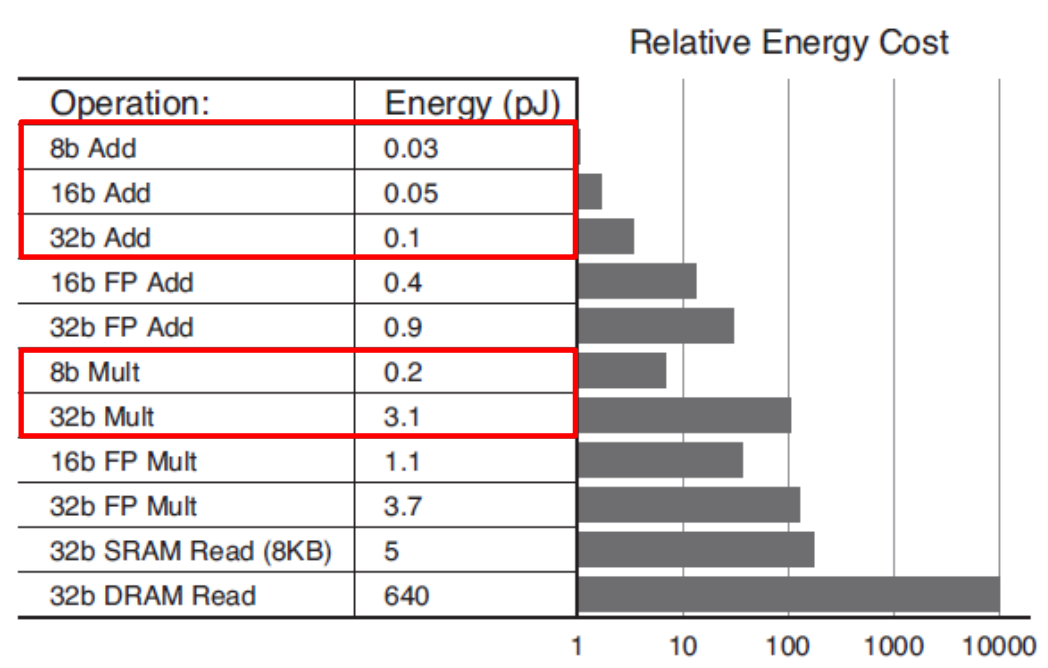
# K26 SOM as an Edge Device

1. Compute Power

* DPU (Deep Learning Processing Unit)

| | DPU B3136 | DPU B4096 | Jetson Nano<br>NVIDIA Maxwell architecture with 128 NVIDIA CUDA® cores |
|---|---|---|---|
| Compute Power | 0.94 TOPS | 1.22 TOPS | 0.472 TOPS |

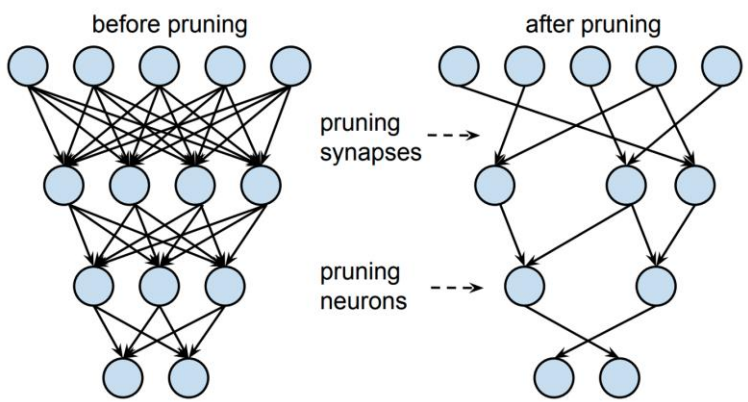
2. Low Power

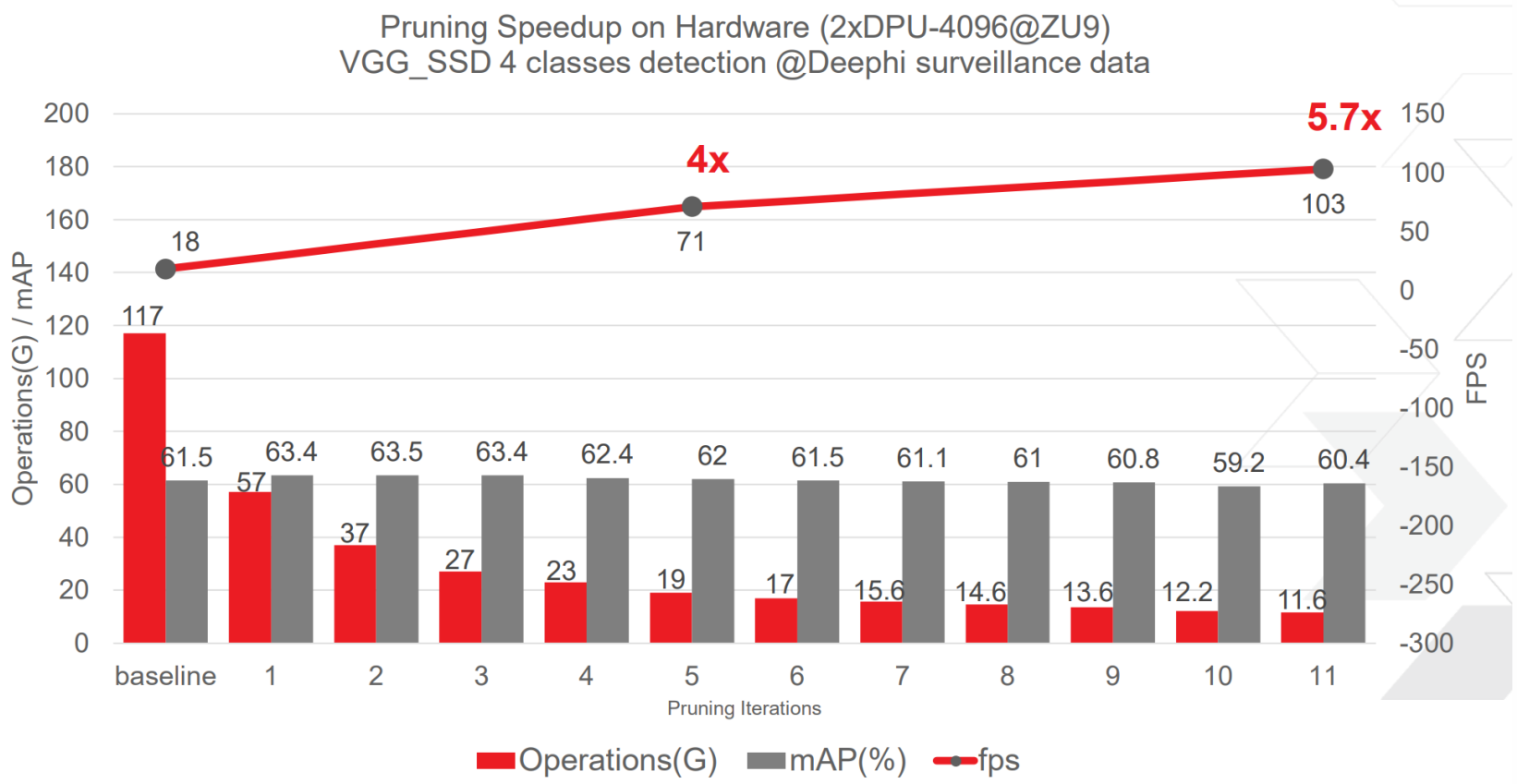



- K26 can support INT8 precision through quantizing by Vitis AI, but Nvidia Jetson Nano and Nvidia Jetson TX2 support FP16 precision because these Nvidia devices do not have lower precision support of INT8.

# K26 SOM as an Edge Device

- Pruning



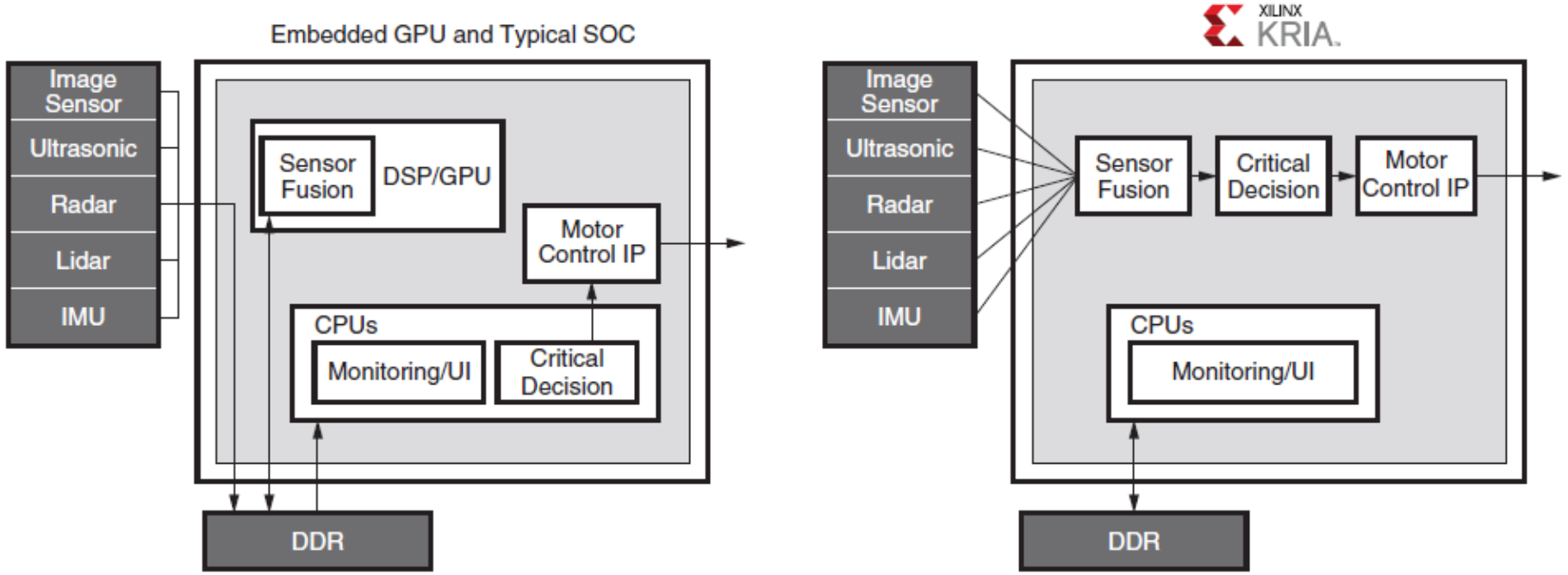






XILINX.

# K26 SOM as an Edge Device

3. Low Latency




4. Flexibility

- Reconfigure the data path specifically to achieve maximum throughput and lower latencies.
- Any-to-any I/O connection enables the K26 SOM to connect to any device, network, or storage device without the need for a host CPU.

# Compare with NVIDIA Jetson Series — Hardware

| No. | Feature | Xilinx's K26 SOM | Nvidia Jetson Nano[1] | Nvidia Jetson TX2[1] |
|---|---|---|---|---|
| 1 | Application Processor | Quad-core Arm® Cortex®-A53 MPCore™ up to 1.5GHz | Quad-Core Arm Cortex-A57 MPCore processor | Dual-Core Nvidia Denver 2 64-Bit CPU and Quad-Core Arm Cortex-A57 MPCore processor |
| | Real-time Processors | Dual-core Arm Cortex-R5F MPCore up to 600MHz | | |
| 2 | GPU | Mali™-400 MP2 up to 667MHz (primarily used for graphics rendering) | 128-core Nvidia Maxwell GPU | 256-core Nvidia Pascal GPU |
| 3 | Machine Learning Throughput | 1.36TOPS[2] | 472GFLOPs (FP16) | 1.33TFLOPs (FP16)<br>1.26TFLOPs for TX2i |
| 4 | Camera Interfaces | MIPI:<br>Up to 44 DPHY2.0 lanes,<br>Up to 11 Cameras,<br>Max BW 10Gb/s BW per interface,<br>Up to 16 virtual channels per interface | 12 DPHY1.1 x 4 lanes<br>Up to 4 Cameras<br>Max BW 6Gb/s per interface | 12 DPHY 1.1 lanes<br>Up to 6 cameras<br>Max BW 6Gb/s per camera |
| | | SLVS, LVDS:<br>11 x4 SLVS or LVDS cameras interfaces | NA | NA |
| | | SLVS-EC:<br>4 lane, 5Gb/s /lane | NA | NA |
| 5 | Display Interface | DP1.2 x 2 lane | 2x HDMI 2.0,<br>DP 1.2,<br>eDP 1.2,<br>2x MIPI DSI x2 lanes<br>(1.5Gb/s /lane) | 2x HDMI 2.0,<br>DP 1.2,<br>eDP 1.2,<br>2x MIPI DSI |
| | | Additional HDMI 2.0 (GTs),<br>DisplayPort 1.4 (GTs) with Soft IPs,<br>MIPI DSI x4 lane<br>(2.5Gb/s /lane) w/ Soft IPs | NA | NA |
| 6 | Video Encode H.264/H.265 | Up to 32 simultaneous streams,<br>Max resolution 4K @60FPS<br>Color format:<br>422 8/10 bpc and 420 8/10bpc | Up to 9 streams;<br>Max resolution 4K<br>@30 FPS 420 8bpc | Up to 8 streams H.265,<br>14 streams of H.264,<br>Max resolution 4K<br>@60FPS 420 8bpc |
| 7 | Video Decode H.264/H.265 | Up to 32 simultaneous streams,<br>Max resolution 4K @60FPS<br>Color format: 422 8/10bpc and 420 8/10bpc | Up to 9 streams;<br>Max resolution 4K<br>@60 FPS 420 8bpc | Up to 32 streams H.265,<br>16 streams of H.264,<br>Max resolution 4K<br>@60FPS 420 8bpc |
| 8 | Wireless | GTR M.2/SATA | M.2 Key-E site on carrier | 802.11a/b/g/n/ac 2×2 867Mb/s \|<br>Bluetooth 4.1<br>BCM4354 on module |
| 9 | Ethernet | 4x 10/100/1000 Base-T Ethernet<br>Additional Ethernet ports with Soft IP in HP I/Os | 10/100/1000 Base-T Ethernet | 10/100/1000 Base-T Ethernet |
| 10 | USB | 2xUSB3.0, 2x USB2.0 | 4x USB 3.0 +<br>Micro-USB 2.0 | USB 3.0 + USB 2.0 |
| 11 | PCIe® | PCIe Gen2 x 4<br>PCIe Gen3 x4 in with Soft IP on GTs | PCIe Gen2 x4 lanes | PCIe Gen2 x5 lanes |
| 12 | High-speed I/O (GTs) Provides Additional Interface Support | 4x GTH transceivers in programmable logic can be configured to support a plethora of high-speed protocols such as SLVS - EC, PCIe Gen 3, HDMI, 10GE and many more .... | NA | NA |
| 13 | I/O Flexibility | 69 3.3V I/Os, 116 1.8V I/Os allows users to create highly flexible and configurable I/O interfaces in programmable logic | NA | NA |
| 14 | Programmable Logic | 256K System Logic Cells, 1248 DSPs, 26.6Mb on-chip memory allows users to implement custom accelerators for vision and ML functions | NA | NA |
| 15 | DRAM | 4GB 64-bit DDR4 | 4GB 64-bit DDR4 | 8GB 128-bit LPDDR4? |
| 16 | eMMC | 16GB | 16GB | 32GB |
| 17 | Flash | 512MB QSPI | NA | NA |
| 18 | Socket Carrier Card Interface | Two 240-pin connectors | 260-pin edge connector | 400-pin board-to-board connector |

**Notes:**

1. Source: https://developer.nvidia.com/embedded/jetson-modules
2. The Deep learning processor's performance is based on Xilinx DPU configurations B4096 @ 333MHz, which is implemented in the programmable logic.

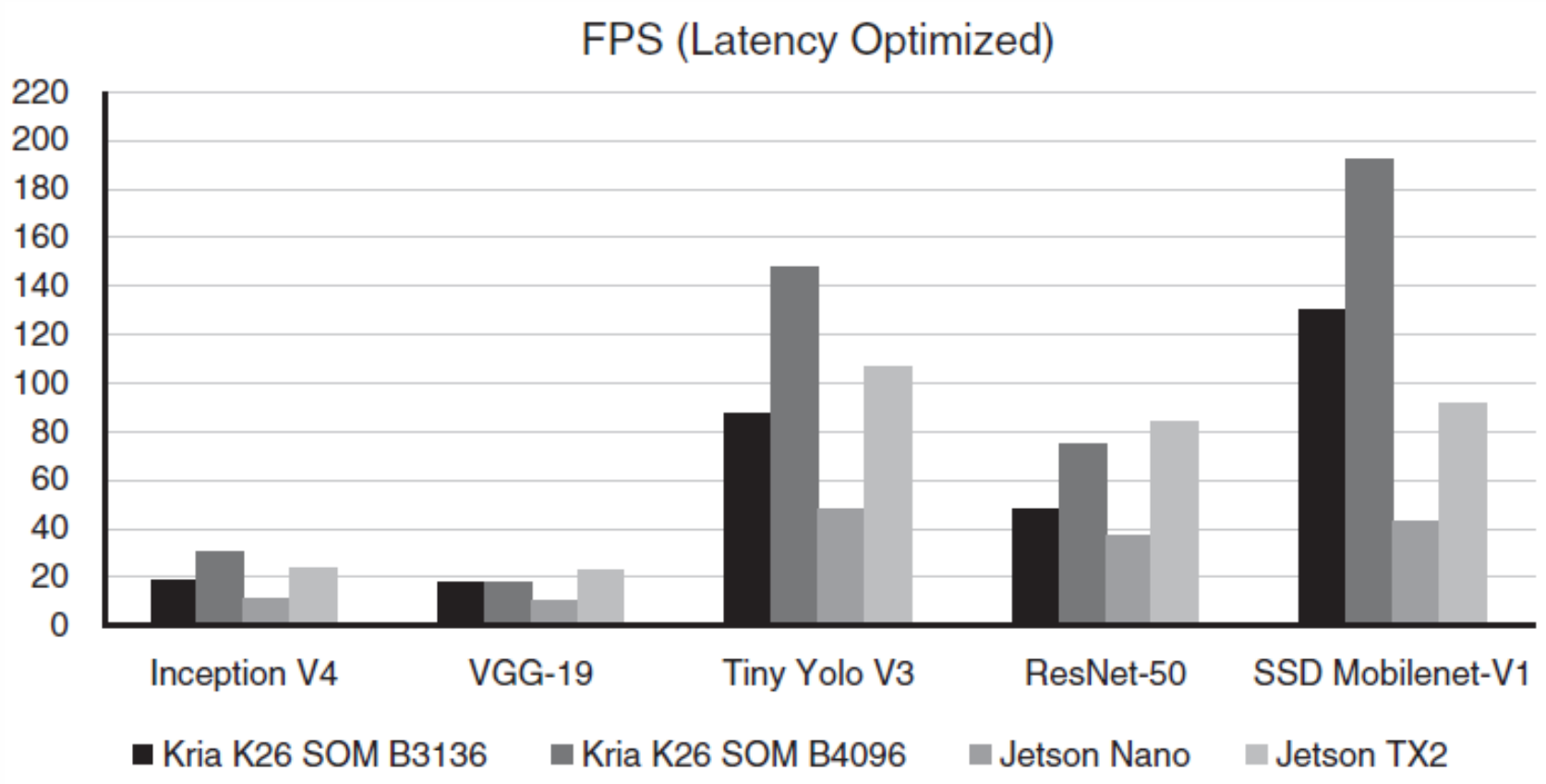
# Compare with NVIDIA Jetson Series — Models

- Performance numbers for Nvidia Jetson Nano and Nvidia Jetson TX2 are reported with FP16 precision, as these Nvidia devices do not have lower precision support of INT8.
- Both Xilinx and Nvidia performance applications use synthetic data as input and do not include pre- and post-processing time in reporting.

**Deep Learning Models Performance Comparison**

| No. | Model | Image Size | Xilinx K26 B3136 DPU | | Xilinx K26 B4096 DPU | | Nvidia Jetson Nano | | Nvidia Jetson TX2 | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | FPS (Latency Optimized)(1) | FPS (Throughput Optimized)(2) | FPS (Latency Optimized) | FPS (Throughput Optimized) | FPS (Latency Optimized) | FPS (Throughput Optimized) | FPS (Latency Optimized) | FPS (Throughput Optimized) |
| 1 | Inception V4 | 299x299 | 19 | 19.1 | 30.3 | 30.4 | 11 | 13 | 24 | 32 |
| 2 | VGG-19 | 224x224 | 17.9 | 17.9 | 17.4 | 17.4 | 10 | 12 | 23 | 29 |
| 3 | Tiny Yolo V3 | 416x416 | 88.2 | 92.6 | 148.0 | 161.3 | 48 | 49 | 107 | 112 |
| 4 | ResNet-50 | 224x224 | 49 | 49.1 | 75.6 | 75.9 | 37 | 47 | 84 | 112 |
| 5 | SSD Mobilenet-V1 | 300x300 | 129.6 | 133.4 | 192.1 | 200.4 | 43 | 48 | 92 | 109 |
| 6 | SSD ResNet34 | 1200x1200 | 1.6 | 1.6 | 2.5 | 2.5 | 1 | 1 | 3 | 2 |

# Compare with NVIDIA Jetson Series — Models



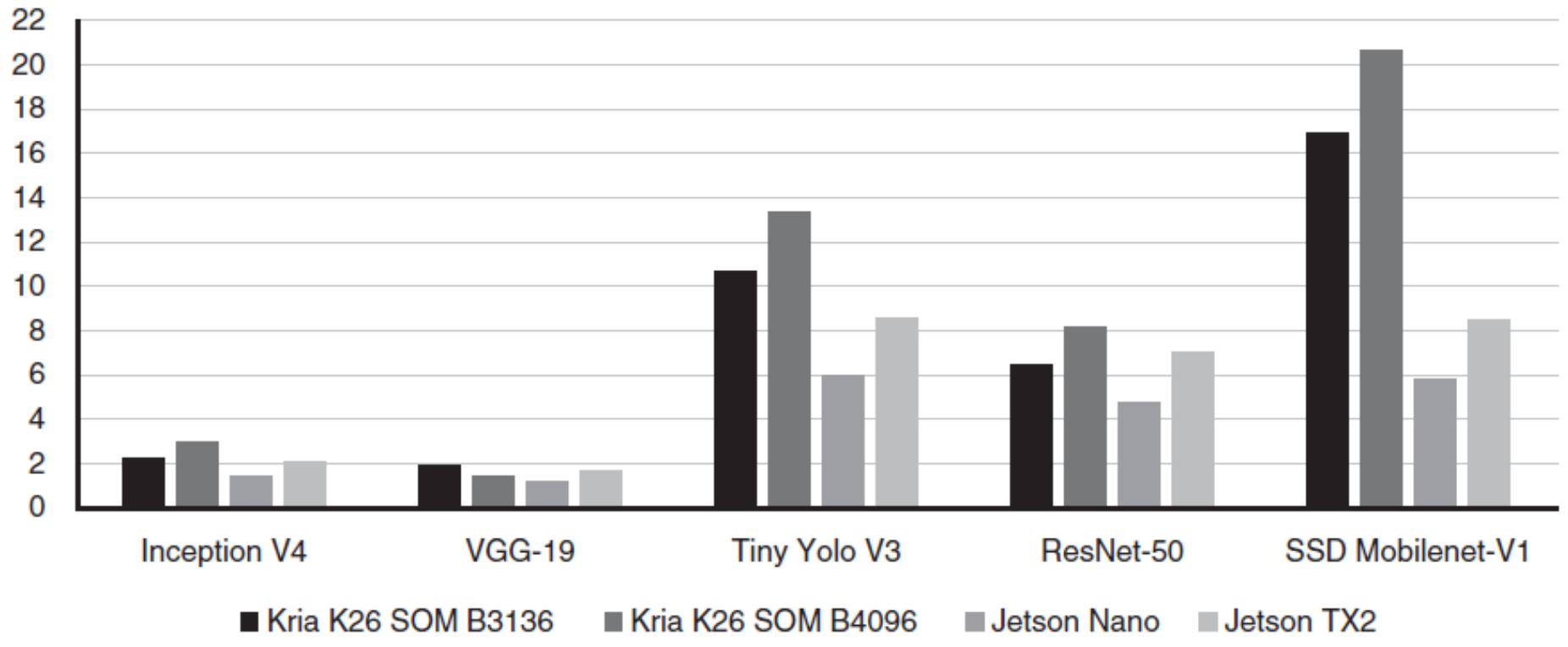

**FPS Measurement (Latency Optimized)**

# Compare with NVIDIA Jetson Series — Models

**Peak Power Measurement (In Watts)**

| No. | Model | Xilinx K26 SOM B3136 DPU | Xilinx K26 SOM B4096 DPU | Nvidia Jetson Nano | Nvidia Jetson TX2 |
|---|---|---|---|---|---|
| 1 | Inception V4 | 8.09 | 10.10 | 7.40 | 11.20 |
| 2 | VGG-19 | 8.55 | 11.28 | 8.10 | 13.10 |
| 3 | Tiny Yolo V3 | 8.26 | 11.08 | 7.80 | 12.30 |
| 4 | ResNet-50 | 7.47 | 9.28 | 7.70 | 11.70 |
| 5 | SSD Mobilenet-V1 | 7.67 | 9.29 | 7.30 | 10.80 |

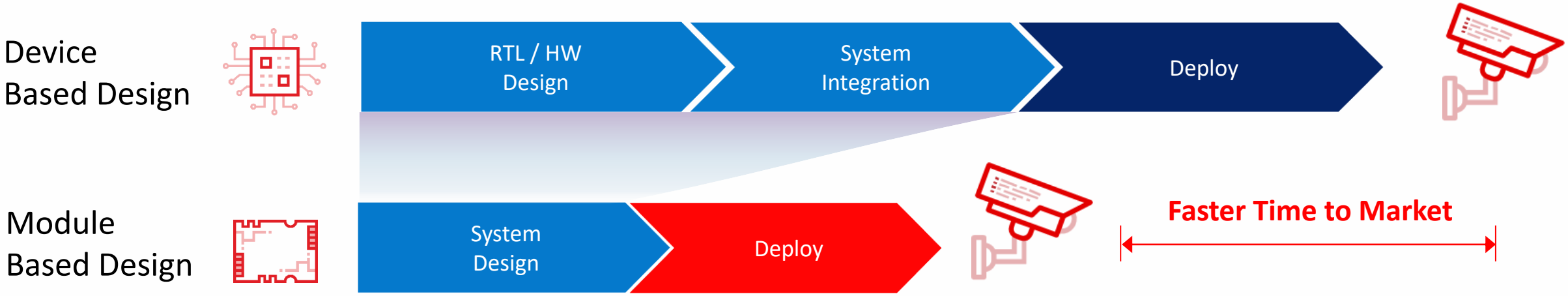
# Compare with NVIDIA Jetson Series — Models




**FPS/Watt**

# Accelerating & Simplifying Design Cycle & Productization

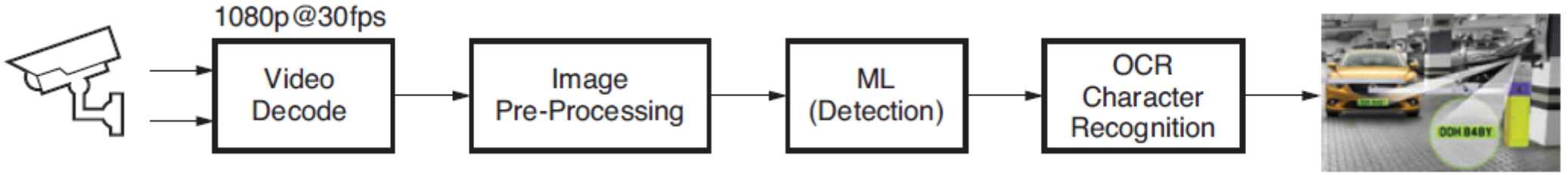
- SOM Advantages over Chip-Down Design




- ✓ Reduce development time by designing at higher abstraction
- ✓ Lower bill of materials (BOM) cost
- ✓ Simplified inventory management
- ✓ Turnkey longevity and product life cycle management

**Faster Productization for High Volume Deployment**

# Example: Automatic Number Plate Recognition (ANPR)




- Work with Uncanny Vision

Uncanny Vision®

| Hardware (Module) | Xilinx Kria K26 SOM | Nvidia Jetson Nano | Nvidia Jetson TX2 4GB |
|---|---|---|---|
| Price | $250 | $129 | $299 |
| FPS | 33 | 8 | 23 |
| Number of Streams (assuming 10fps per stream) | 3 | ~1 | 2 |
| $/streams | $83 | $129 | $150 |
| Max Power (SOM only) | 15W | 10W | 15W |
| Watts/stream | 5 | 10 | 7.5 |

# Xilinx K26 SOM Summary

## Pre-Built HW Acceleration

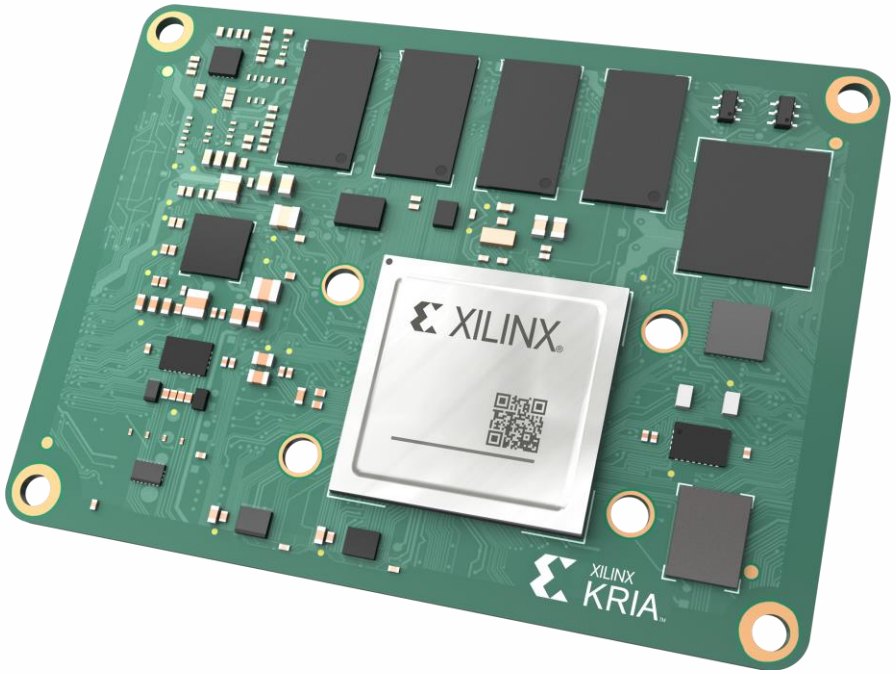
- Application designs included for common AI functions
- 'Out-of-the-box' ready for SW developers

## 3X Performance[1]

- AI at half the power with low latency
- Accelerates the whole application from AI to control

## Future Proof

- Adaptable to changing AI and sensor requirements
- Ruggedized for industrial life cycles
- Path from concept to production to design revisions




Embedded Design Simplicity with System Flexibility

# AI Starter Kit — Kria KV260

XILINX.

# AI Starter Kit — Kria KV260

**KV260**

Vision AI Starter Kit


**K26**

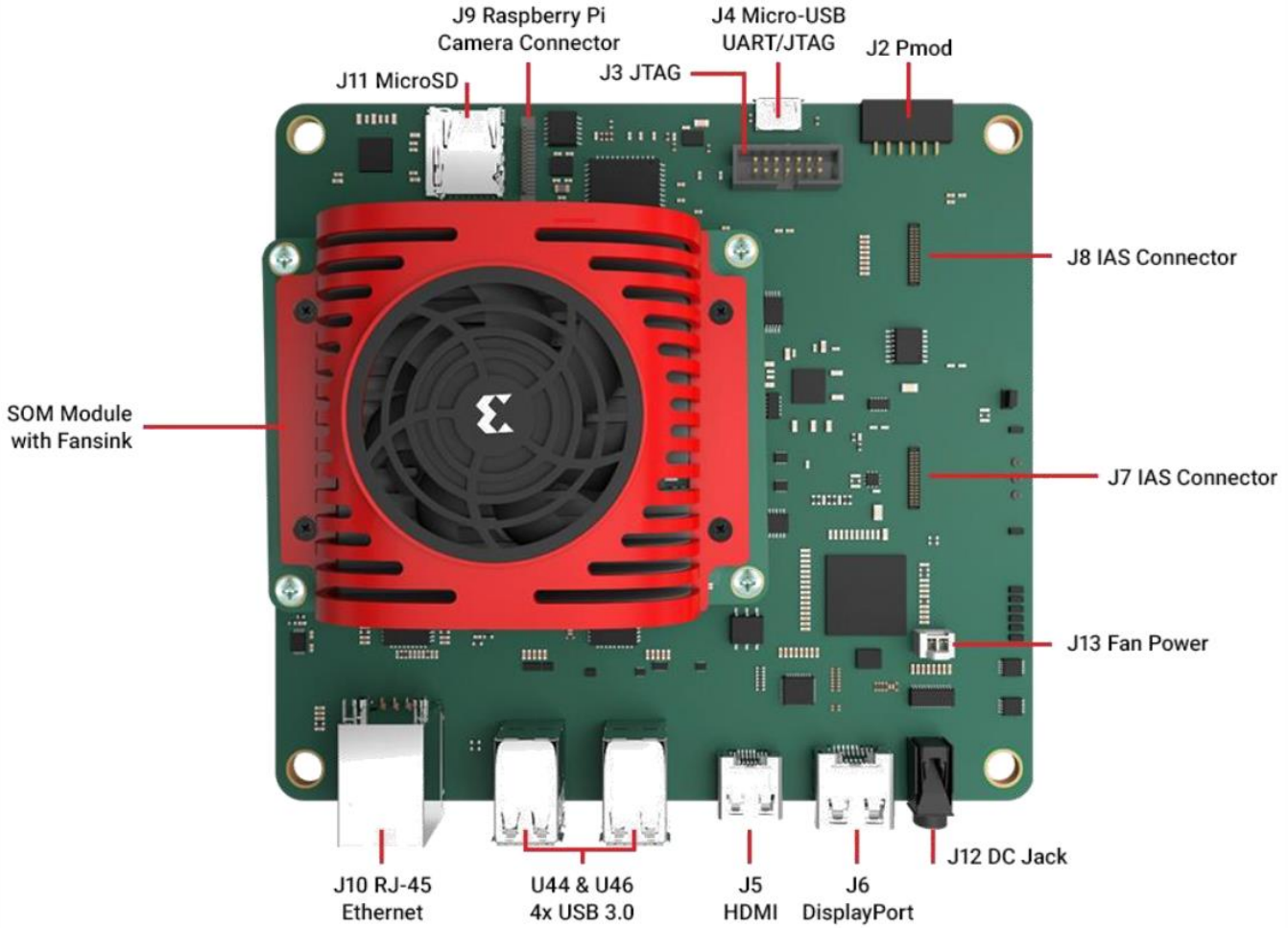
Production SOM Module


DEVELOP ⋯⋯▶ DEPLOY

# AI Starter Kit — Kria KV260

## KV260

Vision AI Starter Kit


XILINX

# AI Starter Kit — Kria KV260

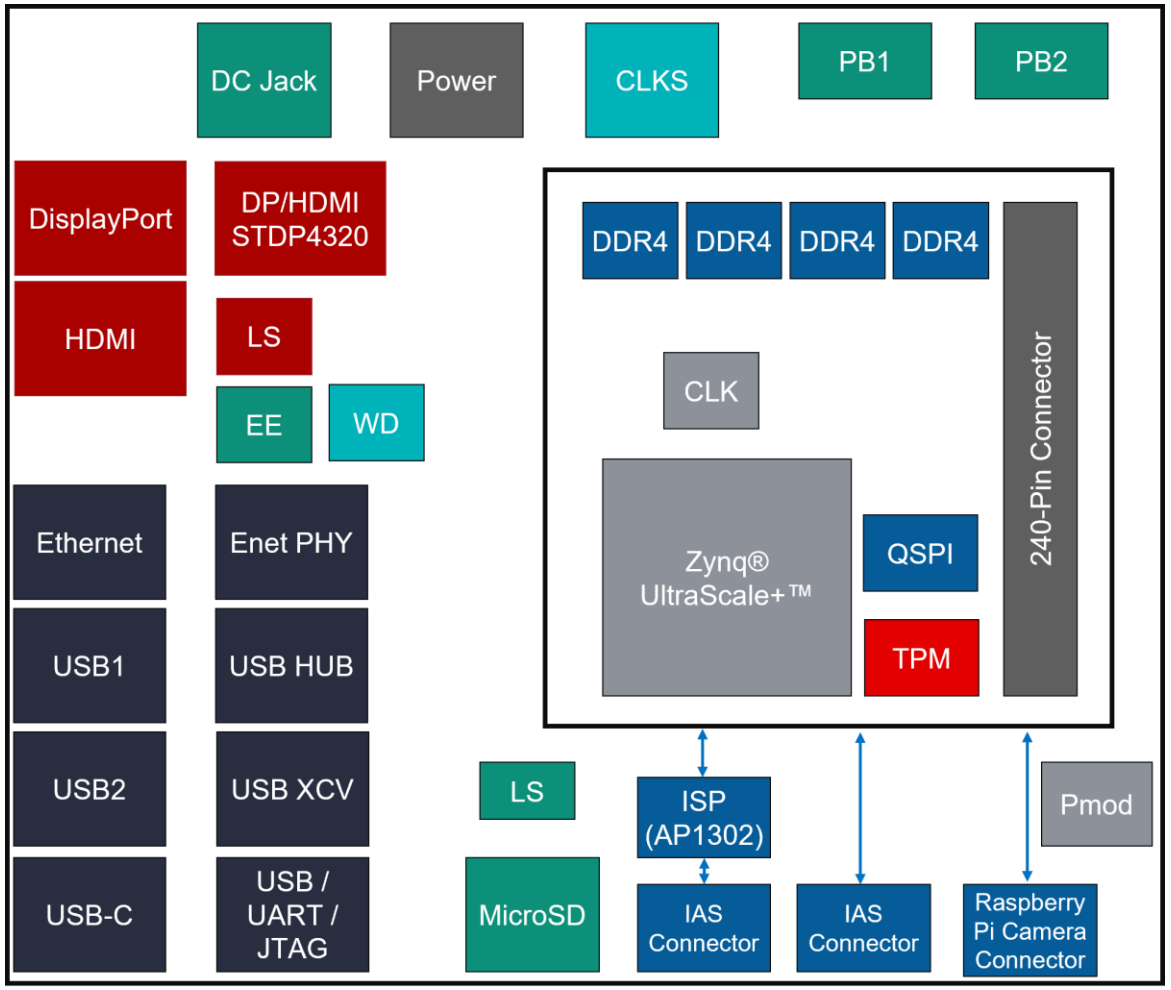
### Carrier Card Optimized for Kria SOM
- 240-pin connectivity to SOM
- Targeting vision applications

### Vision Ready
- 3 MIPI sensor interfaces, USB cameras
- Built-in ISP component (OnSemi)
- HDMI, DisplayPort outputs

### Network & General Connectivity
- 1Gb Ethernet
- USB 3.0 / 2.0

### Pmod Expansion
- Extend to any sensor or interface
- Access Pmod ecosystem

- Production SOM includes eMMC and additional 240-pin connector




119mm x 140mm x 36mm
(SOM + Carrier Card + Heatsink)

XILINX.

# KV260 vs. K26 Multimedia Features

| | | K26 SOM | KV260 Vision AI Starter Kit |
|---|---|---|---|
| Video CODEC | Encode | 4K@60 422 /420 10bpc/8bpc (total BW < 4K@60fps)<br>H.264 or H.265<br>Simultaneous encode up to 32 streams<br>Ultra-low latency and low latency modes<br>ROI encoding | 4K@30 422 /420 10bpc/8bpc (total BW < 4K@60fps)<br>H.264/H.265<br>Simultaneous encode up to 32 streams<br>Ultra-low latency and low latency modes<br>ROI encoding |
| | Decode | 4K@60 422 /420 10bpc/8bpc (total BW < 4K@60fps)<br>H.264 or H.265<br>Simultaneous encode up to 32 streams<br>Ultra-low latency and low latency modes<br>ROI decoding | 4K@30 422 /420 10bpc/8bpc (total BW < 4K@60fps)<br>H.264/H.265<br>Simultaneous encode up to 32 streams<br>Ultra-low latency and low latency modes<br>ROI decoding |
| Camera Inputs | MIPI | Up to 11 x4 DPHY2.0 interfaces<br>Each interface supports up to 10Gb/s BW (>16MP)<br>Configurable as x1 or x2 or x4 DPHY lanes<br>Up to 16 virtual channels per interface | 3x MIPI DPHY interfaces<br>1Gb Ethernet<br>2 x4 lanes MIPI CSI with IAS camera connectors<br>One IAS interface includes OnSemi AP1302 4K HDR ISP<br>1x 2 lanes MIPI CSI with RaspberryPI camera connector |
| | SLVS-EC | One x4 5Gbs/lane | Not bonded out |
| | LVDS/SLVS | 11 x4 LVDS or SLVS camera interfaces | 10 lanes of LVDS or SLVS interfaces over IAS or Rpi connectors |
| Display Out | | 1x DP1.2, x2 lane up to 4K@30<br>1x HDMI 2.0 (over GTs)<br>1x DP1.4 (over GTs)<br>MIPI DSI display out over DPHY lanes | 1x DP1.2, up to 4K@30<br>1x HDMI 1.4 up to 4K@30 |
| GPU | | Mali™-400 MP2 | Mali-400 MP2 |
| ISP | | FPGA programmable logic allows multiple instantiations of flexible, customized ISP implementations | One IAS interface includes OnSemi AP1302 4K HDR ISP<br>Additional ISPs can be instantiated in programmable logic |
| Vision Accelerator | | Open-source XfOpenCV accelerated vision processing functions | Open-source XfOpenCV accelerated vision processing functions |
| Multimedia Stack | | V4L and DRM framework support for all video functions with GStreamer plugins | V4L and DRM framework support for all video functions with GStreamer plugins |
| Socket Carrier Card Interface | | Two 240-pin connectors (SOM240_1 and SOM240_2) | Only connect to SOM240_1 so this can't use GTH |

# Design Path for Any Developer

TIME

AI Developer

Customize AI Model

Custom AI application, AI processor configured to your requirements

XILINX VITIS AI

Embedded Developer

Application SW

Customize application SW targeting Arm Cortex-A53 processing subsystem

XILINX VITIS

Software Developer

Customize Vision Pipeline

Change and accelerate vision pre- and post-processing purely in SW dev environment

XILINX VITIS

HW Developer

*Optional, Not Required*

Full Custom RTL Development

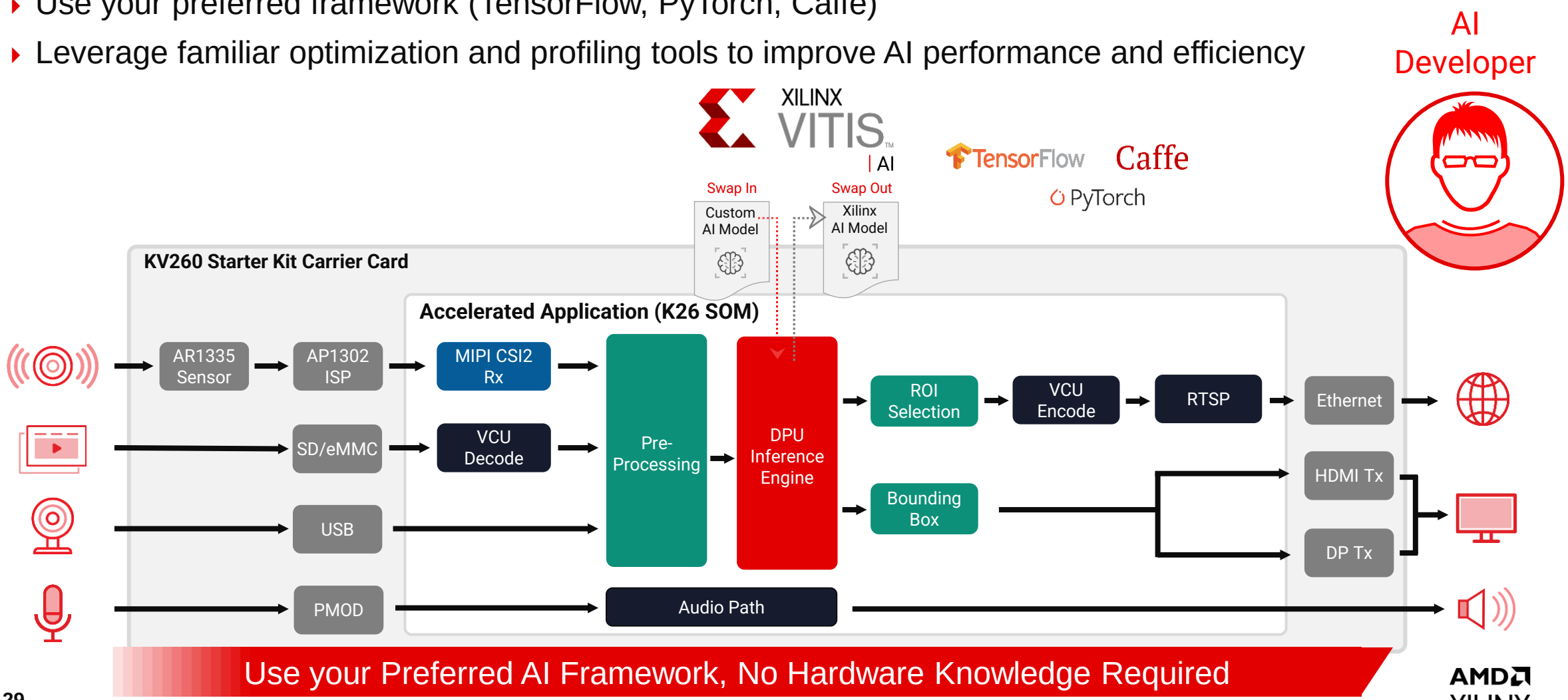
Ultimate flexibility for HW acceleration & differentiation

VIVADO

AMD XILINX

# Design with Vitis AI to Customize Your AI Models

- Use Vitis™ AI to swap in your own custom AI model (running on DPU)
- Use your preferred framework (TensorFlow, PyTorch, Caffe)
- Leverage familiar optimization and profiling tools to improve AI performance and efficiency




Use your Preferred AI Framework, No Hardware Knowledge Required



AMD XILINX

# Design with Vitis to Accelerate Vision Pipeline

## *Hardware Acceleration of Vision Pre- and Post-Processing Functions*

- Leverage pre-built, HW accelerated libraries (400+ libs available) and customize in SW
- Design custom hardware in C, C++, OpenCL
- Change vision sensors via SW

Software Developer




Customize Hardware Purely with a SW Workflow



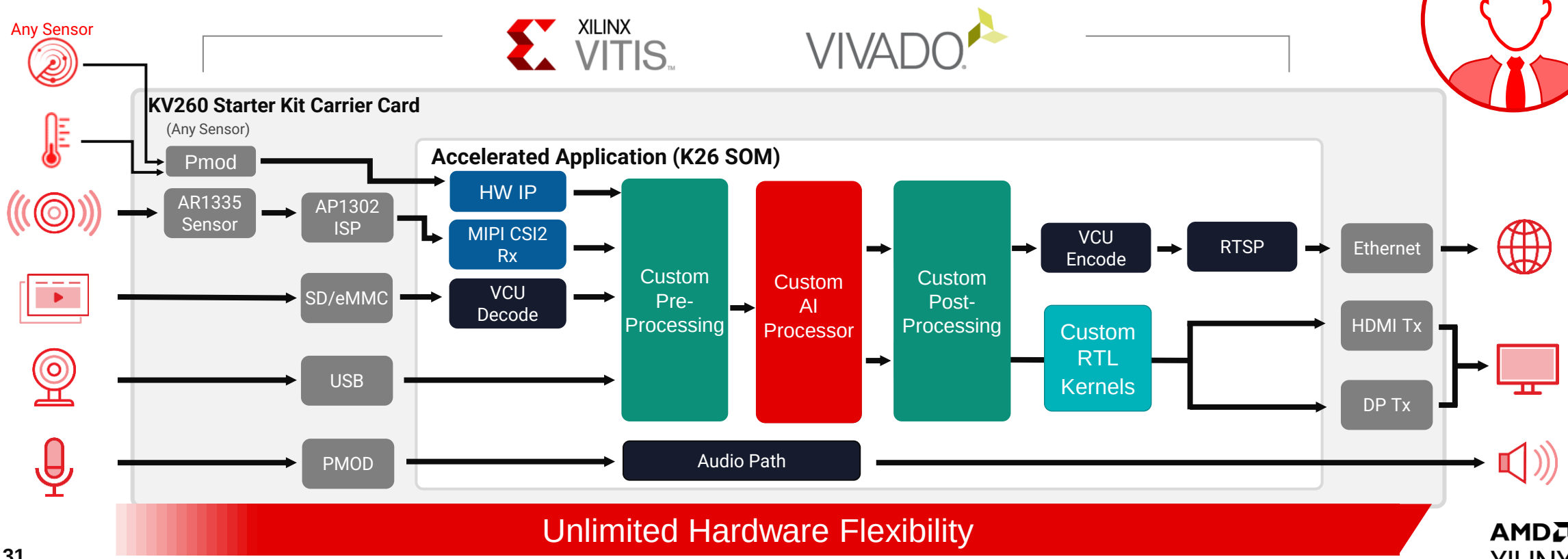
AMD XILINX

# Design with Vivado for Ultimate Hardware Flexibility

## *Extract Even More Performance*

- Leverage Vitis, Vivado®, or both
- RTL design for HW differentiation (e.g., input resolution, optimize for performance)
- Develop custom RTL kernels or AI processor
- Integrate any sensor and customize interfaces

Hardware Developer






AMD XILINX

# Robotics Starter Kit — Kria KR260

XILINX.

# Robotics Starter Kit — Kria KR260

**KR260**

Robotics Starter Kit


**K26**

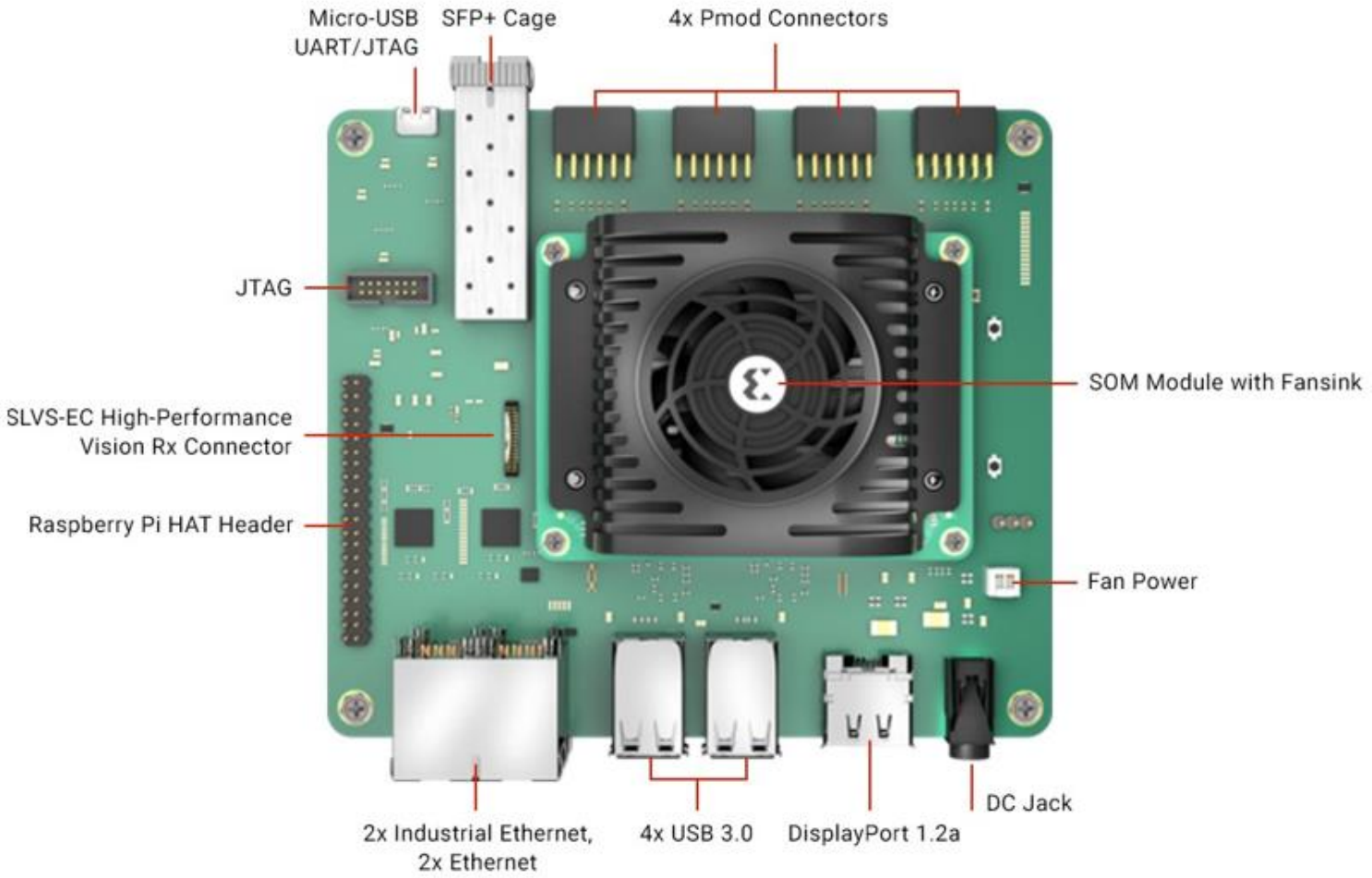
Production SOM Module


DEVELOP ⋯⋯▸ DEPLOY

# Robotics Starter Kit — Kria KR260

## KR260

Robotics Starter Kit

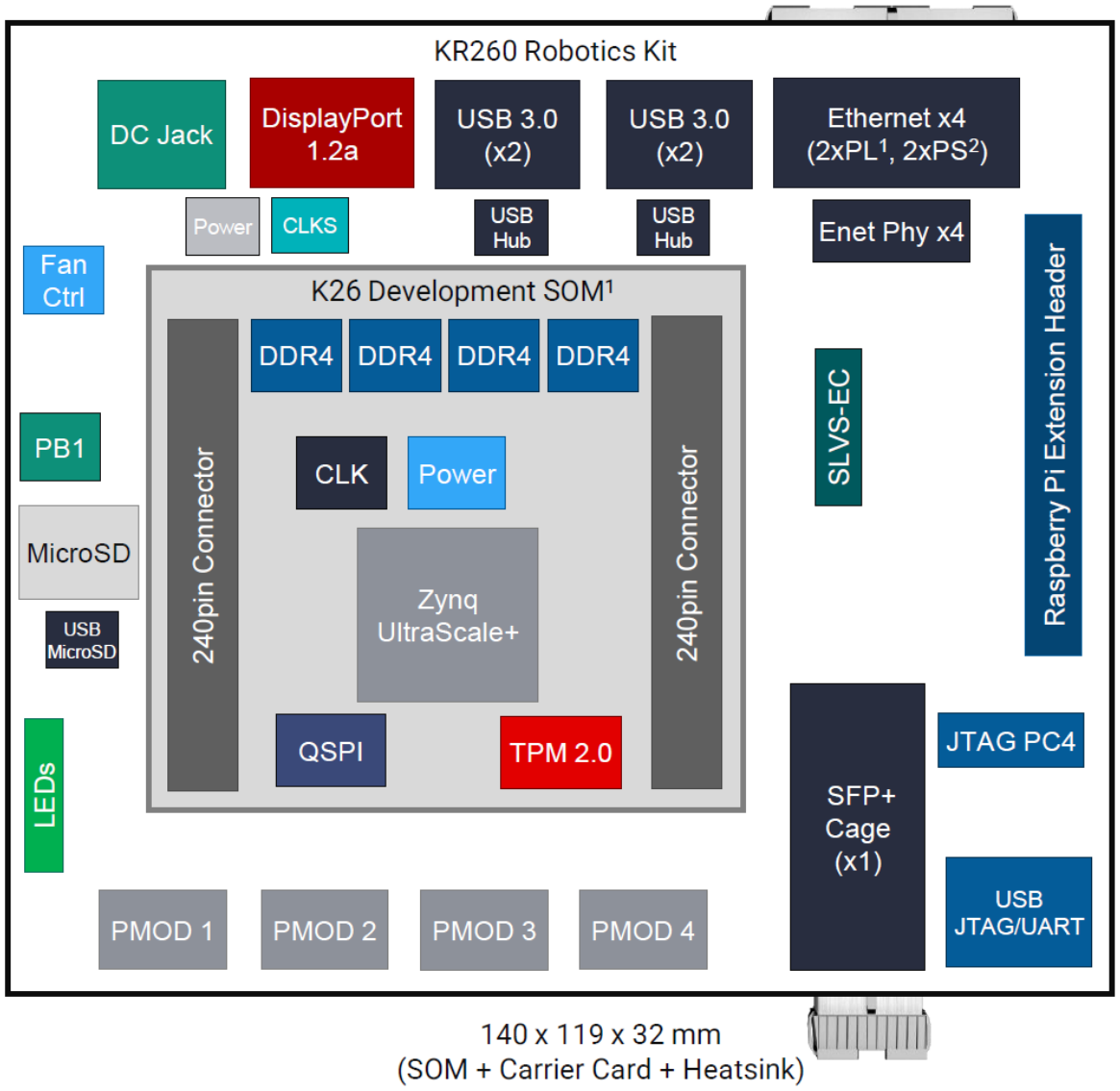
# Robotics Starter Kit Carrier Card Features & Capabilities

## Optimized for Kria K26 SOM
- 2x 240-pin connectors
- All SOM I/O available for sensor & network connectivity

## High Performance Industrial Vision Interfaces
- SLVS-EC Rx
- 3x USB 3.0 for camera interfaces
- DisplayPort 1.2a

## Real-Time Networking Interfaces
- 4x RJ45 Ethernet Ports (10/100/1000)
- 1 SFP+ optics (10G) for 10GE Vision

## Expansion w/PMODs & Raspberry Pi Headers
- Extend to any sensor or interface
- Broad Pmod ecosystem
- e.g., Wi-Fi adapters, RS485



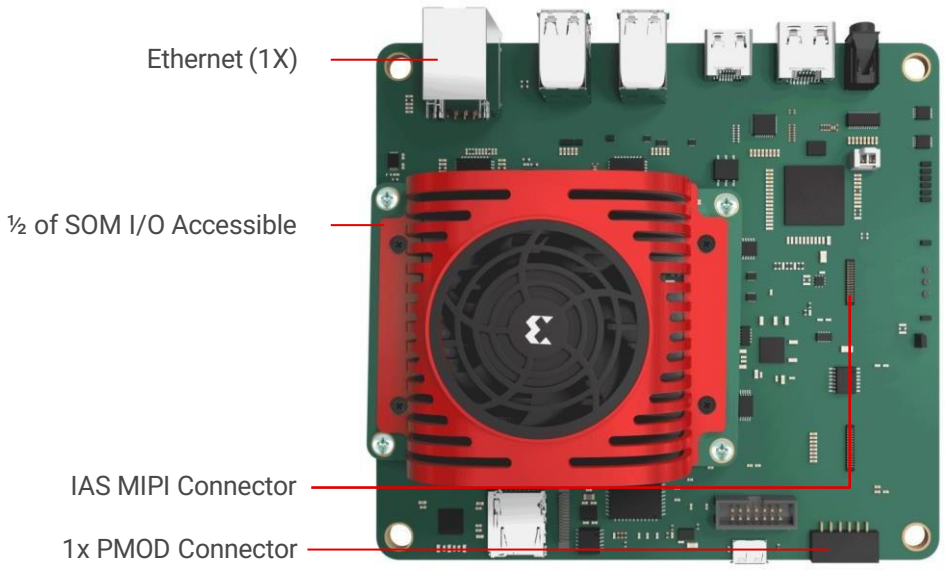

1: Production SOM includes eMMC
2: Zynq SoC Processing Subsystem (PS)
3: Zynq SoC Programmable Logic (PL)



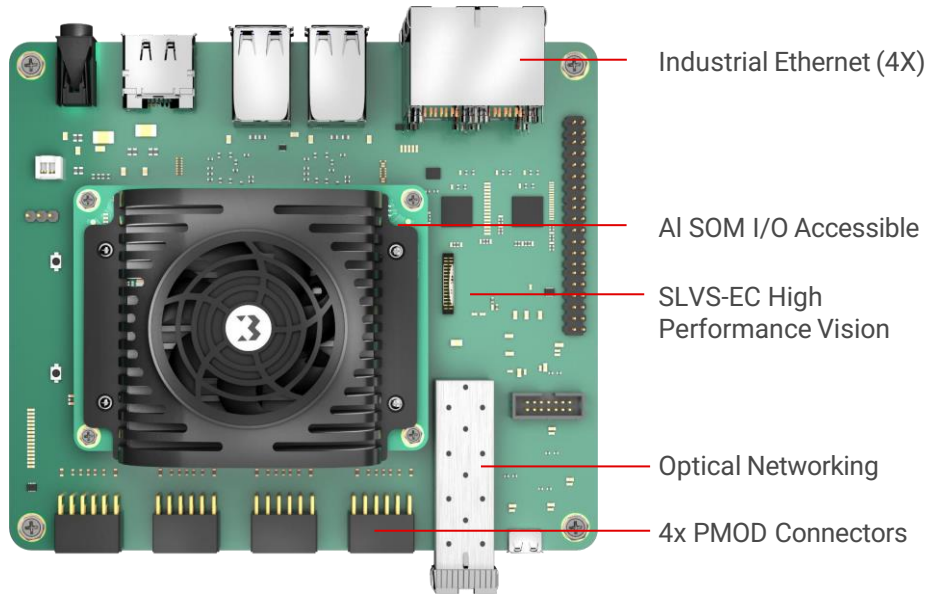
XILINX.

# Comparing Vision AI Starter Kit and Robotics Starter Kit

## For Main-Stream Vision AI Cameras




## For High-Performance Industrial Systems




| | KV260 Vision AI Starter Kit | | KR260 Robotics Starter Kit |
|---|---|---|---|
| **SOM I/O ACCESS** | 1x 240-Pin Connector | 2x SOM I/O | 2x 240-Pin Connector[1] |
| **NETWORK** | 1x Ethernet | 4x Ethernet | 4x Industrial Ethernet, SFP+ |
| **VISION** | MIPI Vision Sensors | SLVS-EC | SLVS-EC Vision Sensors |
| **INTERFACE EXPANSION** | 1X PMOD | 4x PMOD | 4X PMOD |

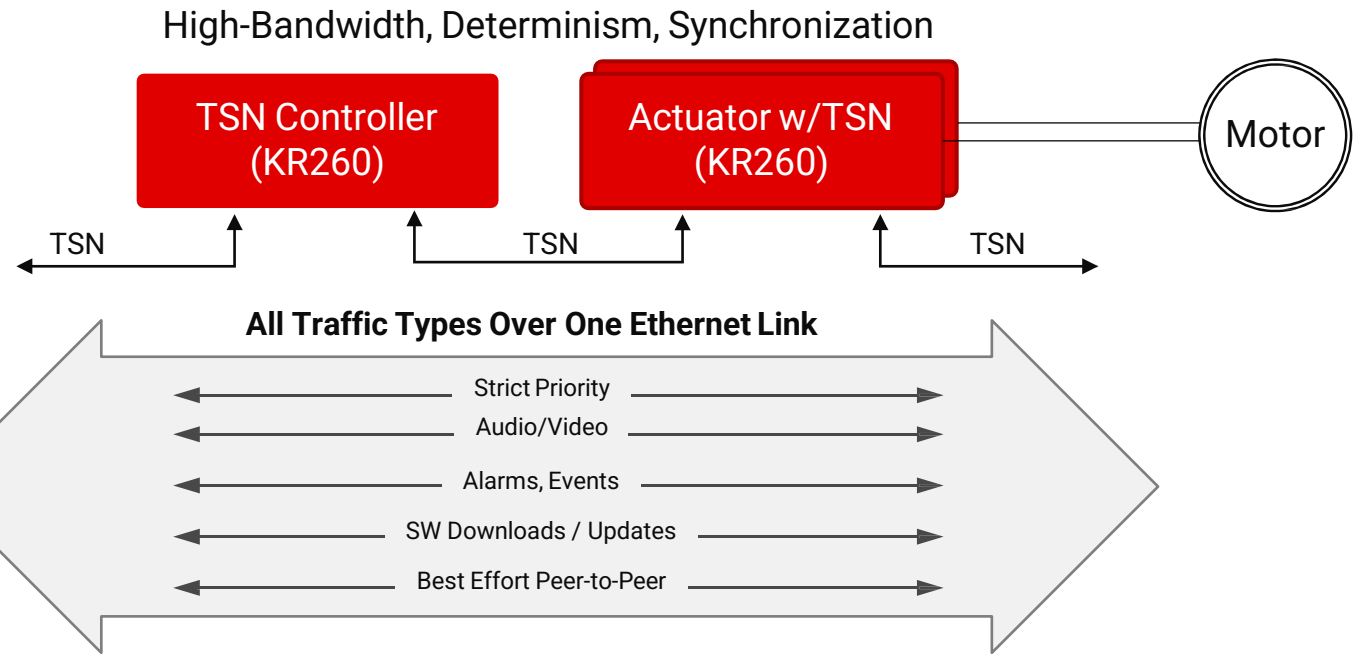
1: All SOM I/O accessible to user, including dedicated board connectors (SFP, Ethernet, VLVS-EC headers) and IO expanders (e.g., PMODs)



XILINX.

# First Mainstream TSN Industrial Communication and Real-time Control Platform

- Two TSN ports for high-bandwidth, deterministic transmission
- IEEE 802.1AS compliant time synchronization (< 20ns) for scheduled traffic
- Built-in ethernet switch eliminates external TSN switch
- All traffic types over a single industrial ethernet link



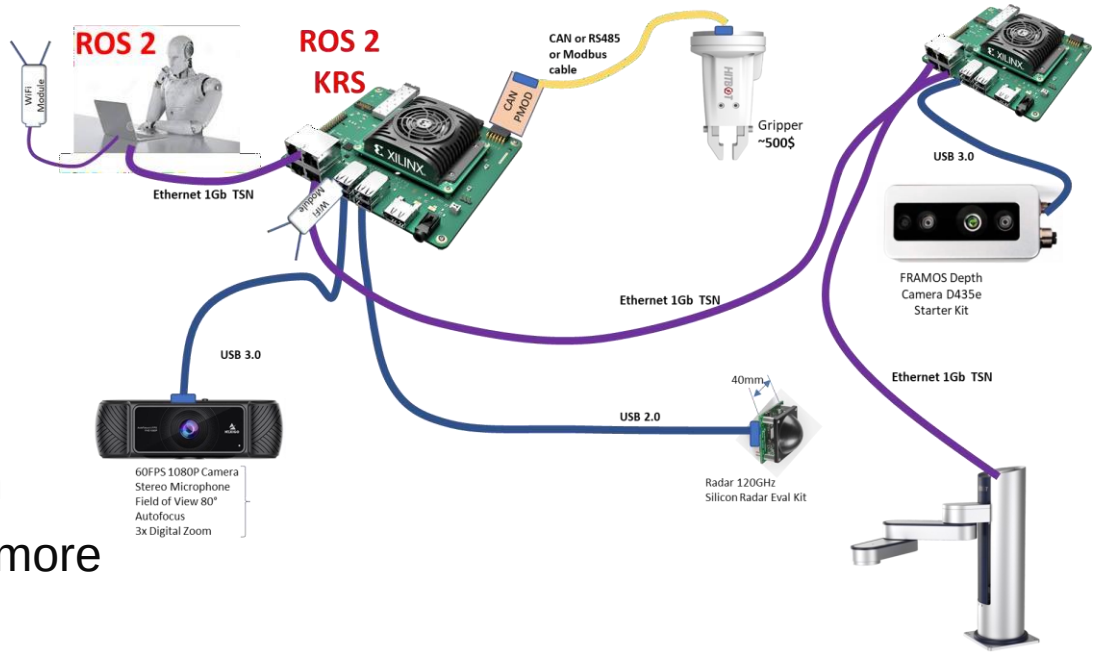



XILINX.

# End-to-End Adaptive Robotics Platform

*TSN, Vision & Sensor Fusion, Actuation, HW Acceleration*

- Intra-network communication
  - Predictable TSN communication for robotics internal network
  - KR260 clustering w/synchronization for multiple controllers
- Perception via vision interface and Pmods
  - e.g., USB Camera, depth sensors, radar, lidar
- Actuation via Pmod/Modbus interfaces
  - Motors, steppers, grippers, manipulators
- Hardware acceleration and offloading
  - Low-latency inter-process, intra-process computation
  - Motional planning, motor control, sensor fusion, and more



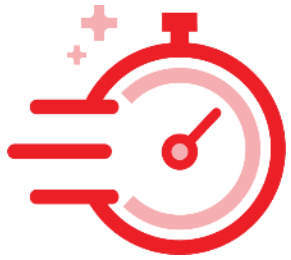

"Instant-On" Robotics Experience



XILINX

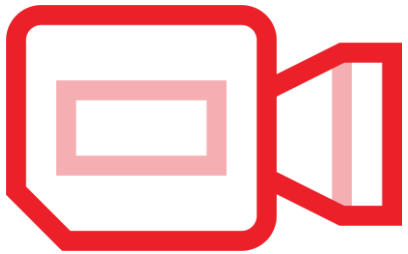
# Accelerated Applications: Pre-Built Solutions Without “FPGA Place-and-Route”

TSN Communications

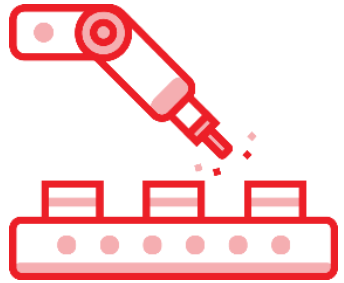


Perception

10GE Vision Camera



Manipulation with TSN[1]



More Applications Coming Soon for Navigation, EtherCAT, and More

1: Contact Xilinx for Early Access

# Xilinx KR260 Robotics Kit Summary

## Native ROS 2 Support

- 5X productivity with Robotics Stack
- C/C++ and RTL flexibility for HW/SW architects

## Complete Industrial Solution

- Pre-built interfaces for robotics and industrial solutions
- Simplified integration, faster time from out-of-box to deployment

## Low-Latency and Determinism

- Real-time response for high performance machines
- Safety & Security for industrial-grade solutions


**Out-of-the-Box Ready for Software and Hardware Developers**

1: Compared to Nvidia CUDA flows; accounts for setting up robotics toolchain with ROS 2, cross-compilation of host code or creation and build of accelerator among other necessary steps.



XILINX

# Design Path for Software and Hardware Developers

TIME

AI Developer

Customize AI Model

- Build custom AI application
- Configure AI processor to your requirements

XILINX VITIS AI

Roboticist

Develops Robot Behavior via KRS

- Based on workspaces (vs. applications)
- Computational graph-centric
- Software-oriented, native support for Kria

ROS 2

Embedded Developer

Customize Vision / Connectivity

- Change pre- and post-processing
- Accelerate entire pipeline in SW
- Customize connectivity in firmware

XILINX VITIS

HW Developer

Full Custom RTL Development

- Ultimate Flexibility (RTL)
- HW Differentiation

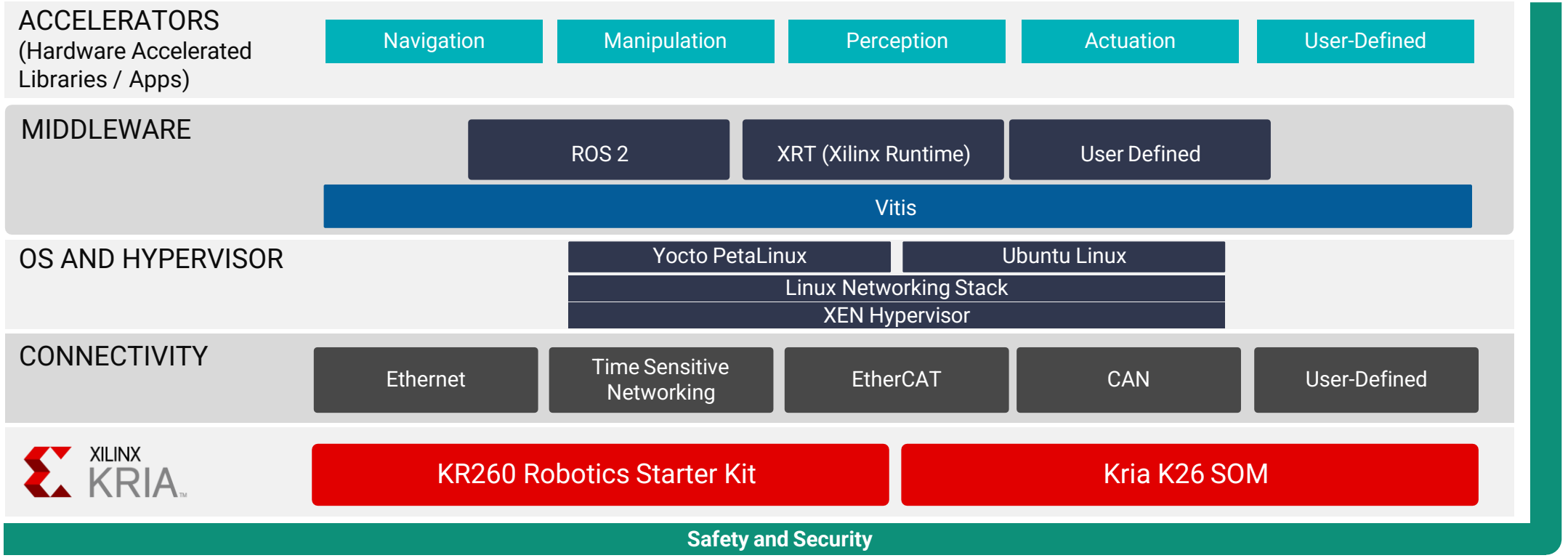
VIVADO



XILINX

# The Kria Robotics Stack for Roboticists

- A familiar entry-point aligned with common robotics flows
- An integrated set of libraries and utilities to accelerate development
- Developed around ROS 2 SDK to enable a SW-defined, HW-accelerated platform

# Detailed Kria Robotics Stack

## ROS 2 Apps and Libraries

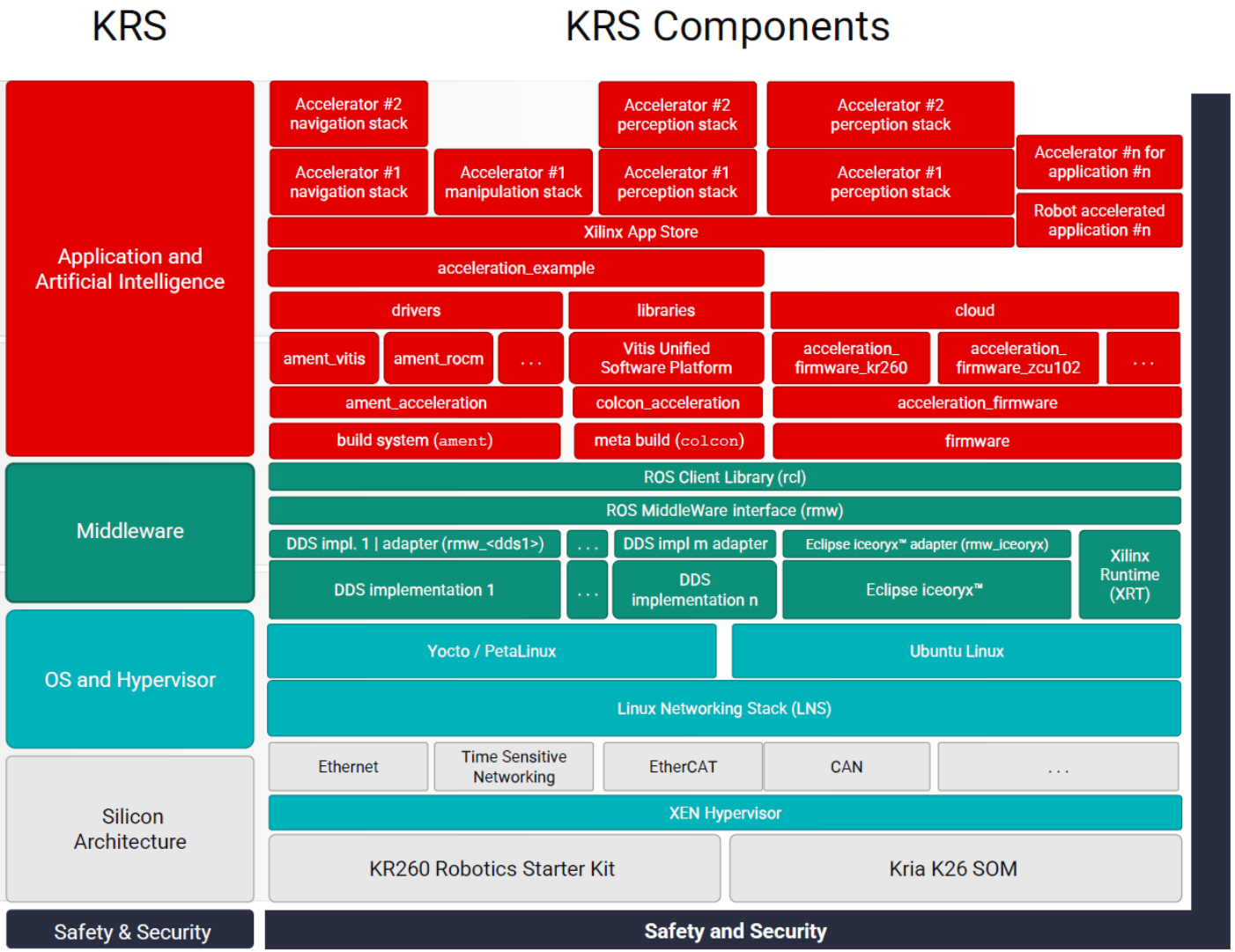
Kernels that speed-up apps and libraries on top of ROS

## ROS 2 Core

Kernels that accelerate or offload ROS 2 core components and tools

## ROS 2 Underlayers

Kernels below the ROS 2 core layers (includes communication middleware)

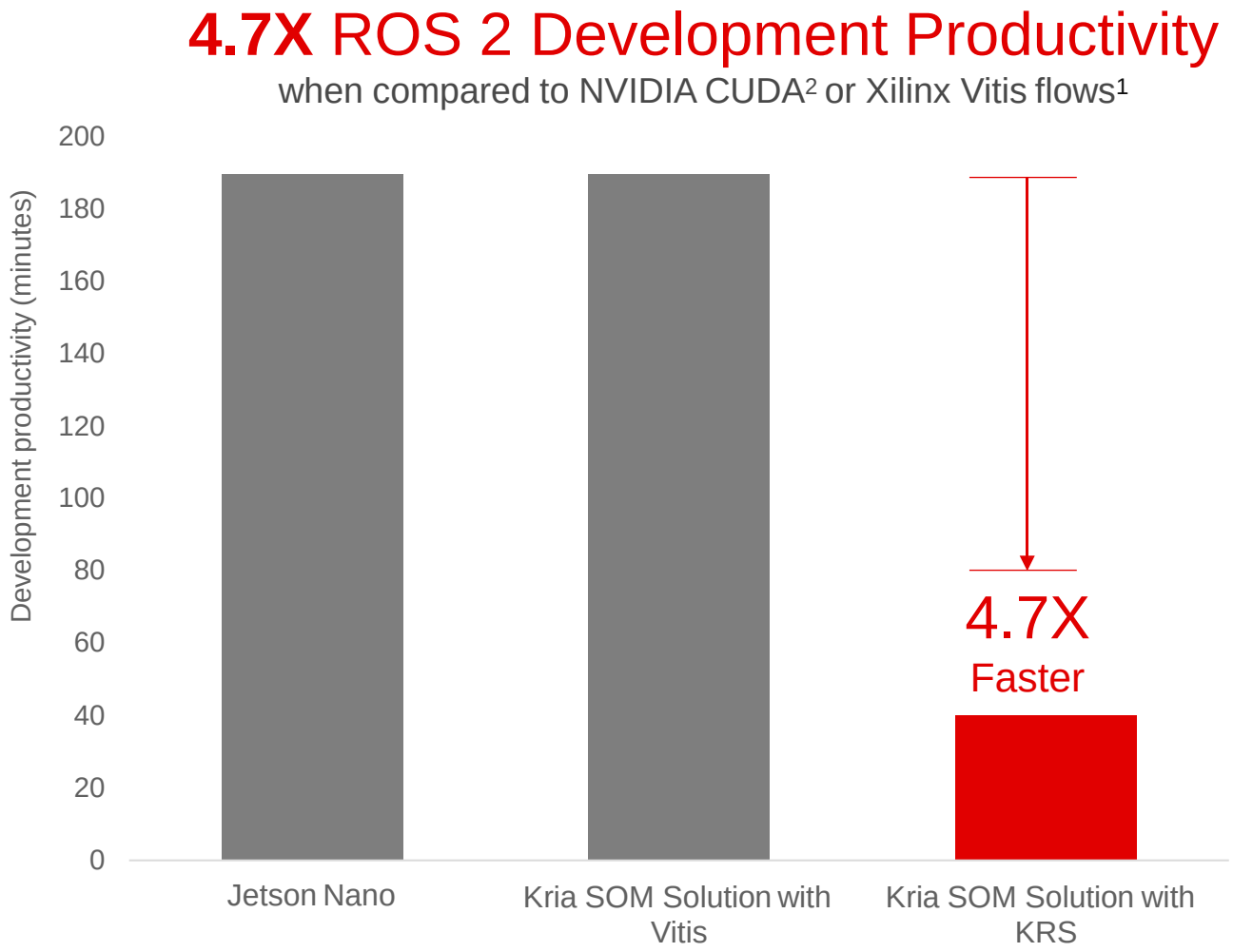





XILINX

# SW-Defined Platform for 4.7X Productivity

- From 3 hours to 40 minutes: 4.7X faster vs. Jetson Nano or native Xilinx Vitis flow
- Development time accounts for
  1. Tool chain setup
  2. Computational graph dev in ROS 2
  3. ROS build system calling Vitis macros
- Vitis tools hidden from roboticists, who can focus on computational graph workspace in ROS 2




1: Evaluated using doublevadd_publisher and accelerated_doublevadd_publisher – https://github.com/ros-acceleration/acceleration_examples

2: Accounts for setting up the toolchain with ROS 2, cross-compilation of host code or creation and build of the accelerator among other necessary steps.



XILINX.

# Thank you very much for your attention!

XILINX.