

Technical Manual

VuePoint II™ Touch Terminal

Manual P/N: 01-010
Revision 0
November 2009



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Preface

This manual provides detailed technical information as well as an overview of the Vuepoint II terminal manufactured by General Digital Corporation.

All schematics and mechanical drawings are included along with operational descriptions of the subcomponents that are contained in the unit.

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The VuePoint II™ Terminal

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The VuePoint II™ is the second generation line of special computer terminals designed for flexible, natural, man-machine interaction. The VuePoint II contains features such as:

1. 40 x 12 Gas Plasma Display with Touch Sensitivity.
2. Compact packaging, versus CRT/Keyboard Terminals.
3. Intelligent Z80A Microprocessor-Based Control with Multiple Display Buffer.

The VuePoint II incorporates a redesign over the original VuePoint™ which allows for smaller packaging, lower power dissipation, increased display buffer storage, and greater flexibility for optional and custom interfaces.

The VuePoint II (VPII) consists of a CPU Board (Z80A) which, under VPII firmware, maintains control of all VPII operations through special plug-on hardware interfaces (see Figure 1).

This hardware includes modules such as the VPII Plasma Controller board, which provides data and control of the Plasma Display, and the VPII Controller Board, which provides an interface to the Touch Scanner, annunciations, and a set of switches for firmware control.

These sub-components are mounted inside a sheet metal enclosure with provisions for mounting power and communications cable assemblies.

If optional or custom interfaces are required, a specific module is simply plugged onto the VPII CPU Board, while a setup menu instructs the VPII firmware as to module operation.

The optional external power supply provides all necessary power for the VuePoint II. Two types of power supplies exist: 1) the VPII power supply that is hardwired for 120 VAC operation; 2) a newer and more flexible version, the VPII Universal power supply, which allows selection of 120 VAC or 240 VAC operation with automatic high voltage selection for VuePoint II's with orange or green display options (250 VDC or 300 VDC).

See Theory of Operation (Section 2) for further details of sub-component operation.

2.0 Theory of Operation

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2.1 Overview

The heart of the VuePoint II is the VPII CPU Board, a Z80A-based single board computer. Under VPII firmware, this controls the various VuePoint II interface modules; processes character, control, and multi-byte command input and output; and handles storage and retrieval of display page information.

On power-up, the VPII Plasma Display Controller is initialized and a memory check is done to determine the number and type of pages installed in the system. If enabled (via Switch-8), the factory setup mode is activated, allowing configuration of the firmware for standard or optional interfaces. These selections are stored in nonvolatile RAM, and are used in generating the menu selections in the VuePoint II setup mode. This setup mode allows setting of VuePoint II characteristics and also configuration of certain Communications and (if installed) Keyboard/Printer interface parameters. These parameters are also saved in non-volatile RAM.

When the setup mode is exited or disabled, the non-volatile parameters are recalled for use in initialization of the existing interface hardware installed in the system. In addition, software flags, buffers, and display page buffers are cleared before the VuePoint II enters normal operating mode .

In normal operation, the VuePoint II firmware periodically checks if data is available in the receive buffer while also checking the Keyboard interface (if installed) for keyboard data. If valid host data is received at the communications port, an interrupt is generated by hardware causing a firmware service routine to place the data into the 256 byte circular receive buffer. When keyboard data is made available, it is placed into the transmit buffer and also the receiver buffer, if "keyboard echo" is enabled.

The VuePoint II firmware then determines if the data byte is a control or character data, or if the data is part of an escape command sequence, and sets an appropriate flag.

These flags are checked by separate routines which process the data or command requests. Command requests normally are used to set or reset control flags, while character data however, is placed into a specific 1K-byte page buffer (Working Page). If a Display Page command is requested, the character and attribute data of the 1K-byte buffer are then used to update the Plasma Display Controller.

When touch is enabled, a touch scanner service routine periodically initiates scanning sequences and checks for available touch data. If valid data exists, the appropriate touch data is placed into the transmit buffer. A routine checks this buffer and transmits available data when the communications hardware is ready.

2.2 VPII CPU Board

2.2.1 Clock and Reset

The VPII CPU board uses an on-board 8 MHz oscillator for a system clock. The 8 MHz is generated by a series of inverters (U23, See Schematic, Section 8.2) and R-C networks with an 8 MHz crystal to stabilize the oscillator frequency. The 8 MHz signal is divided by a series of two D-Flip Flops (U28) providing a 4 MHz clock for the Z80A, and a 2 MHz device clock for the 8251A USART (U18).

On power-up, a reset circuit generates a system reset for both on-board devices and expansion modules. RESET is generated by a one-shot timer (U29), which remains active until the charging R-C network exceeds the input trigger voltage. At this point, RESET is disabled until the next power-on condition occurs. RESET is then inverted and supplied to devices that require RESET/, such as the Z80A and the TMS 4500A dynamic RAM controller.

2.2.2 CPU Bus

The 8 bits of Z80A data bus (D0 -> D7) and specific sections of the address bus (A0 -> A15) are bussed directly to each of the five 28 pin JEDEC memory sockets, the non-volatile RAM area, the 50 pin system bus connector and the 128K dynamic RAM area.

The data bus is then isolated by a bidirectional data buffer (U13) for the I/O data bus (MD0 -> MD7). This data is supplied to each of the expansion module connectors as well as other on-board I/O devices.

Portions of the address bus, however, are made available at the memory decoding area (All -> A15), and are buffered (U19) and connected to various I/O devices and the expansion connectors (MA0 -> MA2).

The remaining CPU signals are used in various areas of the board for control of memory and I/O functions.

2.2.3 Memory Decoding and Devices

Available on the VPII CPU board are five 28-pin sockets for 8-bit JEDEC compatible memory devices. Through jumpers, these can be configured for a variety of different RAM or ROM sizes.

A standard VPII CPU board is supplied with two 8K EPROMS for VPII firmware storage and two 2K static RAMS, which are used by VPII firmware and for the storage of three pages of display information.

Memory decoding for the five 28 pin sockets and the NVRAM is accomplished by the use of a 3-to-8 decoder and two 2-to-4 decoders (U2, U10). The jumper arrays JP3 and JP4 allow the CPU address lines All through A15 and the MREQ/ signal to be available for connection to the various address and enable inputs of the three decoders, while also allowing access to the decoding outputs and the chip select input for the available memory devices.

By configuration of the memory decoding jumpers, the VPII CPU board is setup for EPROM access at locations 0000H and 2000H in the memory address space. RAM access is decoded further which places the two RAMS at location 8000H and 8800H, respectively. The first 1K of this RAM is reserved for VPII firmware variables while the remaining storage area is used for page data.

This configuration allows for both custom firmware expansion (up to 32K) and optional display page expansion of up to 15 pages of "Type A" memory. The last 16K of address space is reserved for bank selecting 16 page sections of optional "Type B" display page expansion memory (0 to 128 pages).

2.2.4

Non-Volatile RAM

The VPII CPU board provides an area for a non-volatile RAM (NVRAM) for permanent storage of data. The board is set up to allow flexibility in selecting 4- or 8-bit devices for use.

The VPII CPU board uses a 256 x 4 NVRAM which is used by VPII firmware for storage and retrieval of various parameters (setup mode). The NVRAM, when activated, is located at address 6000H in the memory area. To avoid interference between the NVRAM and possible expansion firmware, decoding for the NVRAM chip select signal is enabled and disabled by a bit from the chip select/address control latch. Selecting I/O port C1H enables the chip select, while I/O port C0H disables the NVRAM chip select.

The NVRAM also requires STORE/ and RECALL/ signals. These are created by selecting I/O ports D0H and E0H, respectively.

2.2.5

I/O Decoding

The CPU board produces 16 I/O port select signals by using the 3-to-8 decoders (U15, U16), and the top 4 bits of the I/O port address (A4 -> A7). This generates an active low select signal spaced every 10 hex starting at port addresses 00H. These 16 selects can be jumpers to the twelve available expansion module select signals, two for each of the six module locations (MCS0/, MCS1/). Also available are inputs for the NVRAM control signals, the address/chip select latch, and the on-board serial port. The jumper header (JP11) is used to permit flexibility in hardware configurations by eliminating the need for firmware changes.

2.2.6

Serial Interface

The VPII CPU board has an on-board RS-232C serial interface which is used for communication in a standard VPII configuration. The serial interface uses an 8251A USART and RS-232C driver and receiver IC's. The signals are available at a configuration jumper header which passes them to a 26 pin connector mounted on the CPU board.

The data and control ports of the USART are accessed using I/O ports F0H and F1H, respectively. The on-board serial interface allows a choice of either hardwired or programmable baud rates. In a standard VPII configuration baud rates are determined by the CPU by controlling three bits in the baud rate select latch (port address F2H). This is used to

multiplex one of the eight available baud rates into the clock inputs of the USART.

The four USART signals RxRDY, TxRDY, TxEMPTY, and SYNDET are available at JP12 for use in generating CPU interrupts. Up to three of these signals may be jumpered to produce an interrupt request (INT/). Since the VPII uses CPU interrupts for inputs of data, only the RxRDY signal is setup to request interrupts.

Baud rates are generated by first dividing the 8 MHz system clock by 13 (U24), which results in a X16 baud rate of 19,200. This clock is then divided progressively by two (U31). Each stage produces the next lower baud rate, the lowest being 300 baud. These seven baud rates are available on the B row of JP15, along with external RS-232C input and output clock connections.

2.2.7

Expansion Module Connectors

The six available expansion connectors are used to add additional hardware functions to the CPU board. The connectors are positioned on the board to allow access to module connections from the perimeter of the board.

In all VPII configurations, three of the module areas are used for the VPII Plasma Display Controller and the VPII Controller. The double-width Plasma Display Controller module, is located at module position GDX0. Its control registers are selected and accessed through I/O ports 00H and 01H, while Display and Attribute data are latched by a data output to ports 10H and 11H. Module position GDX1 is not used, but is covered by the VPII Plasma Display Controller module.

The VPII Controller module, located at module position GDX2, is accessed via I/O port 40H for Touch Scanner Status and Control, while Switch Status is read through I/O port 50H.

The remaining three multi-module locations (GDX3, GDX4, and GDX5) are available for VPII options such as Extended Serial Communications (GDX3), Parallel Communications (GDX3), and Keyboard/Printer Interface (GDX5) for example. They also can be used for meeting custom communications requirements or other custom applications needs.

All interfacing to the expansion modules is accomplished through the I/O structure of the CPU board. At each 36 pin connector, GDX0 -> GDX5, the CPU board provides the 8-bit I/O data bus on pins 21 through 33 (odd). The bus is buffered from the CPU and is enabled when the CPU selects an I/O request (IOREQ/).

Besides the I/O module select signals (MCS0 and MCS1), the expansion module requires read and write signals for data control, MIORD/ and MIOWT/, and three address signals for additional port decoding, MA0 -> MA2. These are generated by buffering the existing Z80A read, write, and address lines and bussing them to the appropriate pins.

Two additional buffered signals provided at each connector are the system reset (RESET) and the 8 MHz system clock. An 8-bit TTL bus driver (U19) is used to buffer these seven signals. This is required in order to supply enough current capability if maximum loading occurred at all six expansion module sockets.

For CPU control, each expansion module has two interrupt inputs for generating interrupt requests, MINTR0/ and MINTR1/, and a wait input (MWAIT/) for instructing

the CPU to increase the time duration of the CPU signals. This is available for modules that require additional time for data setup.

The module interrupt requests are linked to the CPU by a series of open collector inverters (U20, U21). The two active high interrupt signals from each connector are inverted and made available at the jumper array JP13. The jumper array allows any one of the twelve open-collector outputs to be jumpered to the pulled-up INT/ input of the Z80A.

Each of six MWAIT/ signals are pulled-up and combined by a series of AND gates along with an external WAIT/ input, which is available at JP16 and the 50 pin system bus connector. The resulting active low output is connected to the WAIT/ input of the Z80A. JP16 permits use of self-refreshing memory devices that require additional setup time and provide a READY signal (12186). The memory device setup jumpers at each socket (JP5 -> JP9) allows access to this signal.

2.2.8

128/512K Dynamic RAM Area

When large amounts of memory are required, such as "TYPE B" memory option, the CPU board has an area dedicated for up to 128K bytes of dynamic RAM. If 16K x 4 devices are used (4416's), or 512K of dynamic RAM if 64K x 4 devices are used (4464's). Storage is divided into banks of 16K each. VPII firmware stores 16 pages of data into the one through eight on one through thirty-two available banks, providing up to 128 or 512 pages of display storage. Banked pages are accessed in the 16K memory area, C000H through FFFFH. Selection of banks is controlled by five bits from the baud rate select latch. These control bits, along with the two CPU address signals A14 and A15, and the row address control from the 4500A DRAM controller, are used by a 512 x 8 BIPOLEAR PROM to select the appropriate bank of dynamic RAM.

The 4500A DRAM controller is used to control row and column addressings during memory access (RAS1/) as well as to provide refresh addresses to all devices (RAS0/) when the Z80A enables the RFSH/ signal. The 4500A will also generate refresh automatically if RFSH/ does not occur in time.

2.2.9

Power

DC power is supplied to the VPII CPU board through the main power connector J1. The VPII CPU board requires +5VDC @ 2.5A (w/VPII modules, Plasma Display, Touch Scanner, optional modules and optional memory installed) and ±12VDC @ ±50mA. The ±12VDC requirement can be eliminated if the VPII is in a non RS-232C configuration or via an optional on-board DC-DC Converter which supplies ±12VDC from +5VDC.

2.3

VuePoint II Plasma Controller Module

The VPII plasma controller interfaces the CPU board with the 12 x 40 gas plasma display in the VPII. The Plasma Controller provides the necessary voltage, timing, and data signals required by the plasma display. It also has high voltage protection circuitry to prevent damage to the Plasma Display if a failure occurs in the CPU or Plasma Controller operation.

The VPII Plasma Controller module can be divided into six major functions:

- 1) CRT Controller
- 2) Refresh Memory and Character Generation
- 3) Refresh Memory Updating
- 4) Display Data
- 5) Display Timing
- 6) High Voltage Protect

2.3. 1

CRT Controller

The 6845EA CRT Controller (U17, See Schematic, Section 3.2) provides refresh memory addresses, triggering of timing signals, and control and status of memory updating.

Before data can be displayed, the CPU must initialize the 17 internal timing registers of the CRT Controller. The CPU first selects a register by writing to the register select port with a register address as data. Then a timing value is written to the register data port.

THE CRT CONTROLLER REGISTER SETUP

The following table shows the Register setup parameters and their function:

<u>REGISTER #</u>	<u>VALUE</u>	
00H	0EH	15 horizontal characters total
01H	0CH	12 horizontal characters displayed
02H	0DH	Horizontal Sync. Pos. (Phase clk)
03H	31H	Vertical and Horizontal Sync. pulse width
04H	27H	40 vertical characters total
05H	03H	Vertical adjustment
06H	28H	40 vertical I/O characters displayed
07H	27H	Vertical Sync. Pos. (reset)
08H	4CH	Row column add., transparent memory updating
09H	05H	6 horizontal lines per character
0AH	00H	Cursor start

continued on next page

0BH	20H	Cursor end, no cursor
0CH	00H	Starting display RAM add. high
0DH	000H	Starting display RAM add. low
0EH	00H	Cursor add. high
0FH	00H	Cursor add. low
1FH	XX	Initialize transparent updating mode

NOTE: Serial data is loaded into the Plasma Display in a top to bottom, left to right format, while the CRT Controller chip uses a system rotated by 90 degrees. Thus, “horizontal” refers to the top to bottom scanning while “vertical” refers to left to right scanning.

These timing values refer to the number of clock cycles the CRT Controller receives at the CCLK input. Using this data, the CRT Controller generates row memory addresses (MA0->MA3), column memory addresses (MA8->MAD), individual character column addresses (RA0->RA2), horizontal and vertical timing pulses, and control of memory updating (RA4) during non-display periods.

The 6845EA CRT Controller requires an ENABLE signal (active high) when the device is accessed for a read or write operation. Since no phase-2 CPU clock is available (as in 6800 uP series), the ENABLE signal is triggered by the controller chip select and CPU clock (4 MHz).

2.3.2 Refresh Memory and Character Generation

The Plasma Display Controller uses three 2114 1K x 4 static RAMS for display refresh memory (U1,U4,U10). U4 and U10 are used for storage of 8-bit character codes while U1 is used to store display attributes such as cursor, blink rate and intensities for each character. The ten refresh address signals are supplied by the CRT Controller.

The 8-bit character data from the refresh memories (U4 and U10), along with the character column address (RA0-> RA2) from the CRT Controller, are used to address the 2K x 8 character generator EPROM (U18). This generates the 5x7-bit dot pattern for the actual display data.

This data is then loaded into a shift register (U12) while the 4-bit attribute data is loaded into a holding register (U6). The 7-bit display data is shifted out forming the signal SROUT, while the four attribute control signals (L-INT, CURSOR, BLINK-1, BLINK-2) remain constant until the start of the next character time (CCLK).

2.3.3 Refresh Memory Updating

To alter character data in the refresh memory, the CPU first reads the status port of the CRT Controller. The update bit (bit-7) of the status register indicates whether a previously requested memory update has occurred (high) or not (low).

Once the update has occurred, new character and attribute data are loaded into holding registers (U11 and U5) by writing to the Character data and Attribute data ports. The

row and column location of the new character is then loaded into internal registers 13H and 12H, respectively. An update request is then made by selecting internal register 1FH. At this point the CRT Controller resets the update bit of the status register and waits for a non-display period to update the refresh memory.

The register parameters have been chosen such that a non-display period occurs at the end of each top to bottom scan of the display for three character times (CCLK).

At this point, the CRT Controller initiates an update cycle by placing the row/column update address on the refresh address lines, followed by an UPDATE strobe from the RA4 output. This signal is used to load the holding register data in the refresh memories.

2.3.4 Display Data

The display data is formed by the combination of serial character code data (SROUT) and the character attribute signals which include blink rate, intensity, and cursor control.

The attribute signals BLINK-1 and BLINK-2 are used to control the 4:1 multiplexer (U7), selecting the current blink rate. If both signals are low, a constant high level signal is multiplexed producing a non-blinking character. Activating one of the control inputs, BLINK-1 or BLINK-2, selects one of the respective blink rate oscillators, OSC-1 (slow, 1.5 Hz) or OSC-2 (fast, 7.0 Hz). If both inputs are active, a low level output is produced, disabling the character ("invisible" blink rate).

L-INT causes the character to be displayed on alternate display refresh periods, producing a low intensity.

The cursor control is formed by combining the control signal (CURSOR) with the fast blink rate oscillator (OSC-2) and the low intensity timing signal (U14). The result is a fast blinking cursor which illuminates all dots of the specific character. The low intensity signal is used to synchronize the cursor, if a low intensity character is present.

2.3.5 Display Timing

Plasma Display timing is based on synchronizing the CRT Controller signals, the two clocks (CCLK and DATA CLK), and the serial display data.

DATA SHIFT is used to clock the serial display data into the display. The rising edge of DATA SHIFT latches the current logic level at the SRDATA/ input. As each DATA SHIFT occurs, the following (lower) dot becomes the target for the next data input. This process occurs until data for the last dot (bottom) in the dot column has been latched (84 dots per column). HORZ is used to disable the DATA SHIFT after data for a full dot column has been entered and the next dot column (right) is being selected.

PHASE CLK/ instructs the display to begin entering data into the top of the next column (right). PHASE CLK/ is based on the HORZ timing signal from the CRT Controller. After a dot column has been filled with data (twelve character times) and two non-display character times have passed, the CRT Controller outputs an active high HORZ signal for one character time. This is used to initiate PHASE CLK/.

The RESET/ signal is used to reset data entry to the top of first dot column. This is

required after a complete scan (240 dot columns) of the display. To meet the display requirements, the CRT Controller is setup to generate a VERT signal three horizontal periods in duration. However, the display requires that the RESET/ begins within 100ns of start of PHASE CLK/. Since the CRT Controller cannot position the two signals (HORZ, VERT) simultaneously, the CRT Controller is setup to begin the VERT signal at the first dot column of the last character (40). The VERT signal is then delayed six dot columns using PHASE CLK.

2.3.6 High Voltage Protect

The High Voltage Protect Circuit uses a high voltage, low resistance n-channel MOSFET (Q2) to switch the high voltage (+250VDC). The MOSFET is driven by a photo-voltaic diode (U2), which provides an eight volt output when current is flowing through the input LED (U2).

The HORZ signal from the CRT Controller and a transistor Q1 are used to provide a current pulse through the LED at 60 us intervals. The MOSFET remains conducting due to the internal gate-to-source capacitance. If horizontal signal is disabled or if power is removed (+5VDC), a shunting resistor (R2) discharges the gate-to-source voltage, disabling the MOSFET and removing the high voltage from the Plasma Display.

PORT SUMMARY

The following table is a port summary of the VPII Plasma Controller Module:

<u>Port</u>	<u>MCS0/</u>	<u>MCS1/</u>	<u>MIOWT/</u>	<u>MIORD/</u>	<u>MAO</u>
CRTC REGISTER SELECT	L	H	L	H	L
CRTC REGISTER DATA	L	H	L	H	H
CRTC STATUS	L	H	H	L	L
CHARACTER DATA	H	L	L	H	L
ATTRIBUTE DATA	H	L	L	H	H

NOTE: Signal names refer to module control signals

2.4

VuePoint II Controller Module

The VPII controller module provides an interface between VPII CPU board and the touch scanner, self-test/setup mode option switch, the audible bell, and optional touch enable light.

The touch scanner is controlled by three signals, TPENBL, RESUME/, and XYSEL; while scanner status and data is determined by EOF, SCAN, XLATCH, YLATCH, and TDATA0 through TDATA4.

TPENBL (Touch Panel Enable) is activated by a write operation to the Touch Scanner Control port. This creates a RESUME/ pulse which instructs the touch scanner to begin a scanning sequence while also presetting a D-Flip Flop (U2, See Schematic, Section 3.3), thus enabling the touch scanner.

The EOF (End of Frame) signal from the touch scanner clears the D-Flip Flop (U2) resetting the TPENBL signal, while activating the status signal SCAN. The CPU uses this to determine if the touch scanner has completed a scan of the touch sensitive areas. This is done by reading the Touch Scanner Status port.

The XLATCH/YLATCH touch scanner status signals indicate if an X and/or Y touch location has been detected and latched. The X or Y touch location is represented by 5 bits of binary data, TDATA0 through TDATA4 (MD0 -> MD4).

The XYSEL (X and Y select) control signal instructs the touch scanner to place either X touch data (XYSEL-H) or Y touch data (XYSEL-L) onto the TDATA signal lines. Control of XYSEL is achieved through the clear and preset operation of D-Flip Flop, U4.

The Self-test/Setup mode option switch is used as a method of directly interfacing with the CPU, instructing it to enter setup modes or execute selected diagnostic tests. A closed (on) switch creates a low data bit while an open (off) switch sets the data to a high state. A jumper (JP2) is placed in line with switch 8, allowing a hardware disable of the switch. Switch data is determined by a read operation from the Switch Status port.

The audible bell is controlled by a one-shot timer (U1) and a current limiting resistor (R2, variable), providing an adjustable level control. The CPU enables the bell by writing to the Touch Scanner Control port, triggering the one-shot, which then produces a 110 msec pulse for the bell.

The 3 pin connector, J2, allows access to a Touch-Light signal which is activated when touch is enabled by the host system. This can be used to drive or enable an optional lamp indicating that touch is enabled. Transistor pads (Q1) are available for a MOSFET, when switching of NON-TTL signals is required.

PORT SUMMARY

The following table is a port summary of VPII Controller Module:

<u>DATA</u>	<u>SCANNER CONTROL*</u>	<u>SCANNER STATUS</u>	<u>SWITCH STATUS</u>
MD7	—	SCAN	SWITCH 8
MD6	—	YLATCH	SWITCH 7
MD5	BELL	XLATCH	SWITCH 6
MD4	TPENBL	TDATA4	SWITCH 5
MD3	TCHLITE-OFF	TDATA3	SWITCH 4
MD2	TCHLITE-ON	TDATA2	SWITCH 3
MD1	XYSEL-L (Y DATA)	TDATA1	SWITCH 2
MD0	XYSEL-H (X DATA)	TDATA0	SWITCH 1

* Signals are active high.

<u>PORT</u>	<u>MCS0/</u>	<u>MCS1/</u>	<u>MIOWT/</u>	<u>MIORD/</u>
SCANNER CONTROL	L	H	L	H
SCANNER STATUS	L	H	H	L
SWITCH STATUS	H	L	H	L

NOTE: Signal names refer to module control signals.

2.5

Plasma Display

The display used in VPII is a highly reliable, DC gas plasma unit which provides 12 lines of 40 characters each using a 5 x 7 dot matrix array to generate characters. There are fixed gaps both horizontally and vertically separating individual characters. The display provides large and bright patterns which are viewable over a range of 120 degrees horizontally and vertically. Character size is 0.14" W x 0.26" H. Active screen size is 8.3" W x 4.6" H. Overall panel size is 11.0" W x 6.1" H x 1.4" D.

The Plasma Display mounts to a support panel inside the VPII. Signals and power for the display come through a cutout in the display mounting panel via a 20 conductor flat ribbon and 3 conductor high voltage cables. These connect directly to J3 and J2 of the VPII Plasma Controller Module.

The display requires +5VDC (@ 500 mA max) for logic and +250VDC (@ 90 mA max) for the display elements.

The display panel internally controls all high voltage switching and dot column addressing. Externally, the following signals are required:

DISPLAY SIGNAL CONNECTOR (J1)

A1	RESET/	B1	RESET COM
A2	PHASE CLK/	B2	PHASE CLK COM
A3	SERIAL DATA/	B3	SERIAL DATA COM
A4	DATA SHIFT	B4	DATA SHIFT COM
A5	ALL DOTS/	B5	SCAN MON.
A6	GND	B6	GND
A7	N/C	B7	BLANKING/
A8	+5VDC	B8	+5VDC
A9	BRIGHTNESS (opt.)	B9	BRIGHTNESS (opt.)
A10	N/C	B10	N/C

DISPLAY HIGH VOLTAGE CONNECTOR (J2)

- 1 GND
- 2 +250 VDC
- 3 GND

The display is refreshed approximately 63 frames per second with a dot refresh rate of 1.60 MHz. In the list above, SERIAL DATA/ is a stream of bit data for each dot column (*NOTE:* Vertical scanning is used). Eighty-four bits of data (7-bit/char. x 12 char. + 3 non char.) are strobed via DATA SHIFT at a rate of 1.60 MHz. The PHASE CLK/ pulse is issued (250 nsec duration each 67 usec) to latch the data and advance to the next dot column. This process is repeated 240 times to scan all columns of the display. Although only 5 dot columns are viewable per character column, 6 dot columns are scanned. After a frame has been scanned, RESET/ is activated for 3 column scan times to reset to the beginning of the next frame.

All of the required signals are generated by the VPII Plasma Controller Board in the VPII. See Section 2.3.

2.6

Touch Scanner

The touch panel provides the novel means for operator interaction in the VuePoint. It uses an infrared scanning principle patented by the University of Illinois. The scanner is a PC board containing 32 LED IR emitters and 32 IR photo detectors (12 rows and 20 columns), associated scanning circuitry and a large cutout in the middle for the display. The touch scanner mounts on standoffs such that the IR light beams pass just over the face of the display. See Schematic, Section 3.4.

Connections to the touch panel are made via a flat ribbon cable and header at the bottom left corner of the touch scanner assembly to J3 of the VPII Controller module. The signals are as follows:

TOUCH SCANNER CONNECTOR

1	+5V	11	GND
2	N/C (Key)	12	DATA-3
3	+5V	13	GND
4	EOF	14	TP ENABLE
5	+5V	15	GND
6	XYSEL	16	DATA-0 (LSB)
7	GND	17	Y-LATCH
8	DATA-4 (MSB)	18	DATA-1
9	GND	19	X-LATCH
10	DATA-2	20	RESUME/

Power requirements are +5V at 700mA max. The panel operates in the following manner: Whenever TP ENABLE is active (high) counters, decoders and LED drivers scan all horizontal and vertical emitter-detector pairs. This is accomplished by energizing one emitter and monitoring its corresponding detector at each count, then proceeding to the next pair. Provided the optical path between an emitter and its detector is not blocked, no action is taken and the scanning continues. However, if the path is blocked (beam is "broken" by presence of a finger) the current count is latched and either the X-LATCH or Y-LATCH flag is set depending on which axis is currently being scanned.

When points on each axis have been scanned successively (in the above manner) the EOF (end of frame) signal is asserted (high).

This EOF signal is fed to the VuePoint II Controller Board. This board sets a flag requesting CPU action and stops the scanning by lowering TP ENABLE. The processor services the request by checking for X-LATCH and Y-LATCH both set (ensuring that beams on each axis are broken), reading the X and Y data (via a multiplexed data bus and the XYSEL control signal) and re-asserting TP ENABLE (if required). Since touch sensors are located only at every other horizontal position, VuePoint firmware multiplies the readings obtained from the hardware by two, before returning coordinate data to the

host. Note that the CPU asserts TP ENABLE only when it is instructed to “enable touch” by the host processor. If touch is not enabled the touch panel performs no function.

Through firmware on the CPU board the touch panel may operate in either “keyboard” or “push-button” mode. In “keyboard” mode the user is required to remove his finger before another entry may be made. This is accomplished by checking for X-LATCH and Y-LATCH both reset (no broken beams) at EOF. Once this occurs, the next pair of broken beams is considered a new entry. In “push-button” mode, finger removal is not required. Whenever an “enable touch” is commanded by the host, the touch panel commences scanning until a pair of beams are found to be broken.

2.7

Communication Options

To support additional communication modes, the VuePoint II is setup to allow expansion modules to be plugged onto the GDX-3 location (lower left) of the VPII CPU Board. By selecting a specific communication option in Factory Setup mode, VuePoint II Firmware executes the appropriate initialization and communication routines for the additional module. The VPII CPU board is also configured to accept interrupt requests from the module.

2.7.1

Extended Serial Option

The Extended Serial Option is based on the GDX-SERIAL-1E expansion module, which supports RS-232C, RS-422A, and 20mA Loop communications. The GDX-SERIAL-1E module uses a Western Digital 8250 Asynchronous Communications Element (U7, See Schematic, Section 3) to provide all Serial Data Conversion and interfacing to the VPII CPU module expansion bus. The Communications Element has ten internal registers for Data, Status, and Control of the Device.

The Baud rate timing is provided by the use of a 1.8432 MHz crystal. During VPII initialization the Baud Rate Registers are loaded with a divisor to obtain the selected X16 Baud Clock. Also, the serial parameters are initialized including received data interrupts. Depending upon the mode required (See VPII Installation Manual) jumper pins, JP1 through J10, are setup to connect the appropriate data and control signals to the 26 pin right angle header (J1).

For RS-422A the four channel driver package (U3) provides the differential output signals while receive signals are converted by a four channel receiver, U4. If RS-232C is selected, the non-inverting differential inputs of I.C. U4 are connected to ground for receiving, while the dual drivers U5 and U6 provide output. A wirewrap from OUT2 (JP12/7) to the RI input (JP12/3) of the 8250 instructs the VPII firmware to enable DSR (DM) handshaking.

When 20mA loop is required, JP1 and JP2 allow either current source to be connected in series (active) with the loop or, for total isolation, permits an external current source (passive) to be used. Both transmit and receive loops can be configured separately. Current-to-voltage conversion and isolation is achieved in both the transmit and receive data paths by the use of Opto-Isolators (U2, U6) and resistor dividers. Since no provisions are made for hardware handshaking, DSR is disabled by connecting the RI input to RTS output (JP13/1).

PORT SUMMARY

The following table is a port summary of GDX-SERIAL-1E module.

<u>Register</u>	<u>MCS0/</u>	<u>MIOWT/</u>	<u>MIORD/</u>	<u>MA0</u>	<u>MA1</u>	<u>MA2</u>	<u>Port Add.</u>
Transmit Data	L	L	H	L	L	L	60H
Receive Data	L	H	L	L	L	L	60H
Int. Enable	L	L	H	H	L	L	61H
Int. Indent.	L	H	L	L	H	L	62H
Line Control	L	L	H	H	H	L	63H
Modem Control	L	L	H	L	L	H	64H
Line Status	L	H	L	H	L	H	65H
Modem Status	L	H	L	L	H	H	66H
Baud Rate (LS)	L	L	H	L	L	L	60H
Baud Rate (MS)	L	L	H	H	L	L	61H

NOTE: Access to the Baud Rate Register is done by toggling bit-7 in the Line Control. Signal names refer to module control signals.

2.7.2 Parallel-I/II Communications

The Parallel Communication option is based on the GDX-Parallel-3P expansion module. The expansion module uses a 8255 Parallel Peripheral Interface device which provides three 8-bit data ports or two 8-bit ports with handshaking.

In the Parallel Communications option, data is transmitted and received through two separate 7-bit data buses along with separate strobe and handshake lines (Mode 1 of the 8255).

Two 4-bit drivers (U1 and U2, See Schematic, Section 3.6) buffer receive data to Port A of the 8255 PPI, while Port B is initialized as an output for transmit data and buffered by two 4-bit drivers (7408 - U5/U6). Port C of the device is used for data control and handshaking of Ports A and B.

When the STROBE/ input (Port C, bit-4) is enabled by the host system, the current data at the Port A input is latched and an interrupt signal (Port C, bit-3) is generated for the CPU while an Input Buffer Full signal (Port C, bit-5) instructs the host system to halt further data transmission. During the interrupt service routine data is read from Port A, resetting the Input Buffer Full (IBF/) signal.

When data is transmitted from the VuePoint II, the CPU first checks the BUSY/ signal from the host system (Port C, bit-0). If passive, the CPU will load the 7-bit data into Port B three times, toggling bit-7 (MSB) high-low-high. This provides a 2 uSec STROBE/ signal for the host system.

2.0 Theory of Operation (continued)

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PORT SUMMARY

The following table is a port summary of the GDX-Parallel-3P Module:

<u>Port</u>	<u>MCS0/</u>	<u>MIOWT/</u>	<u>MIORD/</u>	<u>MA0</u>	<u>MA1</u>	<u>Port Add</u>
A-Data In	L	H	L	L	L	60H
A-Data Out	L	L	H	L	L	60H
B-Data Out	L	L	H	H	L	61H
C/Status	L	H	L	L	H	62H
Control	L	L	H	H	H	63H

NOTE: Signal names refer to module control signals.

2.8

Keyboard/Printer Interface Options

The Keyboard Interface allows the user to send data to the host system via the VPII communications port and if enabled, to a selected page buffer as well. The Printer Interface can be used to generate hard copies of a specified page buffer. The VuePoint II has provisions in firmware to support two modes of KEYBOARD/PRINTER interfacing, Serial or Parallel.

These expansion module interfaces are installed at the GDX-5 (lower right) location of the CPU board.

2.8.1

Parallel Keyboard/Printer Interface

The Parallel Keyboard/Printer option is based on the GDX-Parallel-3P expansion module, which is also used for the Parallel-I/II Communication option, since the board is configured in a manner similar to Section 2.7. In this option, two separate 7-bit data buses are used along with separate strobe and handshake lines (Mode 1, 8255).

When the STROBE/ input (Port C, bit-4) is toggled by the keyboard, the current keyboard data is latched at the Port A input. This causes the 8255A PPI to set the Input Buffer Full (IBF) signal, which instructs the keyboard to withhold further data transmissions. If the keyboard input is enabled, the CPU will routinely check the status of Port A. When data is read, the Input Buffer Full (IBF) signal is reset.

When the host system instructs the VuePoint II to print a specific page buffer, the CPU first checks the BUSY/ signal from the printer (Port C, bit-0); if active, the CPU will load the 7-bit printer data into Port B three times, toggling bit-7 (MSB) high-low-high. This provides a 2 usec STROBE/ signal for the printer.

See Section 2.7 for port summary of GDX-Parallel-3P module.

NOTE: Base address of port begins at A0H, rather than 60H.

2.8.2

Serial Keyboard/Printer Interface

The Serial Keyboard/Printer option is based on the GDX-SERIAL-2S expansion module. This module provides two channels of RS-232C communications using two 8251A USART (U5 and U6, See Schematic, Section 3.7). Since only one channel is required, one USART (U5) and accompanying driver/receiver packages (U1, U2) are removed from the module. The 8251A USART provides an input and output serial data along with several handshaking lines. These are buffered via driver/receiver packages (U3, U4) for RS-232C level conversion.

The USART requires an external baud rate clock for operation. This is supplied from the VPII CPU board via a wire wrap connection. All other serial communication parameters are initialized by using the options selected from the setup menu. This is accomplished by writing to the command port of the 8251A.

When the external keyboard sends valid serial data to the interface, the Receive Data Ready (RxRDY) signal of USART is enabled. This signal is routed through an unused RS-232C driver and connected to the Data Terminal Ready (DTR) output of the I/O connector, instructing the keyboard to halt further data transmission.

2.0 Theory of Operation (continued)

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If the keyboard is enabled, the CPU routinely checks the status of the USART by reading from the Command Port. If data is available, the CPU will read the data port, resetting the Receive Data Ready signal.

When a display page buffer has been selected for printing, the CPU will first check the status of both the transmitter (TxRDX) and the Data Set Ready (DSR) input of the USART. The DSR input is connected to the I/O connector via a RS-232C receiver, allowing the printer to control data transmission. If ready, a character is loaded into the data port and transmitted. This process is repeated until an entire page is printed.

PORT SUMMARY

The following is a port summary of the GDX-Serial-2S expansion module.

<u>Port</u>	<u>MCS0/</u>	<u>MCS1/</u>	<u>MIOWT/</u>	<u>MIORD/</u>	<u>MA0</u>	<u>Port Add.</u>
Receive Data	H	L	H	L	L	B0H
Transmit Data	H	L	L	H	L	B0H
Status	H	L	H	L	H	B1H
Command	H	L	L	H	H	B1H

NOTE: Signal names refer to module control signals.

2.9

Barcode Option

The Barcode Reader option uses the GDX-BARCODE-1 expansion module, which allows entry of both Code-39 and Interleaved 2 of 5 barcodes. The barcode module uses a 8301 Barcode I.C. (U1, See Schematic, Section 3) which processes incoming barcode data via a wand, and provides this data as well as status to the VPII CPU.

The external barcode reading device (wand) provides TTL Level signals at the J3 connection. This video data is passed to the Barcode Processor I.C. where the data is checked for validity. If the data comprises a valid barcode a status bit, periodically polled by the VPII CPU, is set. At this point the VPII CPU downloads this data to a buffer in the CPU RAM. This data is then passed on to the Host system when requested.

The Barcode module has two status ports, one for the Barcode Processor and one for the module status. These also have command ports that are used to initialize as well as control the operation of the barcode reader.

The module status provides the data available status bit (Bit-7), whereas the Barcode Processor status port provides Barcode Length type as well as data read. The module command port is used to enable or disable the operation of the barcode module while the Barcode Processor command port is initialized to send data to the VPII CPU.

PORT SUMMARY

The following is a port summary of the GDX-BARCODE-1 expansion module.

<u>Port</u>	<u>MCS0/</u>	<u>MCS1/</u>	<u>MIOWT/</u>	<u>MIORD/</u>	<u>MA0</u>	<u>Port Add.</u>
Processor Status	L	H	H	L	L	80H
Processor Command	L	H	L	H	L	80H
Module Status	L	H	H	L	H	81H
Module Command	L	H	L	H	H	81H

NOTE: Signal names refer to module control signals.

2.10 Speech Option

The VPII Speech Module option uses the GDX-SPEECH-TI expansion module. This module is based on the TI 5220 Speech Processor IC (U2, See Schematic, Section 3), which uses LPC-10 data for speech synthesis. The module has onboard ROMS (U3, U4) which are used to store LPC-10 speech data vocabularies. When the VuePoint II is commanded to speak, the VuePoint checks bit-7 of the module status port. If reset, VPII CPU loads in the starting address (16 bit) of a word which resides in the vocabulary ROM. The 5220 IC then begins to sequentially load data from the vocabulary ROM to the internal speech processor until the entire word or phrase has been spoken.

The speech module also has an on board low-pass filter (U8) to attenuate sampling noise as well as a 2 watt audio amplifier (U9) which is connected to an output Jack (J1). R15 provides a variable audio level control.

PORT SUMMARY

The following is a port summary of the GDX-BARCODE-1 expansion module.

<u>Port</u>	<u>MCS0/</u>	<u>MCS1/</u>	<u>MIOWT/</u>	<u>MIORD/</u>	<u>Port Add.</u>
Module Status	L	H	H	L	90H
Module Control/Data	L	H	L	H	90H

NOTE: Signal names refer to module control signals.

2.11 Power Supply/Universal Power Supply Option

The VuePoint II Power Supply provides all necessary DC power to VuePoint through an external DC power cable. The power supply consists of low voltage (+5 VDC) and high voltage (+250 VDC) regulated linear supplies, which are mounted into a heatsink enclosure.

To provide cooling to the unit, a 120 VAC fan is located at one end of the enclosure while the other end is used for mounting a power switch, a DC output connector and Line Input/Filter/Fuse assembly.

In order to generate + and - 12 VDC, a special power supply adaptor board (See Schematic, Section 3.8) is mounted internally in the power supply unit. This board consists of a voltage doubler which provides + and - 20 VDC to two IC voltage regulators which supply the + and - 12 VDC output.

If the power supply is to be operated at 220 VAC the transformer connections are rewired, connecting the primary windings in series instead of parallel (120 VAC).

In Universal Power Supply units, a similar configuration is used; however, the power supply adaptor board (Universal, See Schematic, Section 3.9) also provides automatic switching of the high voltage to 300 VDC, in order to accommodate the use of VuePoint II's with the Green Display option. An opto-isolator (U2) changes the voltage at the adjustment potentiometer when the enable signal (300V/) is grounded at the VuePoint II rear power connector. The Universal Power Supply adaptor board isolates the High Voltage from the exposed pins on the DC power cable when the cable is removed from the VuePoint II. This is also achieved by grounding an enable signal (HV/).

The Universal Power Supply also allows selection of input line voltages through positioning of a selector card in the Line Input/Filter/Fuse assembly. This automatically connects the transformer primaries in a series or parallel configuration for 240 VAC or 120 VAC, respectively. The series format also provides a 120 VAC step down source for powering the internal fan.

2.12 Embedded Power Supply Option

The VuePoint II Embedded Power Supply option provides all necessary DC power to the VuePoint. The power supply case is designed to become an integral part of the VuePoint by replacing the top rear cover panel.

The Embedded Power Supply consists of a switching power supply which converts 120 or 240 VAC to +5, +12, and -12 VDC. A small DC to DC converter is then employed to convert the +12 VDC to +250 VDC required by the Gas Plasma Display, this configuration provides increased efficiency over the external power supply option thus eliminating the need for forced-air cooling.

The power supply uses an AC Line Filter/Fuse assembly for attenuation of switching noise. Internal cable assemblies are provided, which connect directly to the internal VPII circuit boards.

3.1 VuePoint II CPU Board Schematics

JP3 WIREWRAP CONFIGURATION

7A – 5B

9A – 18A

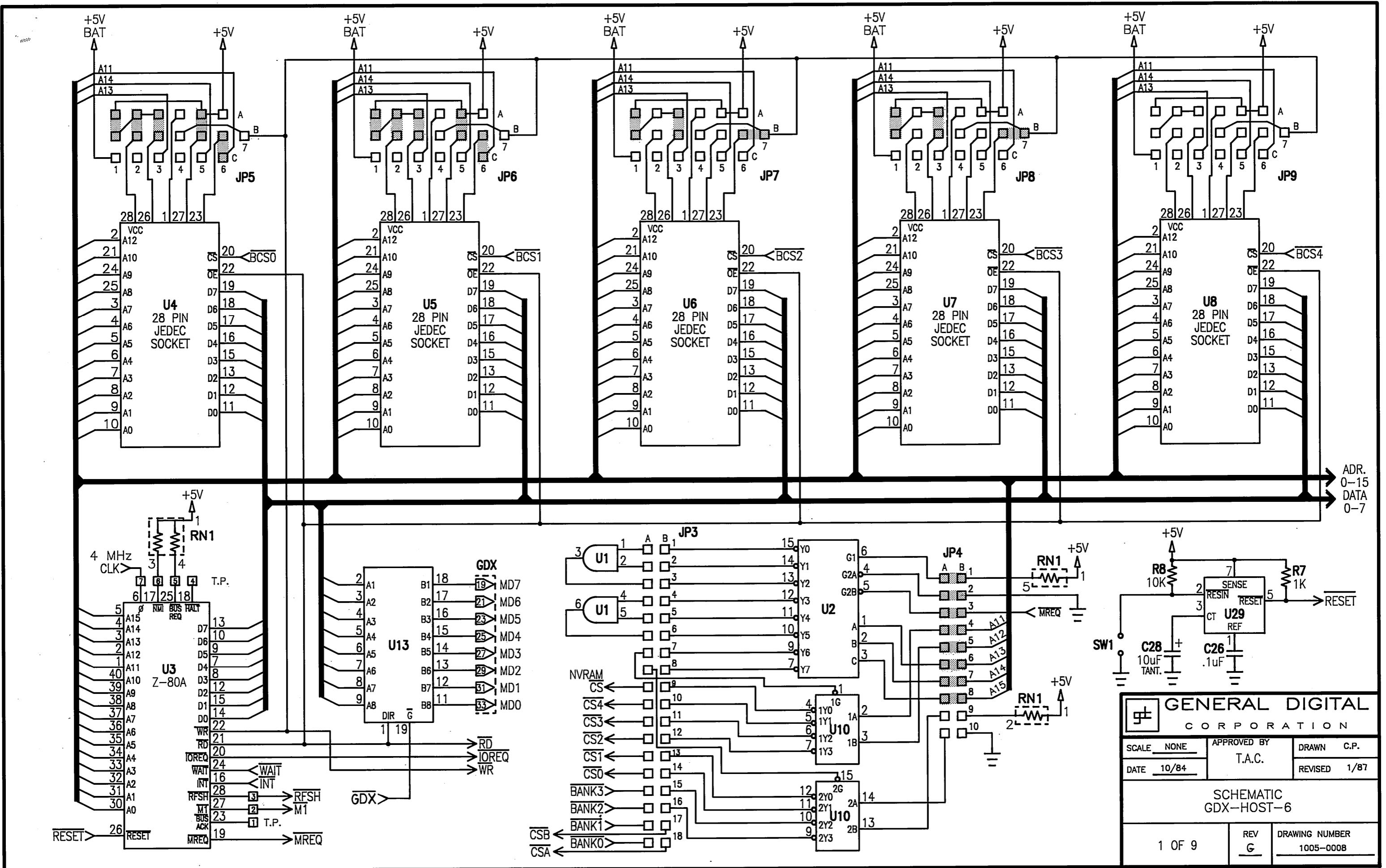
11A – 10B

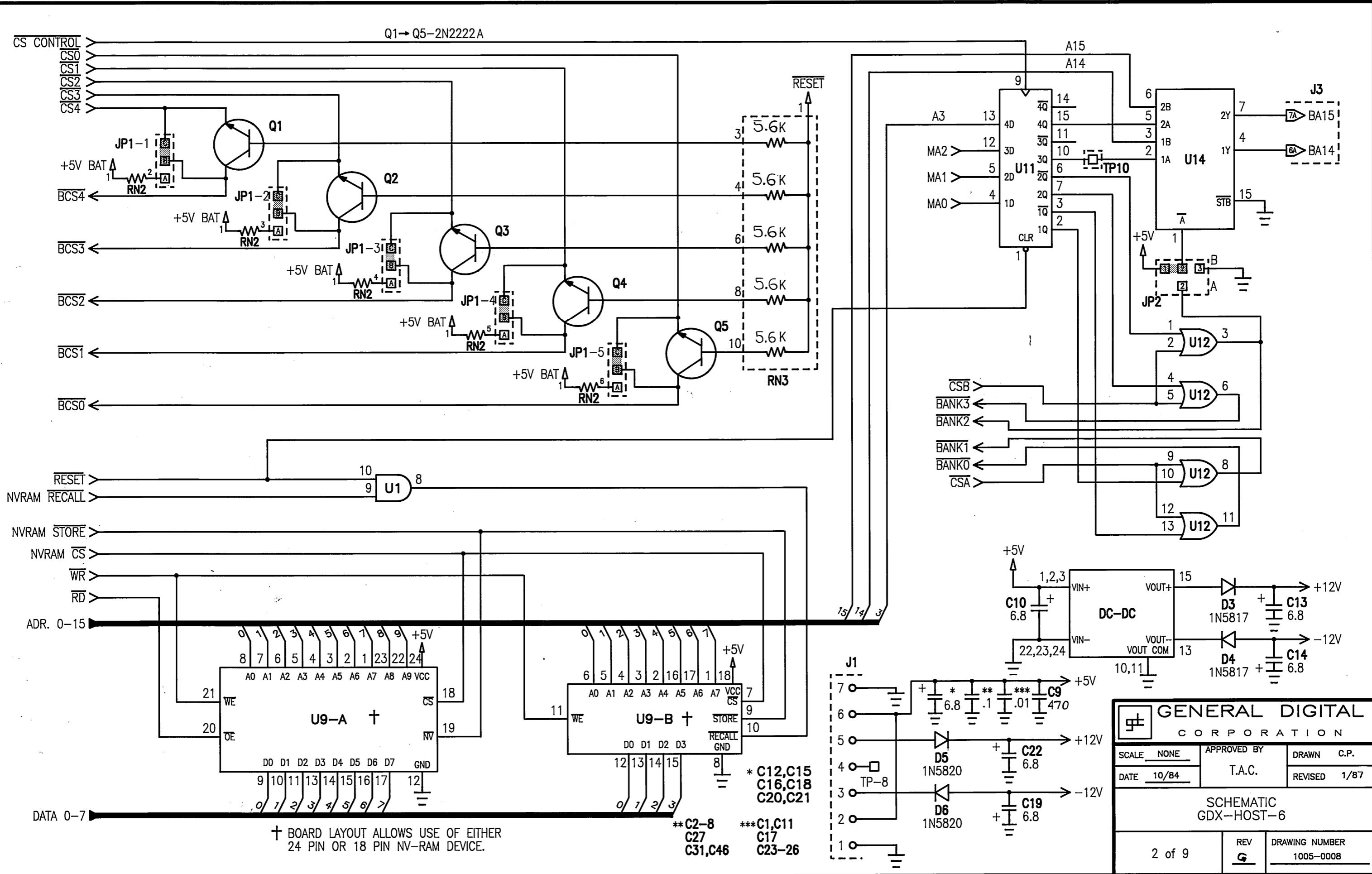
12A – 9B

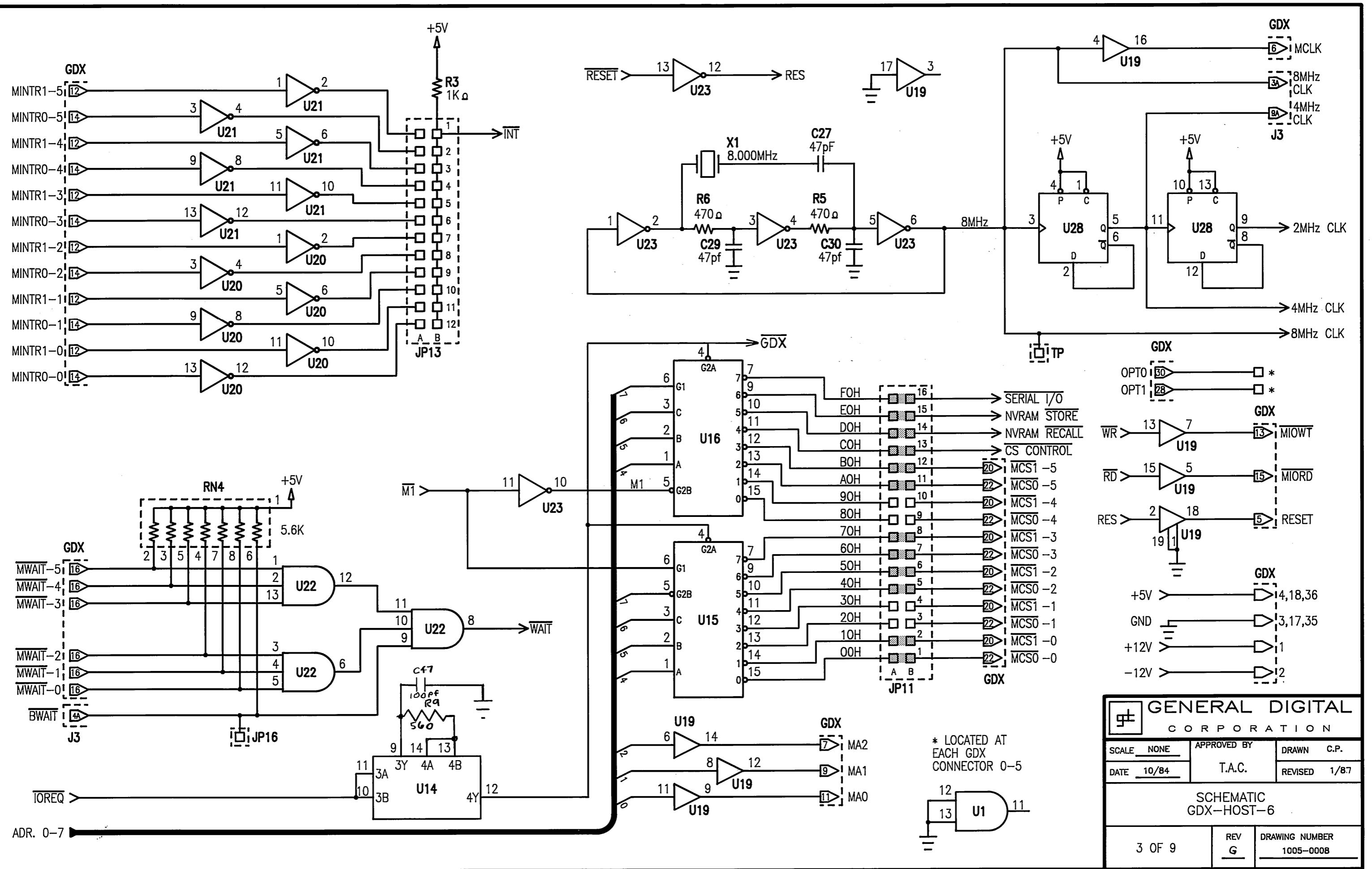
13A – 2B

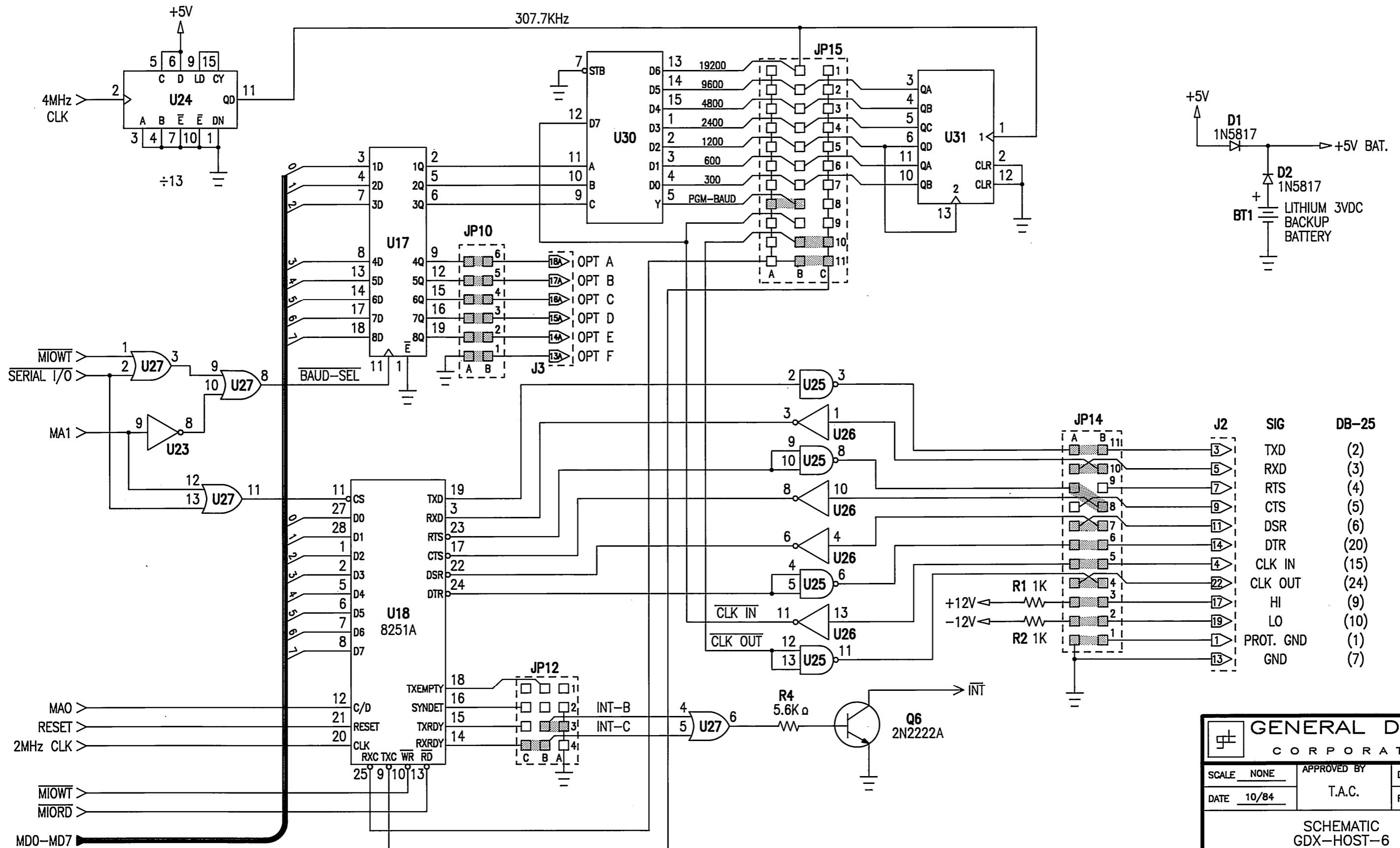
14A – 1B

4B – 18B

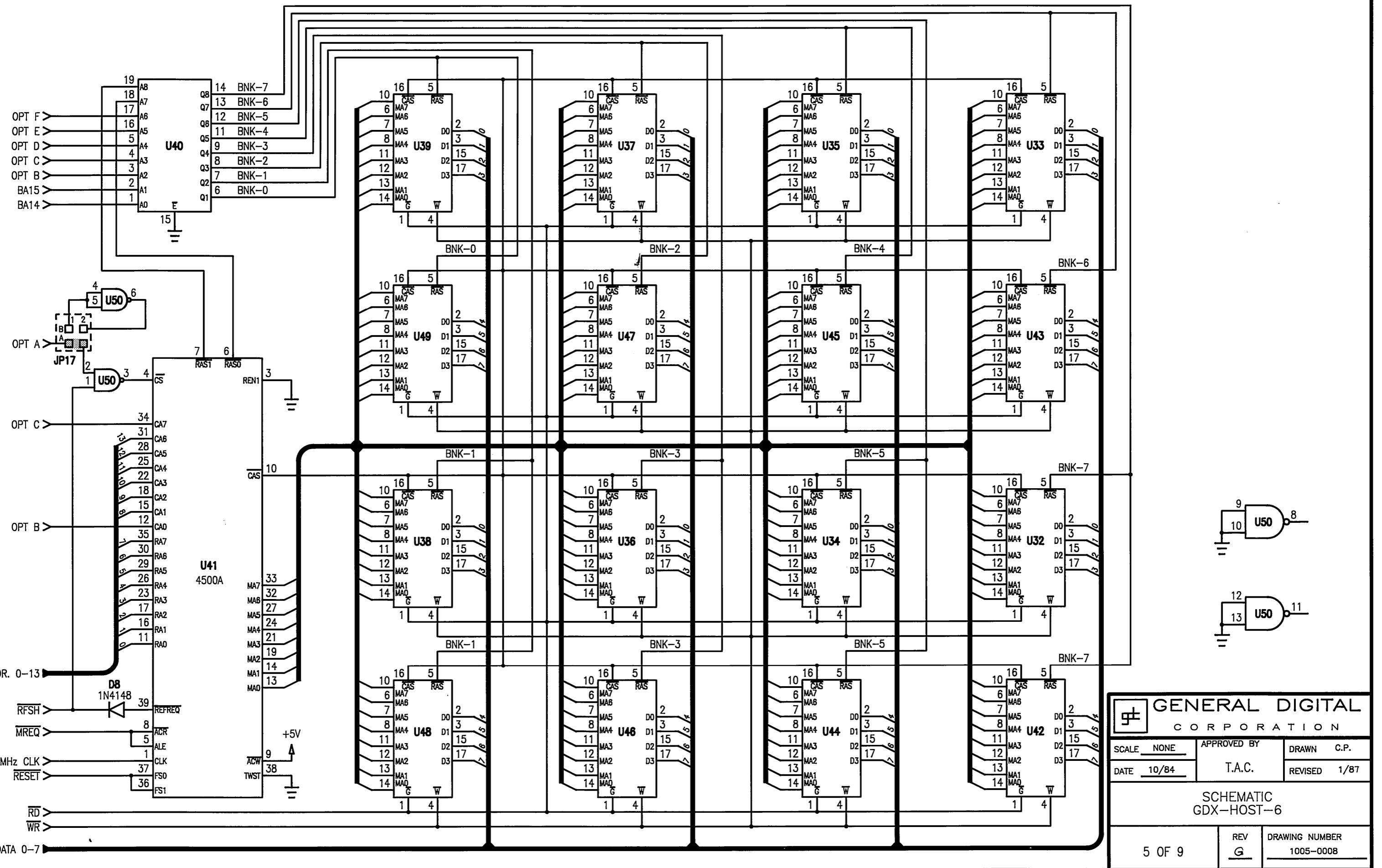


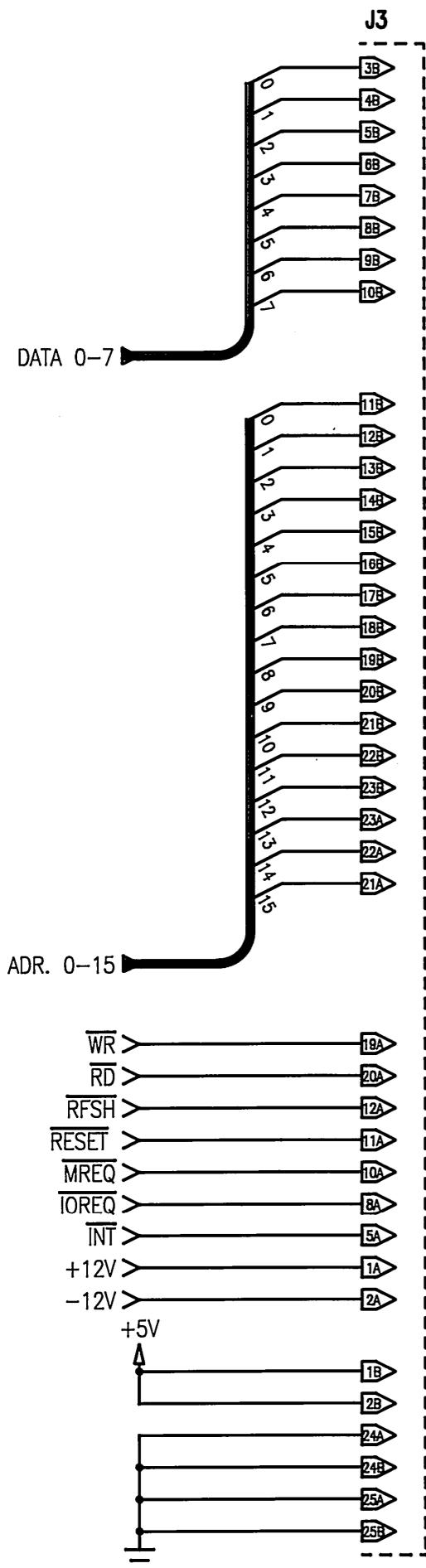






GENERAL DIGITAL CORPORATION	
SCALE <u>NONE</u>	APPROVED BY <u>T.A.C.</u>
DATE <u>10/84</u>	DRAWN <u>C.P.</u>
REV <u>G</u> DRAWING NUMBER <u>1005-0008</u>	
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* SEE SCHEMATIC (PAGE 2)

** +12VDC ON PIN 14, -12VDC ON PIN 1

CONNECTOR J2			
SERIAL I/O			
PIN	SIGNAL	PIN	SIGNAL
1	PROT. GND	2	-
3	TX DATA	4	CLK IN
5	RX DATA	6	-
7	REQ TO SND	8	-
9	CLR TO SND	10	-
11	DATA SET RDY	12	-
13	GND	14	DATA TERM RDY
15	-	16	-
17	HI(+12)	18	-
19	LO(-12)	20	-
21	-	22	CLK OUT
23	-	24	-
25	-	26	-

CONNECTOR GDX0-GDX5			
EXPANSION MODULE BUS			
PIN	SIGNAL	PIN	SIGNAL
1	+12V	2	-12V
3	GND	4	+5V
5	RESET	6	MCLK
7	MA2	8	-
9	MA1	10	RESERVED
11	MA0	12	MINTR1
13	MIOWT	14	MINTR0
15	MIORD	16	MWAIT
17	GND	18	+5V
19	MD7	20	MCS1
21	MD6	22	MCS0
23	MD5	24	RESERVED
25	MD4	26	-
27	MD3	28	OPT1
29	MD2	30	OPT0
31	MD1	32	-
33	MDO	34	-
35	GND	36	+5V

CONNECTOR J3			
BUS EXPANSION			
PIN	SIGNAL	PIN	SIGNAL
1A	+12V	1B	+5V
2A	-12V	2B	+5V
3A	8MHz	3B	D0
4A	BWAIT	4B	D1
5A	INT	5B	D2
6A	BA14	6B	D3
7A	BA15	7B	D4
8A	IREQ	8B	D5
9A	4MHz	9B	D6
10A	MREQ	10B	D7
11A	RESET	11B	A0
12A	RFSH	12B	A1
13A	OPT F	13B	A2
14A	OPT E	14B	A3
15A	OPT D	15B	A4
16A	OPT C	16B	A5
17A	OPT B	17B	A6
18A	OPT A	18B	A7
19A	WR	19B	A8
20A	RD	20B	A9
21A	A15	21B	A10
22A	A14	22B	A11
23A	A13	23B	A12
24A	GND	24B	GND
25A	GND	25B	GND

CONNECTOR J1			
POWER			
PIN	SIGNAL	PIN	SIGNAL
1	GND	2	+5V
3	-12V	4	TP-8
5	+12V	6	+5V
7	GND		

RESISTOR NETWORKS		
#	TYPE	# PINS
RN1	5.6KΩ SIP	6
RN2	1KΩ SIP	6
RN3	5.6KΩ SIP	10
RN4	5.6KΩ SIP	8
RN5	1KΩ SIP	6

GENERAL DIGITAL CORPORATION

SCALE <u>NONE</u>	APPROVED BY <u>T.A.C.</u>	DRAWN <u>C.P.</u>
DATE <u>10/84</u>	REV <u>G</u>	DRAWING NUMBER <u>1005-0008</u>

SCHEMATIC
GDX-HOST-6

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NOTE:
RESISTORS-1/4 WATT UNLESS OTHERWISE SPECIFIED.
CAPACITORS-DECIMAL VALUES ARE MICROFARADS, ALL OTHERS ARE PICOFARADS.

JP1					
CS PULLUP ENABLE					
PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1A	+5V BAT-PU	1B	<u>BCS4</u>	1C	<u>CS4</u>
2A		2B	<u>BCS3</u>	2C	<u>CS3</u>
3A		3B	<u>BCS2</u>	3C	<u>CS2</u>
4A		4B	<u>BCS1</u>	4C	<u>CS1</u>
5A	+5V BAT-PU	5B	<u>BCS0</u>	5C	<u>CS0</u>

JP4					
MEMORY DECODE INPUT					
PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1A	DECOD8-G1	1B	+5V-PU		
2A	DECOD8-G2A	2B	GND		
3A	DECOD8-G2B	3B	MREQ		
4A	DECOD4-1A	4B	A11		
5A	DECOD4-1B	5B	A12		
6A	DECOD8-A	6B	A13		
7A	DECOD8-B	7B	A14		
8A	DECOD8-C	8B	A15		
9A	DECOD4-2B	9B	+5V-PU		
10A	DECOD4-2A	10B	GND		

JP7					
JEDEC CONFIGURATION-U6					
PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1A	+5V BAT	1B	VCC	1C	+5V
2A	N/C	2B	U6/28	2C	VCC
3A	A13	3B	U6/26	3C	VCC
4A	N/C	4B	WR	4C	U6/1
5A	A14	5B	U6/27	5C	+5V
6A	A11	6B	U6/23	6C	+5V
		7B	WR		

JP2			
B-ADDRESS CONTROL			
PIN	SIGNAL	PIN	SIGNAL
2A	<u>BANK2</u>	1B	+5V
		2B	U14/1
		3B	GND

JP5					
JEDEC CONFIGURATION-U4					
PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1A	+5V BAT	1B	VCC	1C	+5V
2A	N/C	2B	U4/28	2C	VCC
3A	A13	3B	U4/26	3C	VCC
4A	N/C	4B	WR	4C	U4/1
5A	A14	5B	U4/27	5C	+5V
6A	A11	6B	U4/23	6C	+5V
		7B	WR		

JP3			
MEMORY DECODE OUTPUT			
PIN	SIGNAL	PIN	SIGNAL
1A	U1/1	1B	DECOD8-Y0
2A	U1/2	2B	DECOD8-Y1
3A	U1/3	3B	DECOD8-Y2
4A	U1/4	4B	DECOD8-Y3
5A	U1/5	5B	DECOD8-Y4
6A	U1/6	6B	DECOD8-Y5
7A	DECOD4-1G	7B	DECOD8-Y6
8A	DECOD4-2G	8B	DECOD8-Y7
9A	NVRAM-CS	9B	DECOD4-1Y0
10A	<u>CS4</u>	10B	DECOD4-1Y1
11A	<u>CS3</u>	11B	DECOD4-1Y2
12A	<u>CS2</u>	12B	DECOD4-1Y3
13A	<u>CS1</u>	13B	DECOD4-2Y0
14A	<u>CS0</u>	14B	DECOD4-2Y1
15A	<u>BANK3</u>	15B	DECOD4-2Y2
16A	<u>BANK2</u>	16B	DECOD4-2Y3
17A	<u>BANK1</u>	17B	<u>CSB</u>
18A	<u>BANK0</u>	18B	<u>CSA</u>

JP6					
JEDEC CONFIGURATION-U5					
PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1A	+5V BAT	1B	VCC	1C	+5V
2A	N/C	2B	U5/28	2C	VCC
3A	A13	3B	U5/26	3C	VCC
4A	N/C	4B	WR	4C	U5/1
5A	A14	5B	U5/27	5C	+5V
6A	A11	6B	U5/23	6C	+5V
		7B	WR		

JP9					
JEDEC CONFIGURATION-U8					
PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1A	+5V BAT	1B	VCC	1C	+5V
2A	N/C	2B	U8/28	2C	VCC
3A	A13	3B	U8/26	3C	VCC
4A	N/C	4B	WR	4C	U8/1
5A	A14	5B	U8/27	5C	+5V
6A	A11	6B	U8/23	6C	+5V
		7B	WR		

	GENERAL DIGITAL	
	CORPORATION	
SCALE	NONE	APPROVED BY
DATE	10/84	T.A.C.
REV	G	DRAWING NUMBER
SCHEMATIC		1005-0008
GDX-HOST-6		
7 OF 9		

JP10			
128K DRAM BANK CONTROL			
PIN	SIGNAL	PIN	SIGNAL
1A	GND	1B	OPT F
2A	BAUD-SEL/Q8	2B	OPT E
3A	BAUD-SEL/Q7	3B	OPT D
4A	BAUD-SEL/Q6	4B	OPT C
5A	BAUD-SEL/Q5	5B	OPT B
6A	BAUD-SEL/Q4	6B	OPT A

JP11			
GDX I/O SELECT			
PIN	SIGNAL	PIN	SIGNAL
1A	PORT 00H	1B	MCS0-0
2A	PORT 10H	2B	MCS1-0
3A	PORT 20H	3B	MCS0-1
4A	PORT 30H	4B	MCS1-1
5A	PORT 40H	5B	MCS0-2
6A	PORT 50H	6B	MCS1-2
7A	PORT 60H	7B	MCS0-3
8A	PORT 70H	8B	MCS1-3
9A	PORT 80H	9B	MCS0-4
10A	PORT 90H	10B	MCS1-4
11A	PORT A0H	11B	MCS0-5
12A	PORT B0H	12B	MCS1-5
13A	PORT C0H	13B	CS-CONTROL
14A	PORT D0H	14B	NVRAM-RECALL
15A	PORT E0H	15B	NVRAM-STORE
16A	PORT F0H	16B	SERIAL I/O

JP13			
GDX INTERRUPT ENABLE			
PIN	SIGNAL	PIN	SIGNAL
1A	MINTR1-5	1B	INT
2A	MINTR0-5	2B	
3A	MINTR1-4	3B	
4A	MINTR0-4	4B	
5A	MINTR1-3	5B	
6A	MINTR0-3	6B	
7A	MINTR1-2	7B	
8A	MINTR0-2	8B	
9A	MINTR1-1	9B	
10A	MINTR0-1	10B	
11A	MINTR1-0	11B	INT
12A	MINTR0-0	12B	

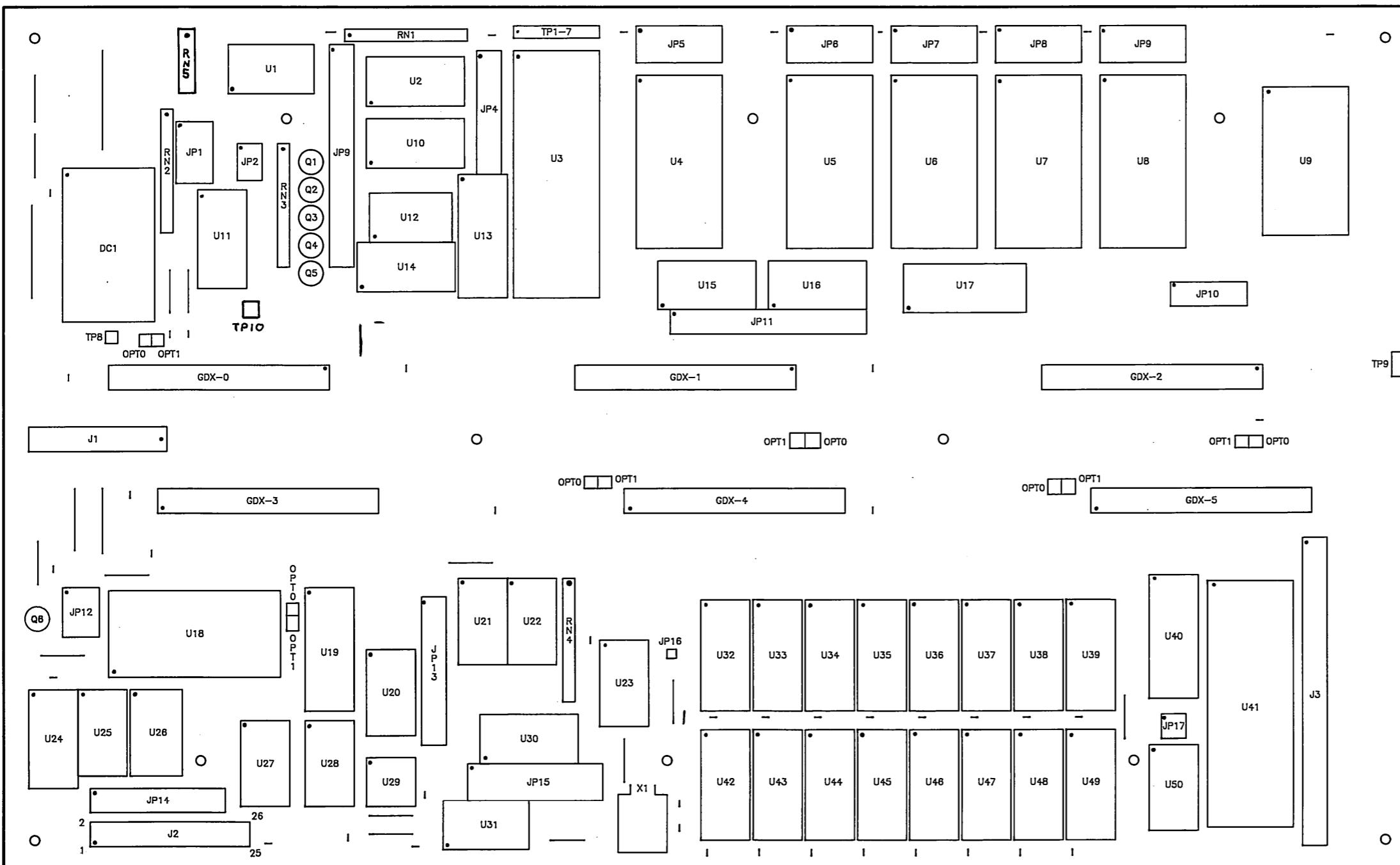
JP15			
BAUD RATE			
PIN	SIGNAL	PIN	SIGNAL
1A	RXC	1B	19200
2A		2B	9600
3A		3B	4800
4A		4B	2400
5A		5B	1200
6A		6B	600
7A		7B	300
8A		8B	PGM-BAUD
9A		9B	CLK IN
10A		10B	CLK OUT
11A		11B	RXC
			TXC

JP14			
SERIAL I/O			
PIN	SIGNAL	PIN	SIGNAL
1A	GND	1B	J2/1
2A	LO(-12V)	2B	J2/19
3A	HI(+12V)	3B	J2/17
4A	J2/22	4B	CLK OUT
5A	CLK IN	5B	J2/4
6A	DTR	6B	J2/14
7A	J2/11	7B	DSR
8A	J2/9	8B	CTS
9A	RTS	9B	J2/7
10A	J2/5	10B	RXD
11A	TXD	11B	J2/3

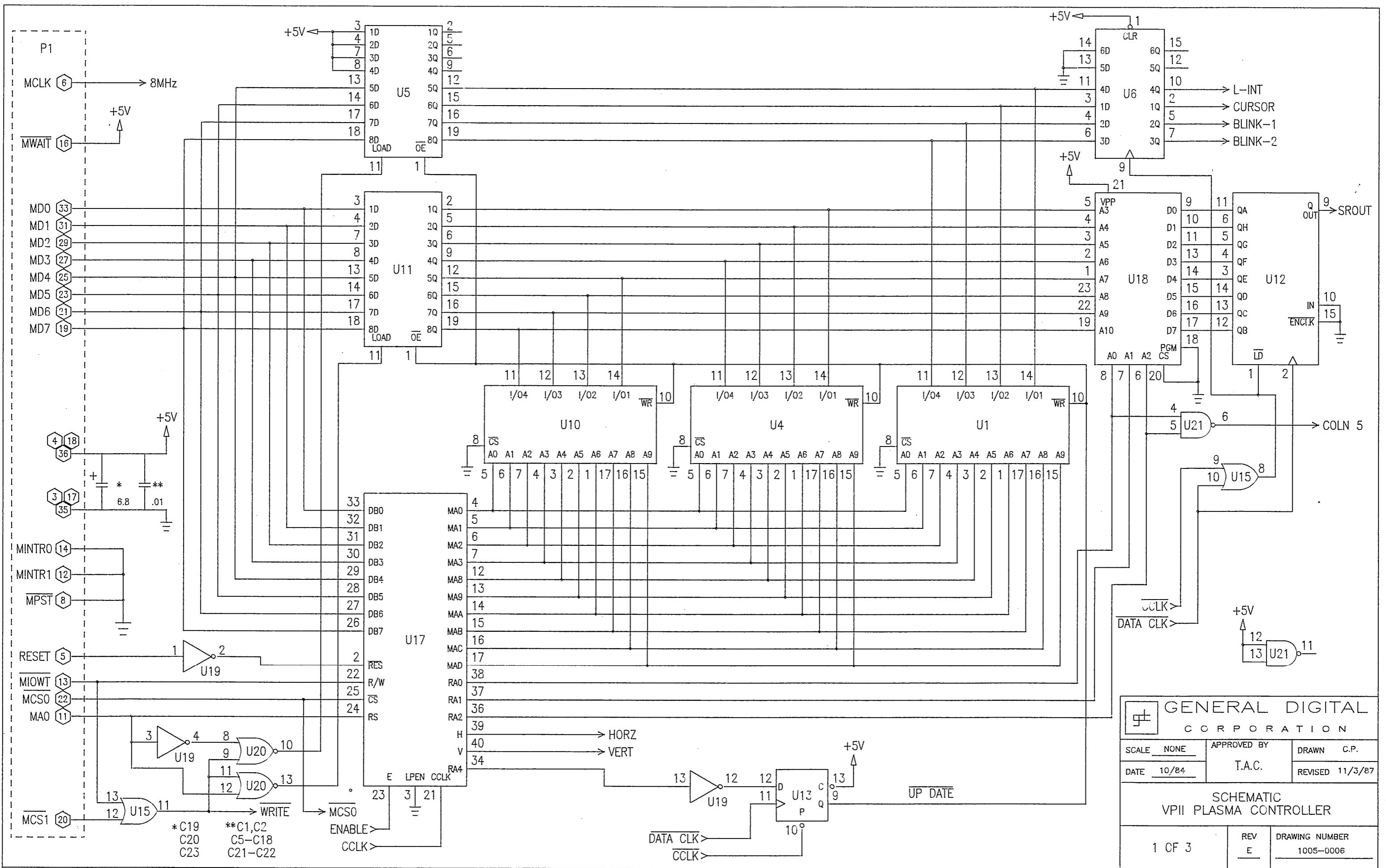
JP16			
128K/512K DRAM ENABLE			
PIN	SIGNAL	PIN	SIGNAL
1A	OPT A	1B	A
2A	CS	2B	Y

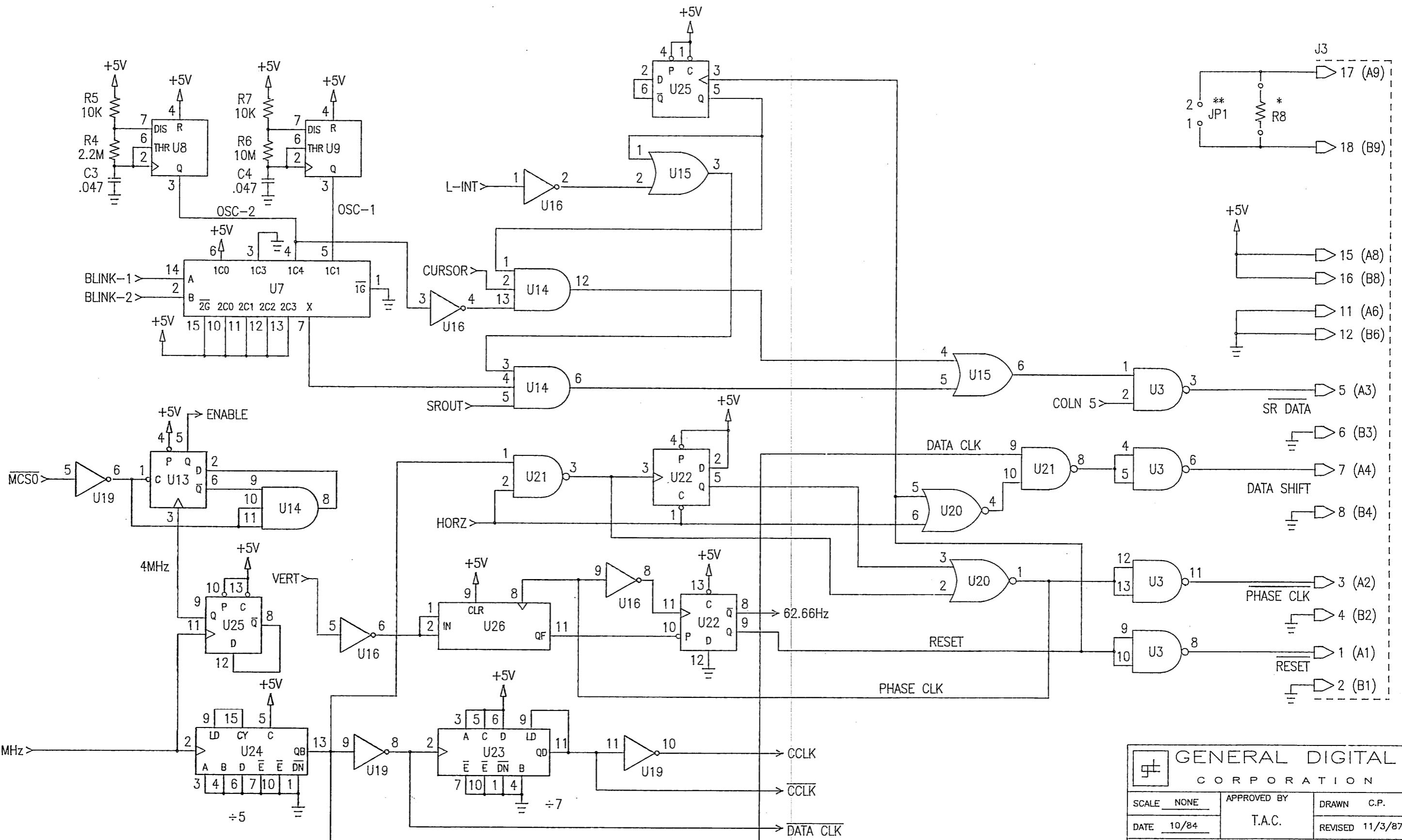
JP12					
SERIAL I/O INTERRUPTS					
PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1A	N/C	1B	TXEMPTY	1C	N/C
2A	GND	2B	N/C	2C	SYNDET
3A	GND	3B	INT-B	3C	TXRDY
4A	GND	4B	INT-C	4C	RXRDY

GENERAL DIGITAL CORPORATION	SCALE <u>NONE</u>	APPROVED BY <u>T.A.C.</u>	DRAWN <u>C.P.</u>
DATE <u>10/84</u>	REV <u>G</u>	REvised <u>1/87</u>	DRAWING NUMBER <u>1005-0008</u>
SCHEMATIC GDX-HOST-6			
8 OF 9	REV <u>G</u>	DRAWING NUMBER <u>1005-0008</u>	



GENERAL DIGITAL		CORPORATION	
SCALE <u>NONE</u>	APPROVED BY	DRAWN C.P.	
DATE <u>12/84</u>	T.A.C.	REVISED <u>1/87</u>	
SCHEMATIC GDX-HOST-6			
9 OF 9	REV <u>G</u>	DRAWING NUMBER <u>1005-0008</u>	





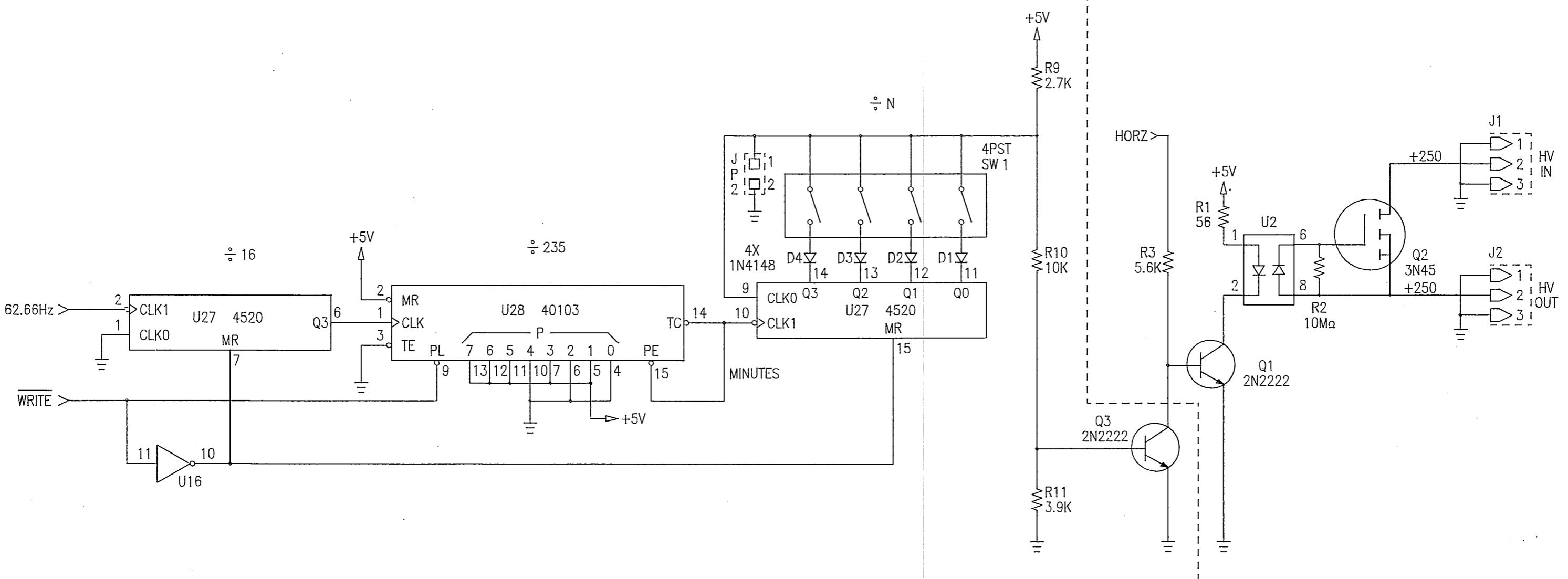
* OPTIONAL RESISTOR FOR DISPLAY BRIGHTNESS CONTROL.

** OPTIONAL 2PIN .1 SP CONNECTOR FOR POTENTIOMETER CONTROL OF BRIGHTNESS. (50K Ω)

GENERAL DIGITAL CORPORATION		
SCALE	NONE	APPROVED BY
DATE	10/84	T.A.C.
		DRAWN C.P.
REV E DRAWING NUMBER 1005-0006		
2 OF 3		

SCHEMATIC
VPII PLASMA CONTROLLER

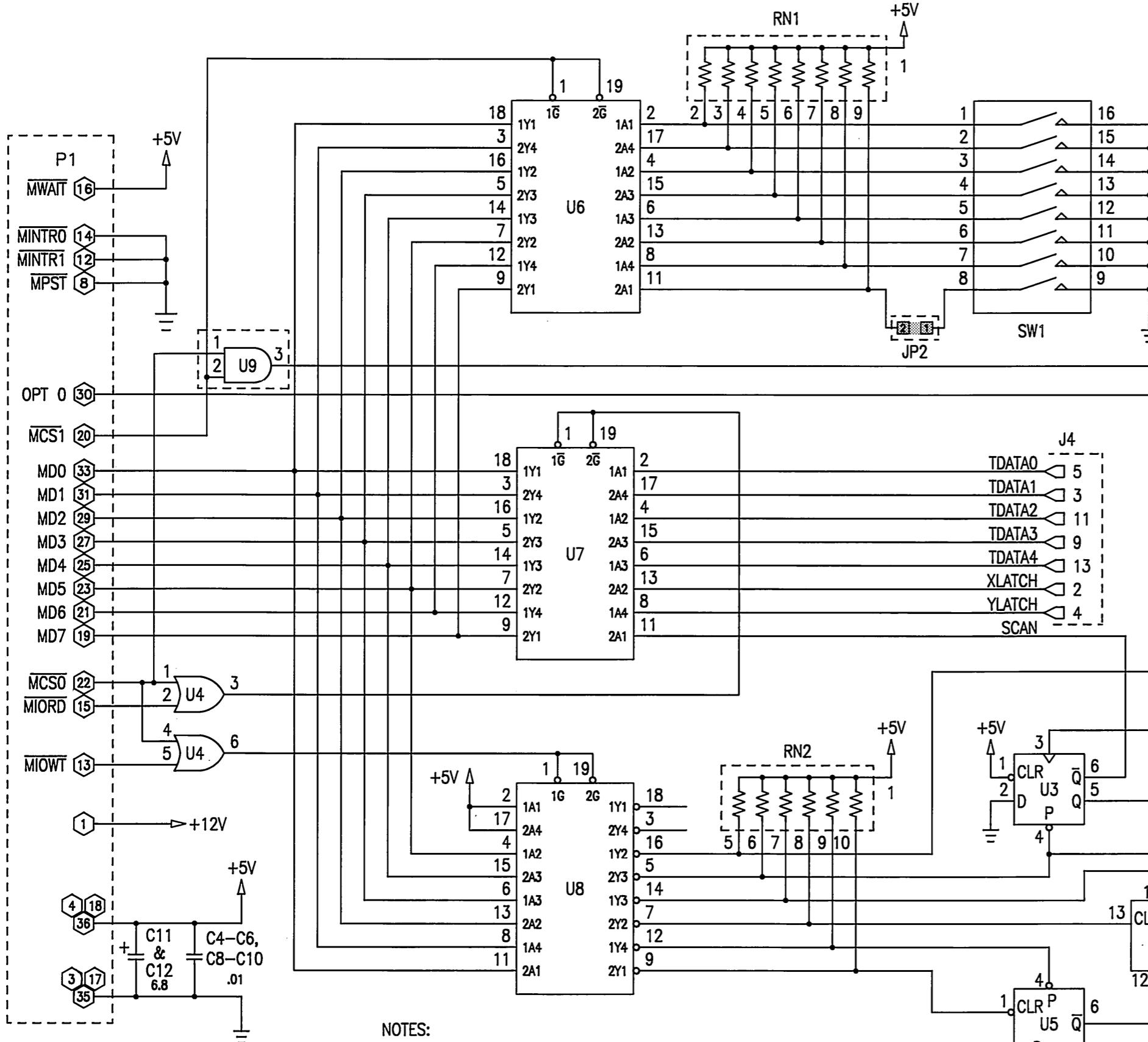
OPTIONAL DISPLAY BLANKING CIRCUIT



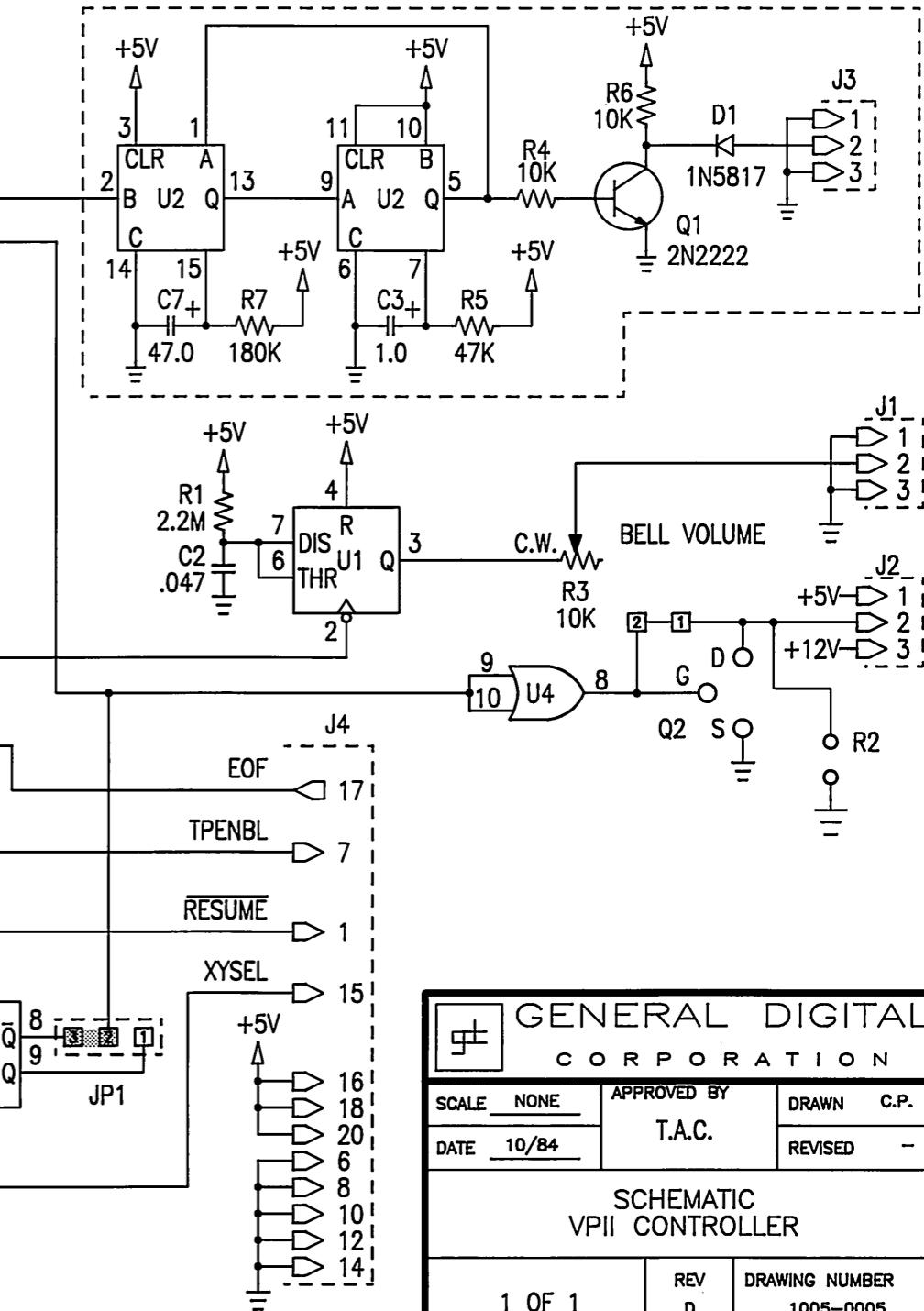
IC	TYPE	+5	GND	IC	TYPE	+5	GND
U1	2114	18	9	U15	74LS32	14	7
U2	DIG-11-06-30	-	-	U16	74LS04	14	7
U3	74LS38	14	7	U17	6545EA	20	1
U4	2114	18	9	U18	2716	24	12
U5	74LS373	20	10	U19	74LS04	14	7
U6	74LS174	16	8	U20	74LS02	14	7
U7	74LS153	16	8	U21	74LS00	14	7
U8	555	8	1	U22	74LS74	14	7
U9	555	8	1	U23	74LS169	16	8
U10	2114	18	9	U24	74LS169	16	8
U11	74LS373	20	10	U25	74LS74	14	7
U12	74LS165	16	8	U26	74LS164	14	7
U13	74LS74	14	7	U27	4520	16	8
U14	74LS11	14	7	U28	40103	16	8

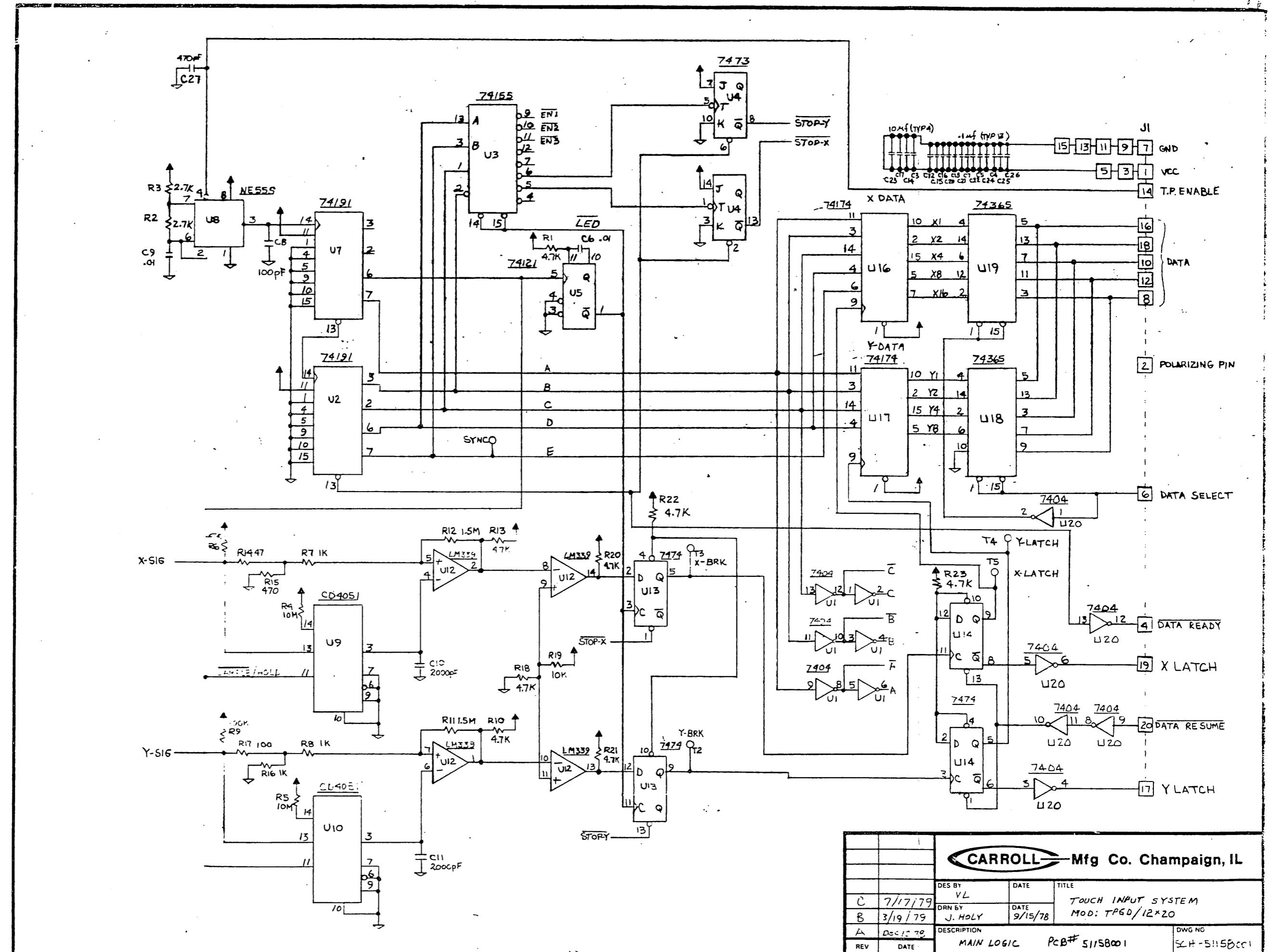
NOTE:
RESISTORS-1/4 WATT UNLESS OTHERWISE SPECIFIED.
CAPACITORS-DECIMAL VALUES ARE MICROFARADS, ALL OTHERS ARE PICOFARADS.

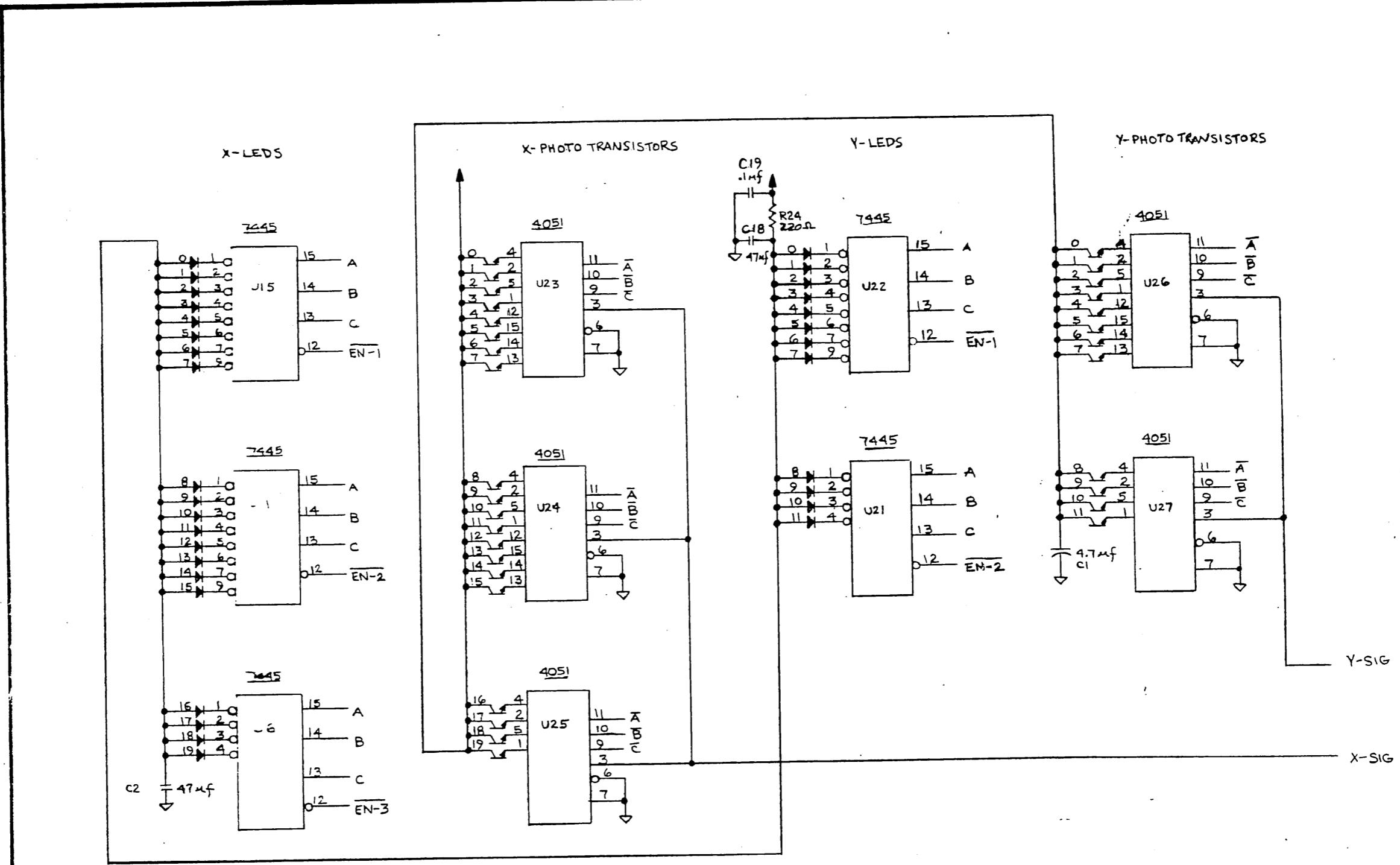
GENERAL DIGITAL CORPORATION		
SCALE <u>NONE</u>	APPROVED BY <u>T.A.C.</u>	
DATE <u>10/84</u>	DRAWN <u>C.P. R.J.</u> REVISED <u>11/3/87</u>	
SCHEMATIC VPII PLASMA CONTROLLER		
3 OF 3	REV <u>E</u>	DRAWING NUMBER <u>1005-0006</u>



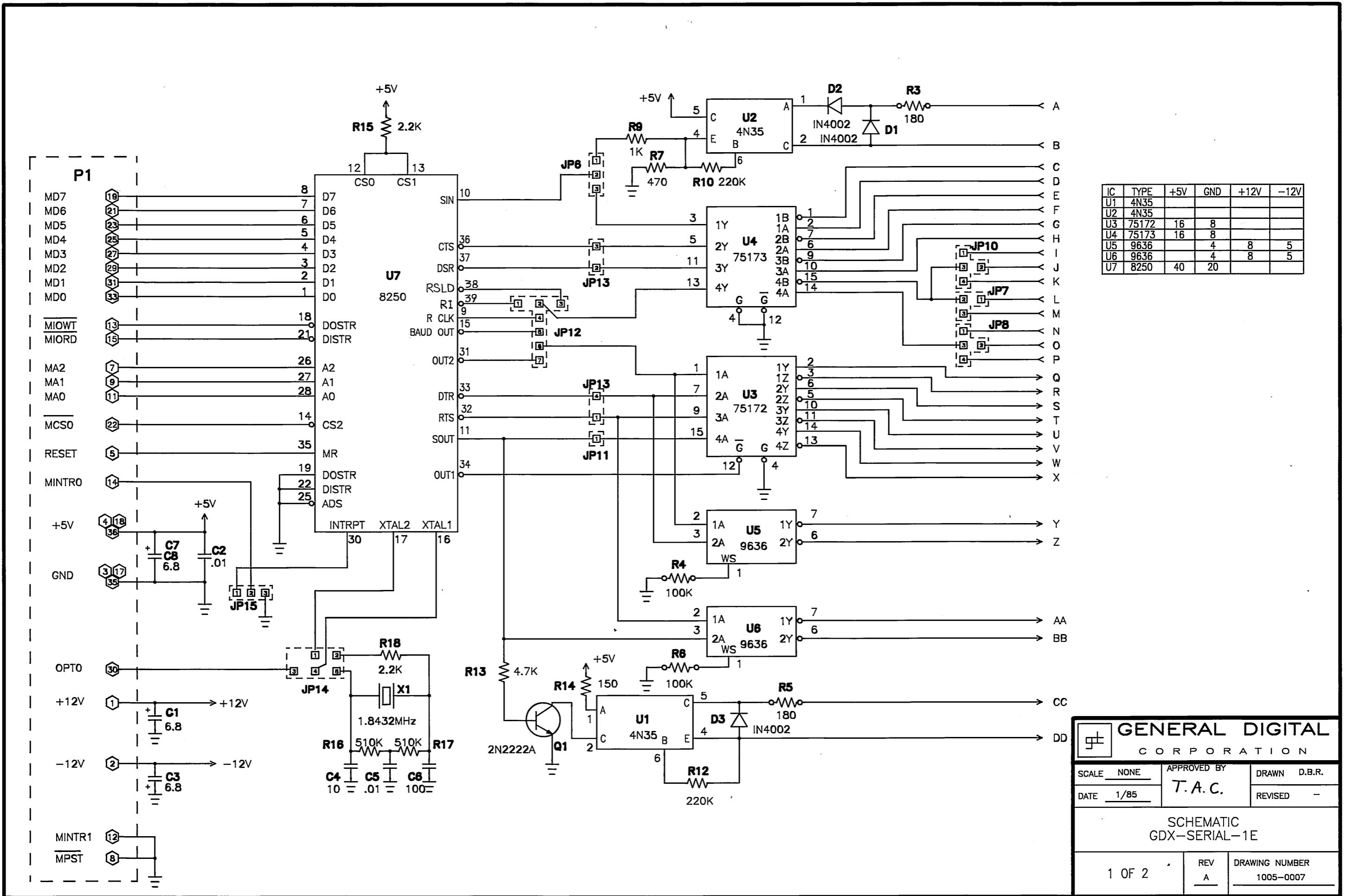
IC	TYPE	+5	GND
U1	555	8	1
U2	74LS123	16	8
U3	74LS74	14	7
U4	74LS32	14	7
U5	74LS74	14	7
U6	74LS244	20	10
U7	74LS244	20	10
U8	74LS240	20	10
U9	74LS08	14	7
RN1	5.6K SIP	1	-
RN2	5.6K SIP	1	-
SW1	DIP SWITCH	-	-

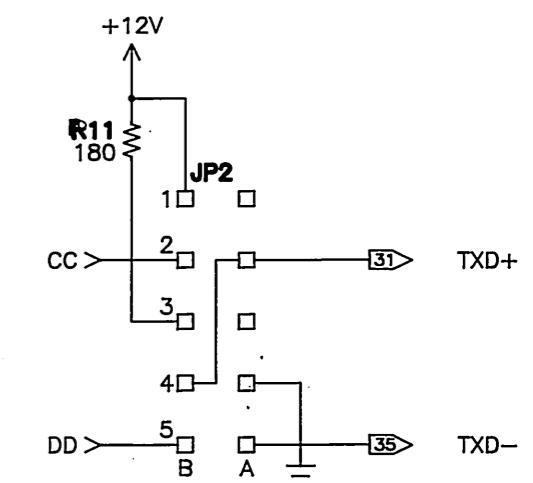
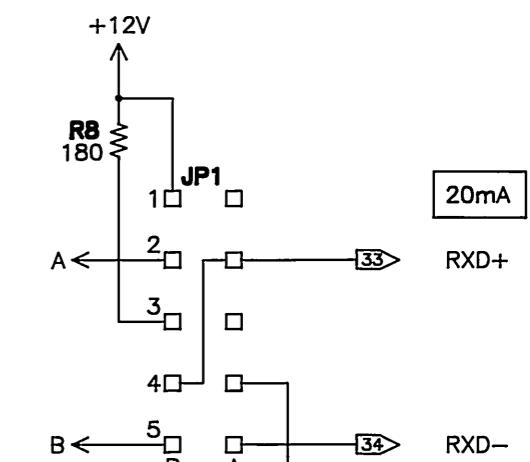
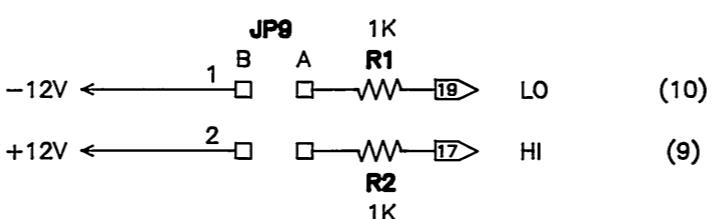
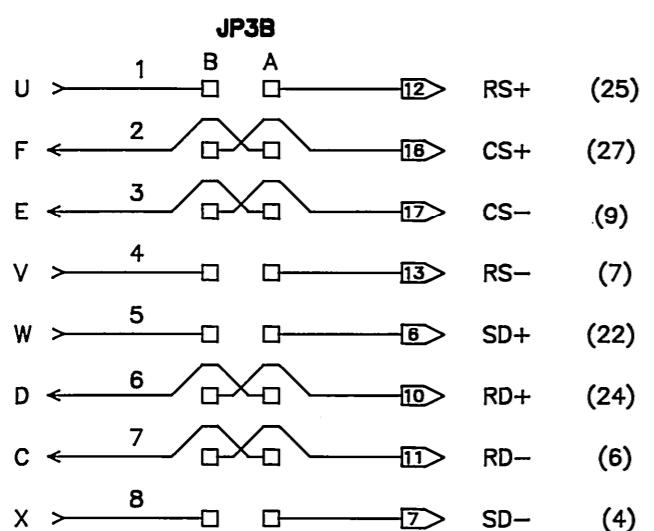
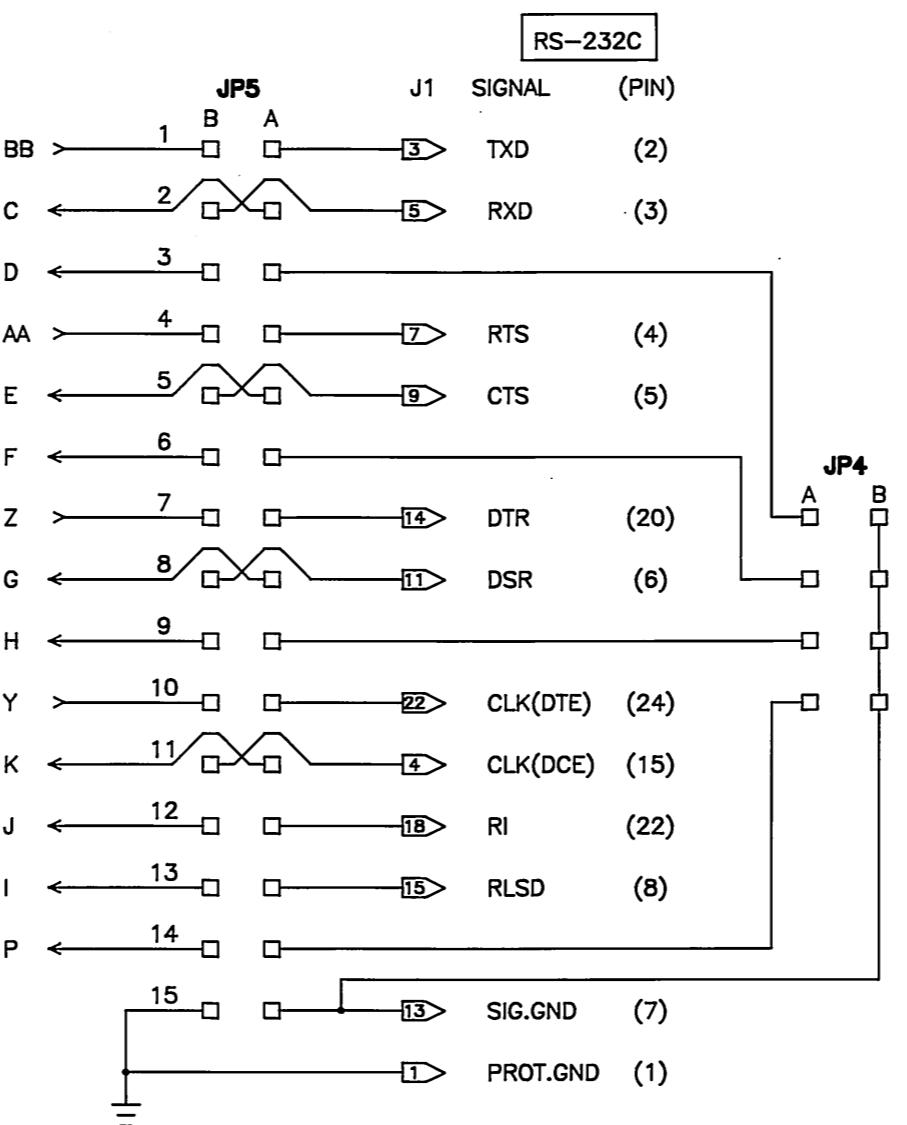
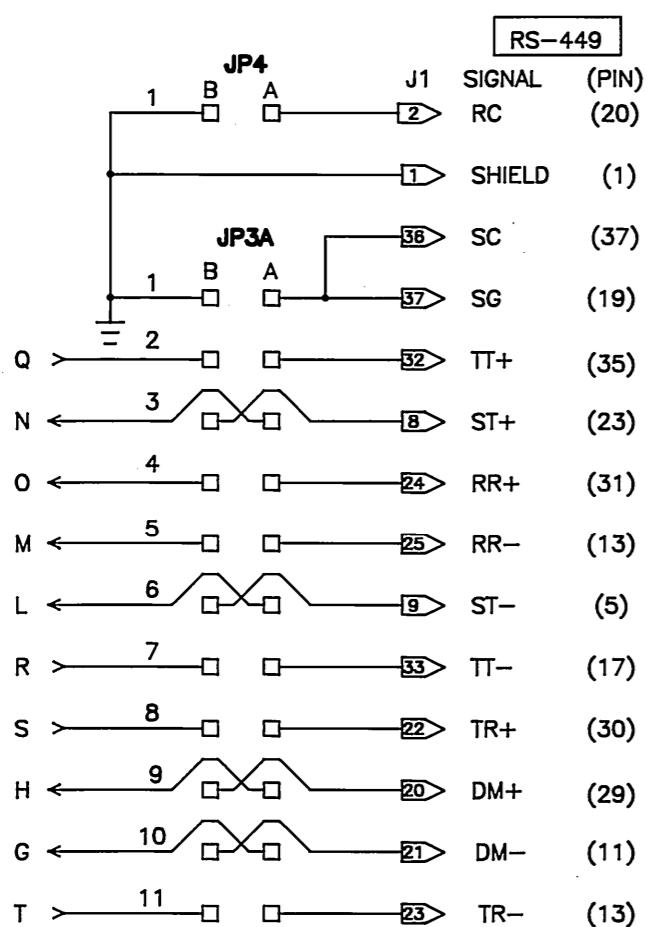




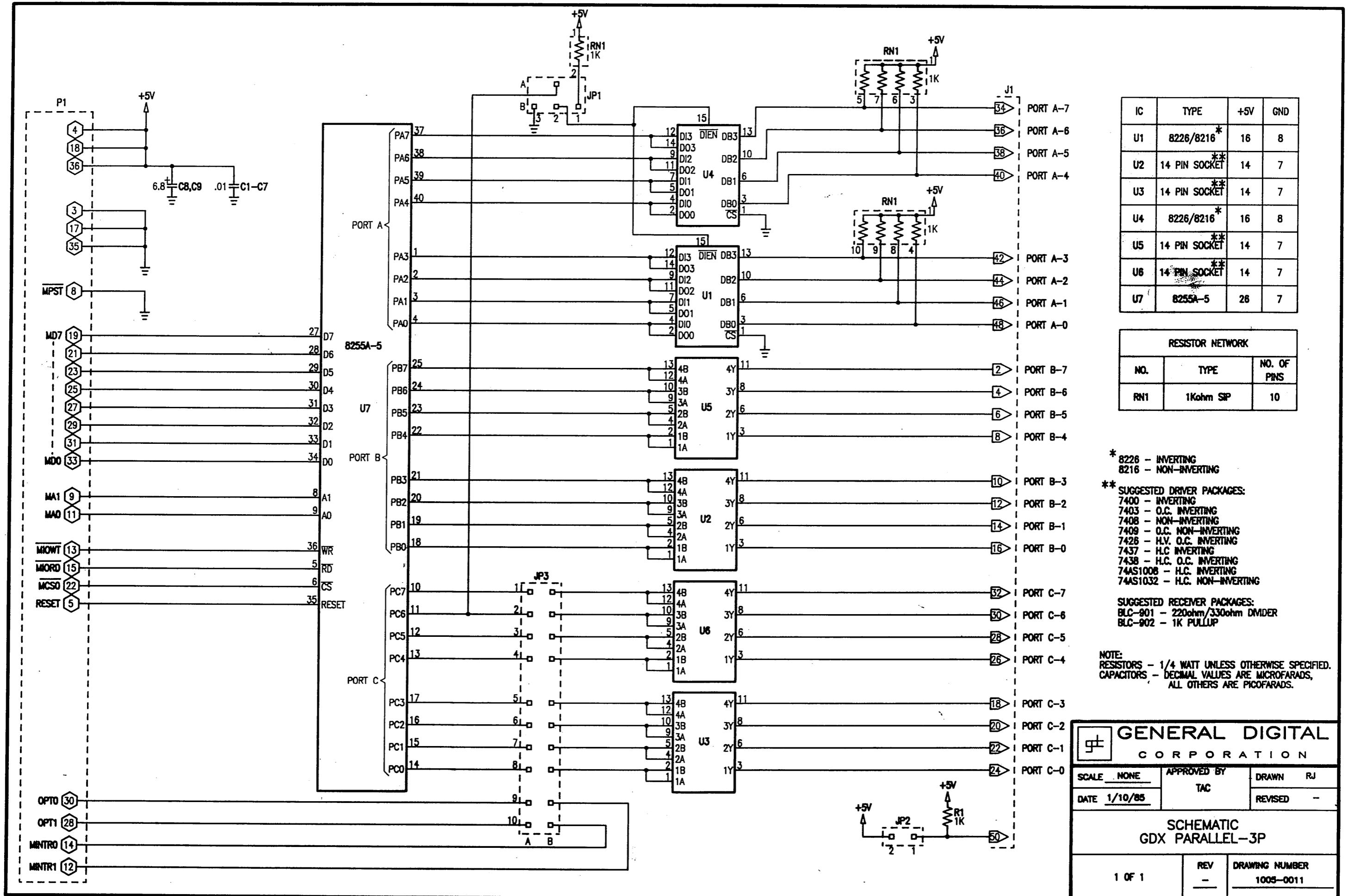


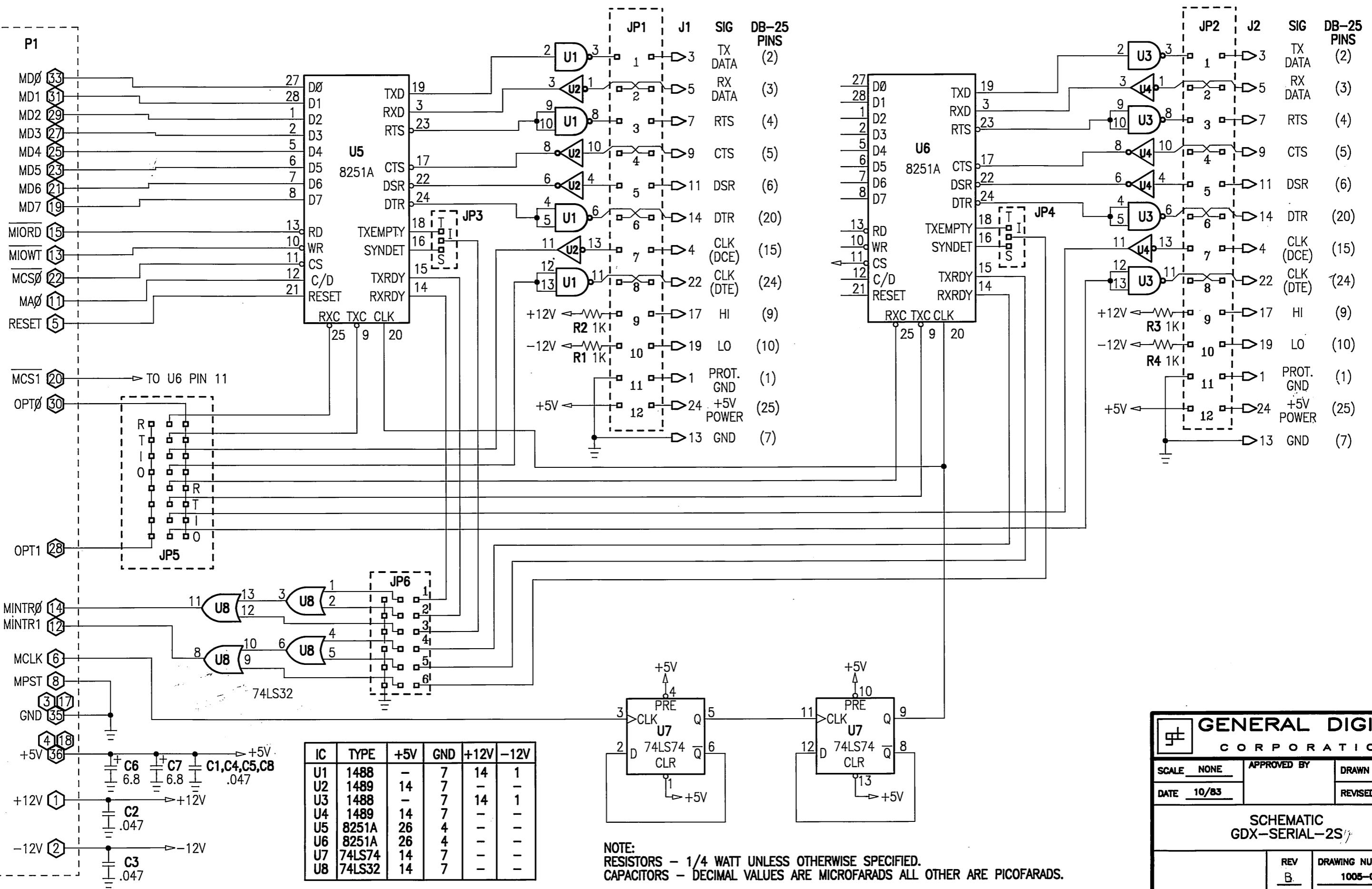
			CARROLL Mfg Co. Champaign, IL		
			DES BY	DATE	TITLE
			JL		
			DRN BY	DATE	
			J. HARDETT	9/72	
A	DEC 12 78		PC B# 51158001	TOUCH INPUT SYSTEM MOD: TPGD/12X20	
REV	DATE		DESCRIPTION 'X' AND 'Y' PHOTO TRANSISTOR AND LED SYSTEM		
			DWG NO SCH 51158001		



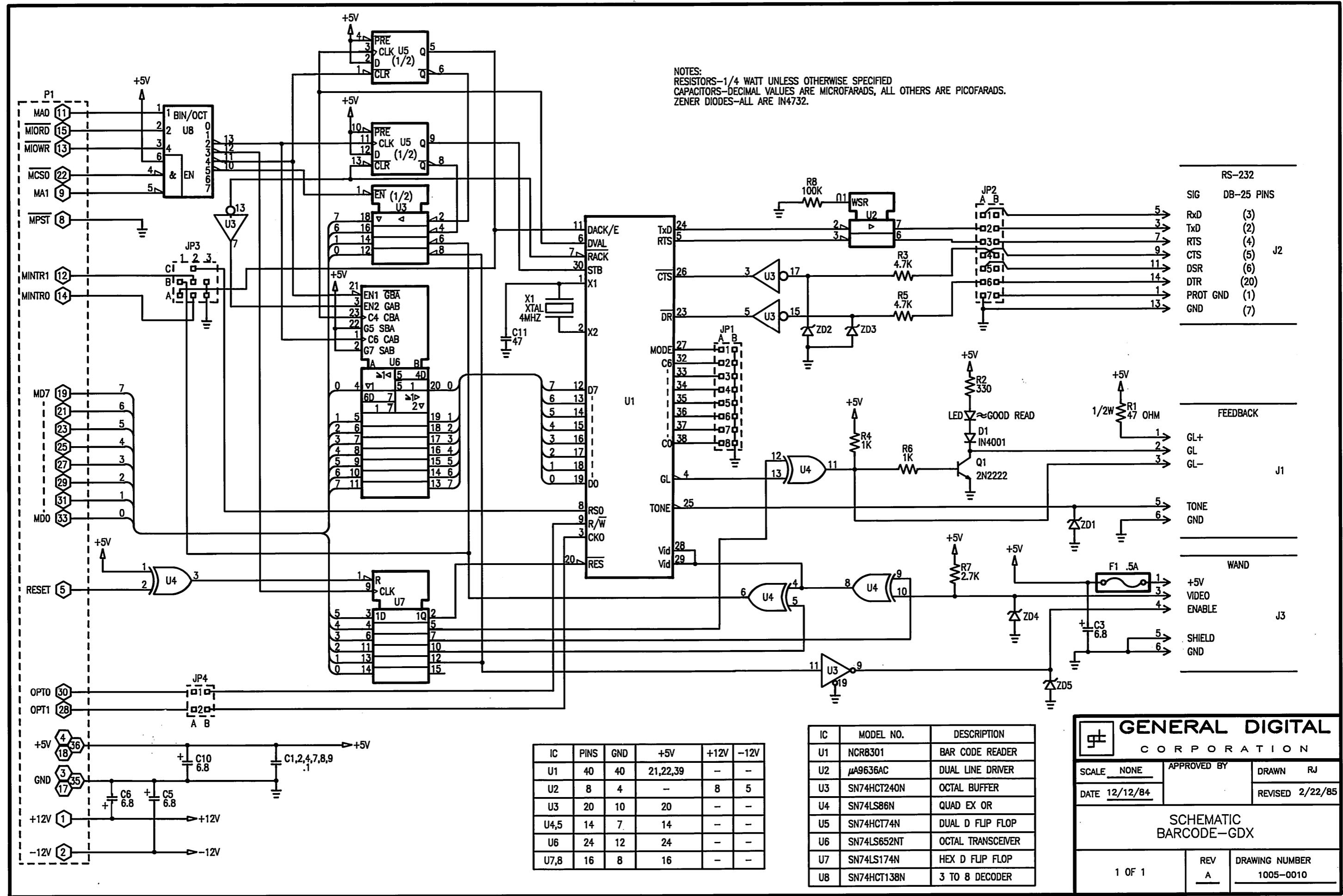


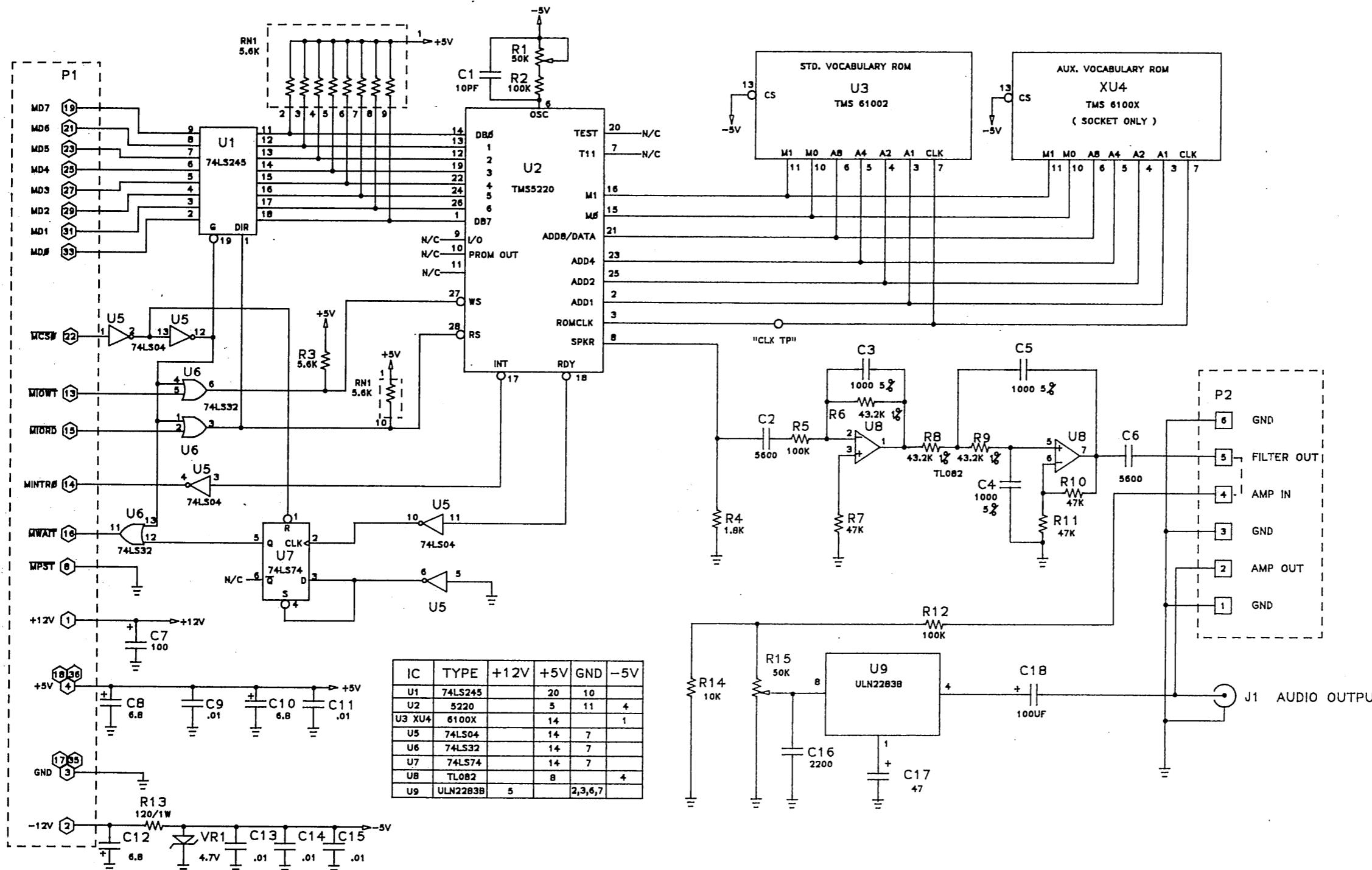
GENERAL DIGITAL CORPORATION		
SCALE <u>NONE</u>	APPROVED BY <u>T.A.C.</u>	DRAWN <u>D.B.R.</u>
DATE <u>1/85</u>		REVISED <u>-</u>
SCHEMATIC GDX-SERIAL-1E		
2 OF 2	REV <u>A</u>	DRAWING NUMBER <u>1005-0007</u>





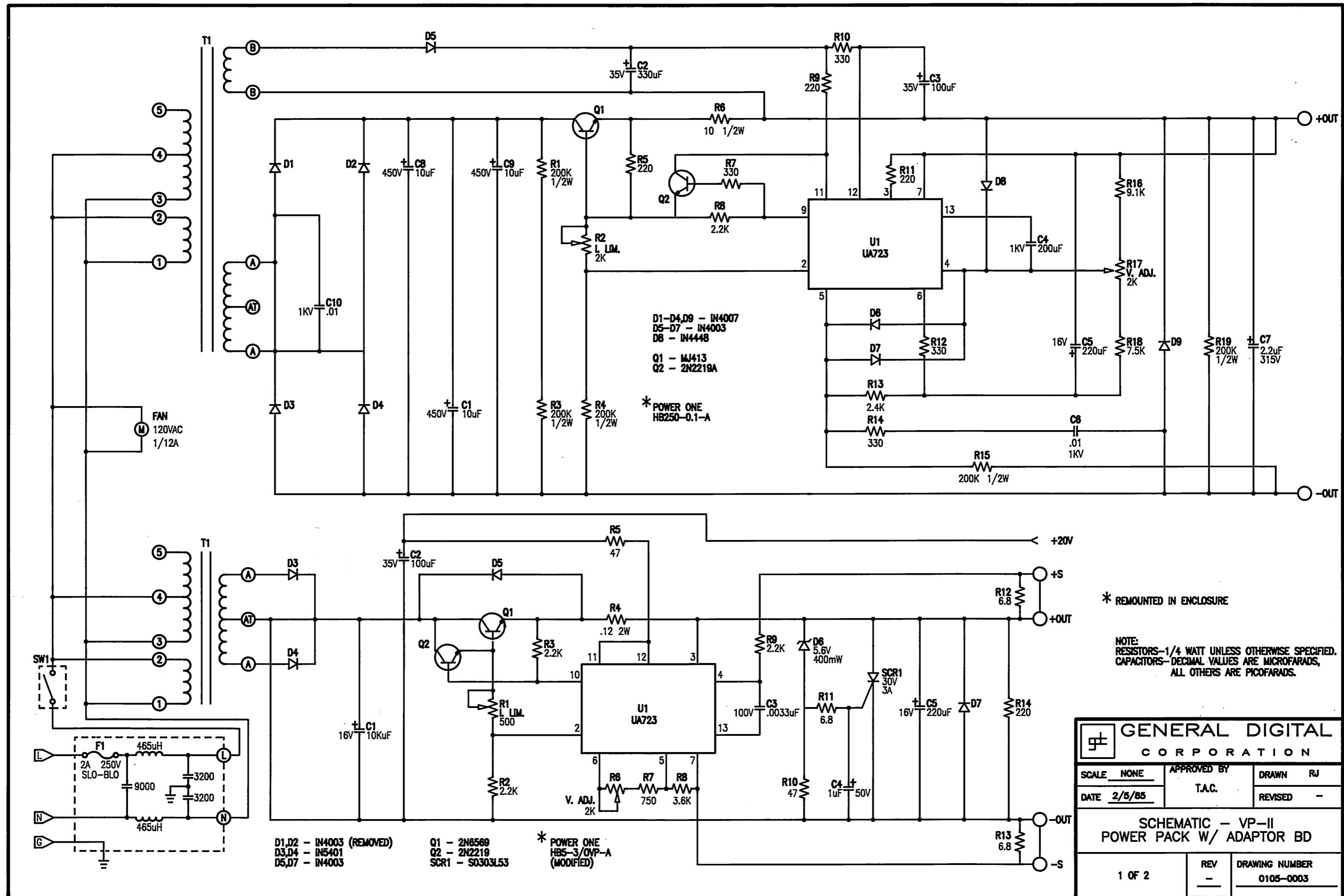
GENERAL DIGITAL	
CORPORATION	
SCALE <u>NONE</u>	APPROVED BY <u>Marcin</u>
DATE <u>10/83</u>	REVISED <u>3/88</u>
SCHEMATIC	
GDX-SERIAL-2S	
REV <u>B</u>	DRAWING NUMBER <u>1005-0002</u>

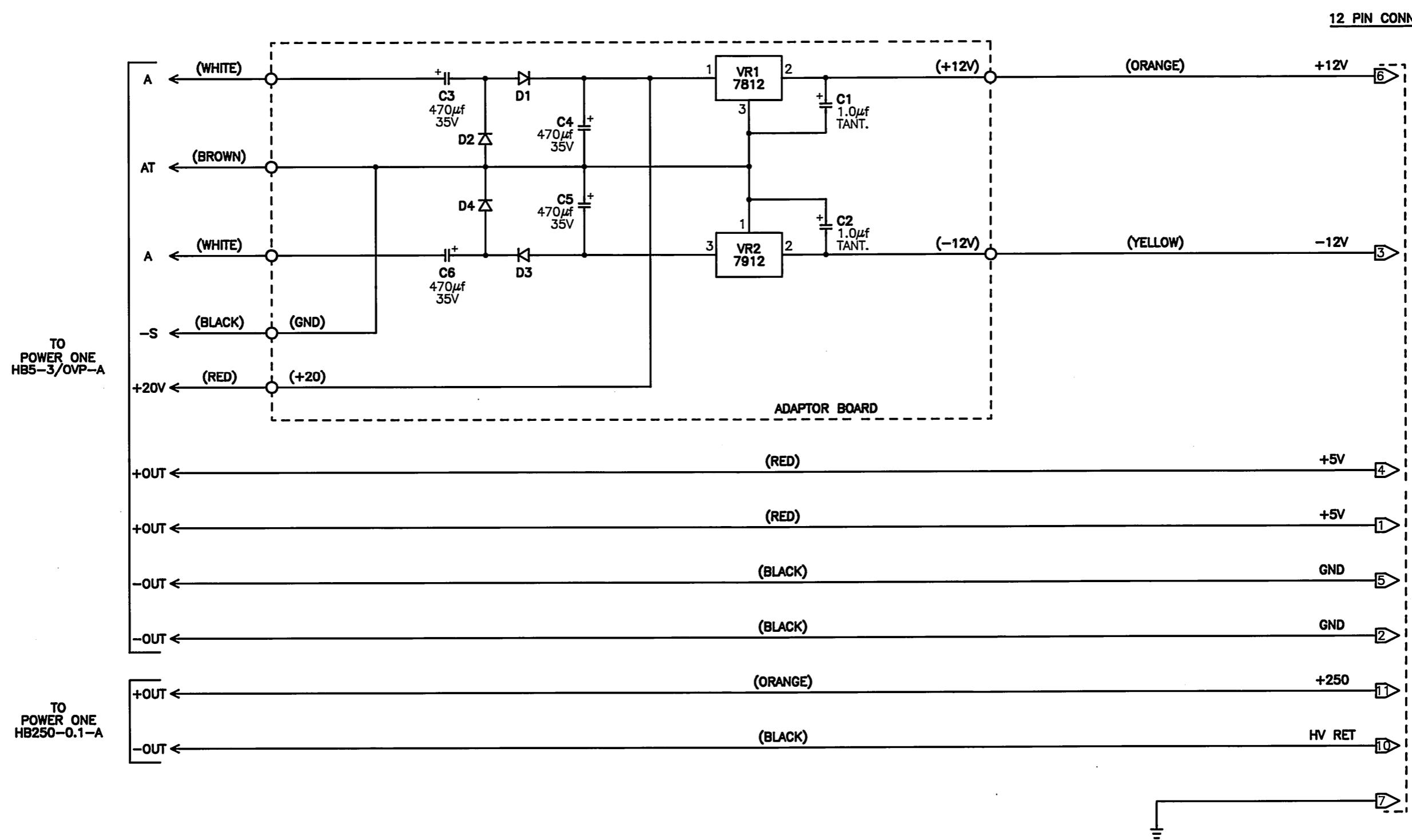




NOTE:
RESISTORS - 1/4 WATT UNLESS OTHERWISE SPECIFIED.
CAPACITORS - DECIMAL VALUES ARE MICROFARADS ALL OTHER ARE PICOFARADS.

	GENERAL DIGITAL CORPORATION	
SCALE: NONE	APPROVED BY	DRAWN BY R MARCIN
DATE: 5/1/83	R REISS	
GDX SPEECH-TI		
		DRAWING NUMBER 1005-0001





12 PIN CONNECTOR

TO
POWER ONE
HB5-3/OVP-A

**TO
POWER ONE
HB250-0.1-A**



GENERAL DIGITAL CORPORATION

SCALE _____

<u>NONE</u>	<u>APPROVED BY</u>	<u>DRAWN</u>	<u>RJ</u>
1/1/85	T.A.C.	REVISED	-

1

SOUTHLANDS 102-4

1

SCHEMATIC - VP-II
WIRE DIAGNOSTIC BOARD

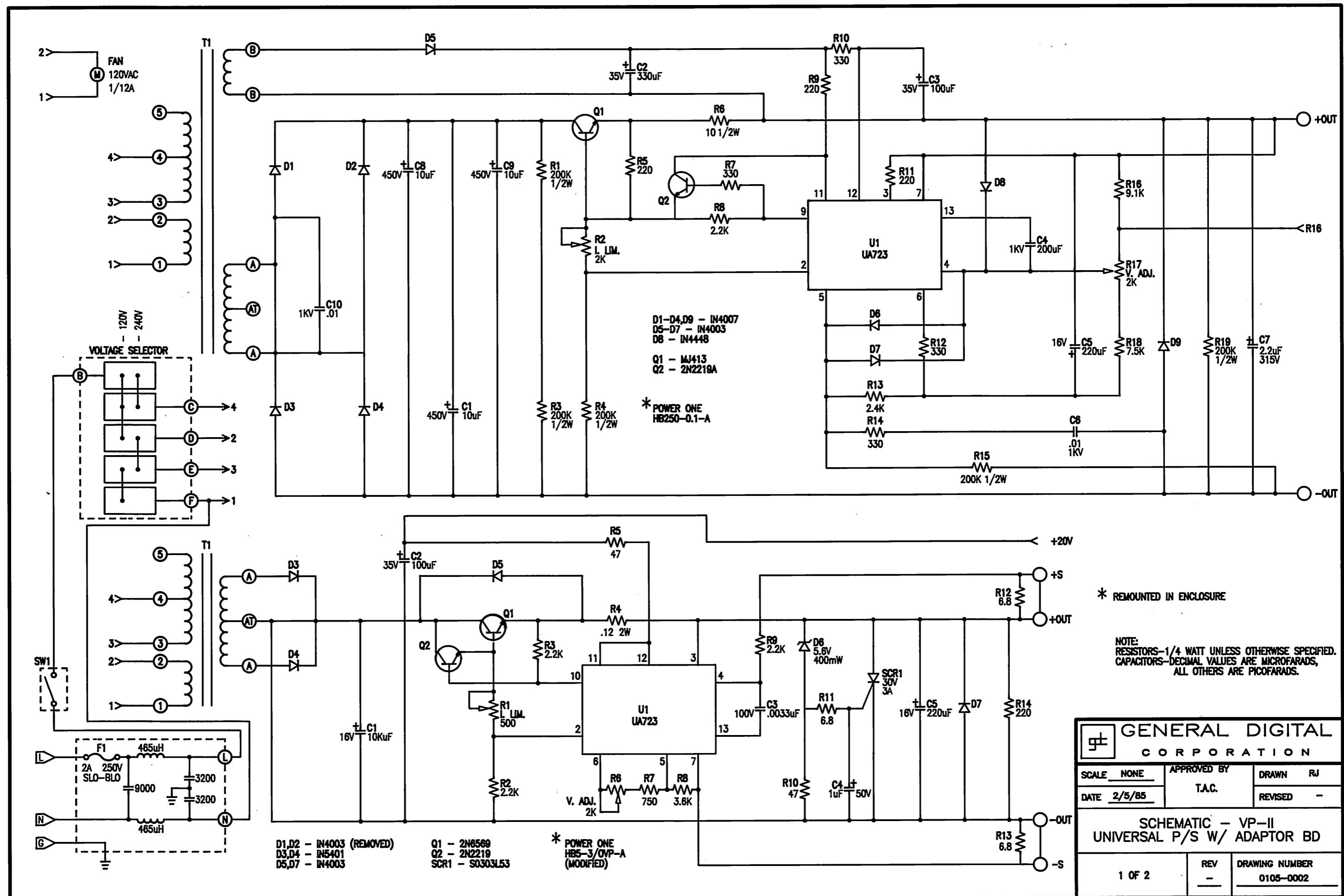
P0

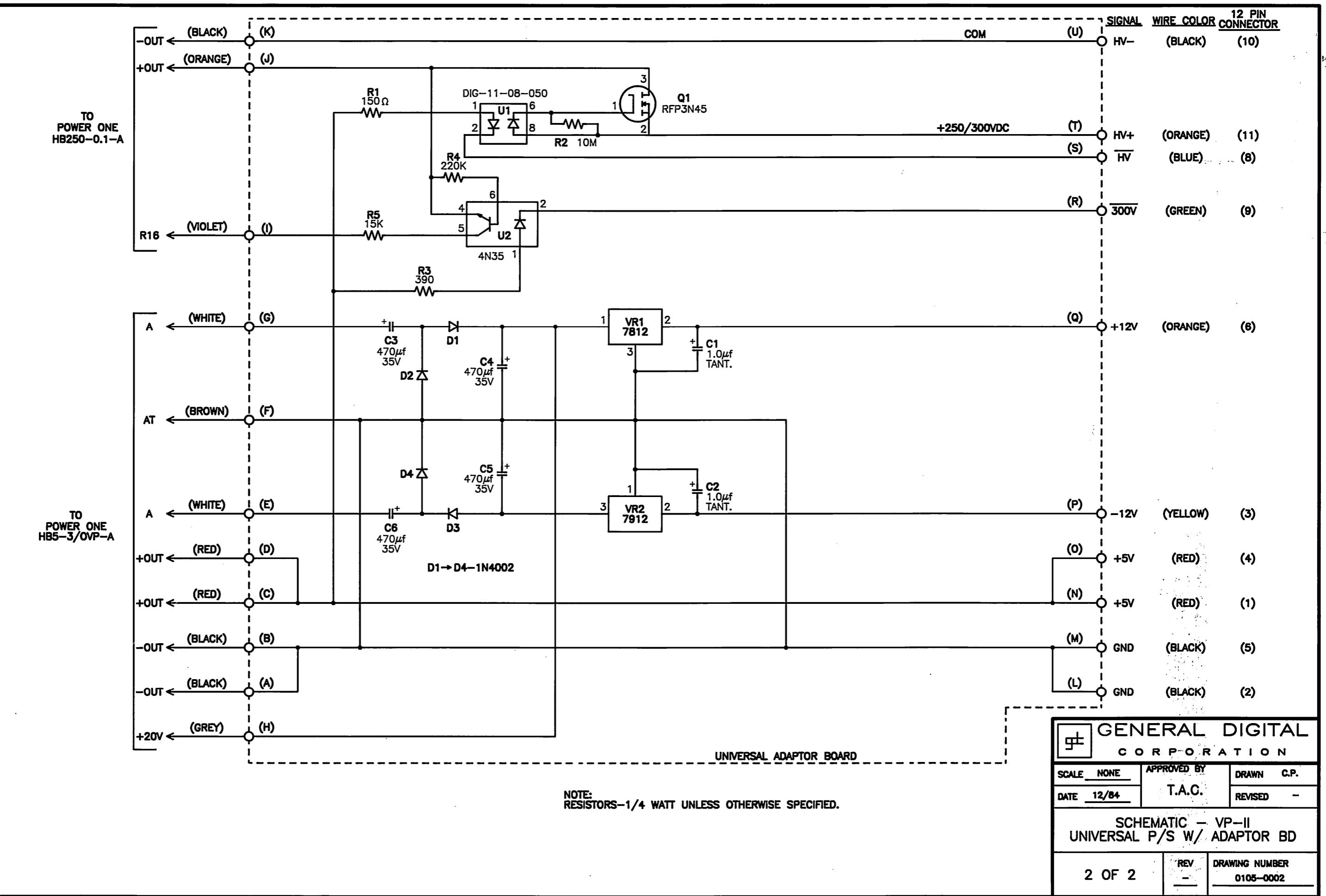
POWER PACK W/ ADAPTER BD

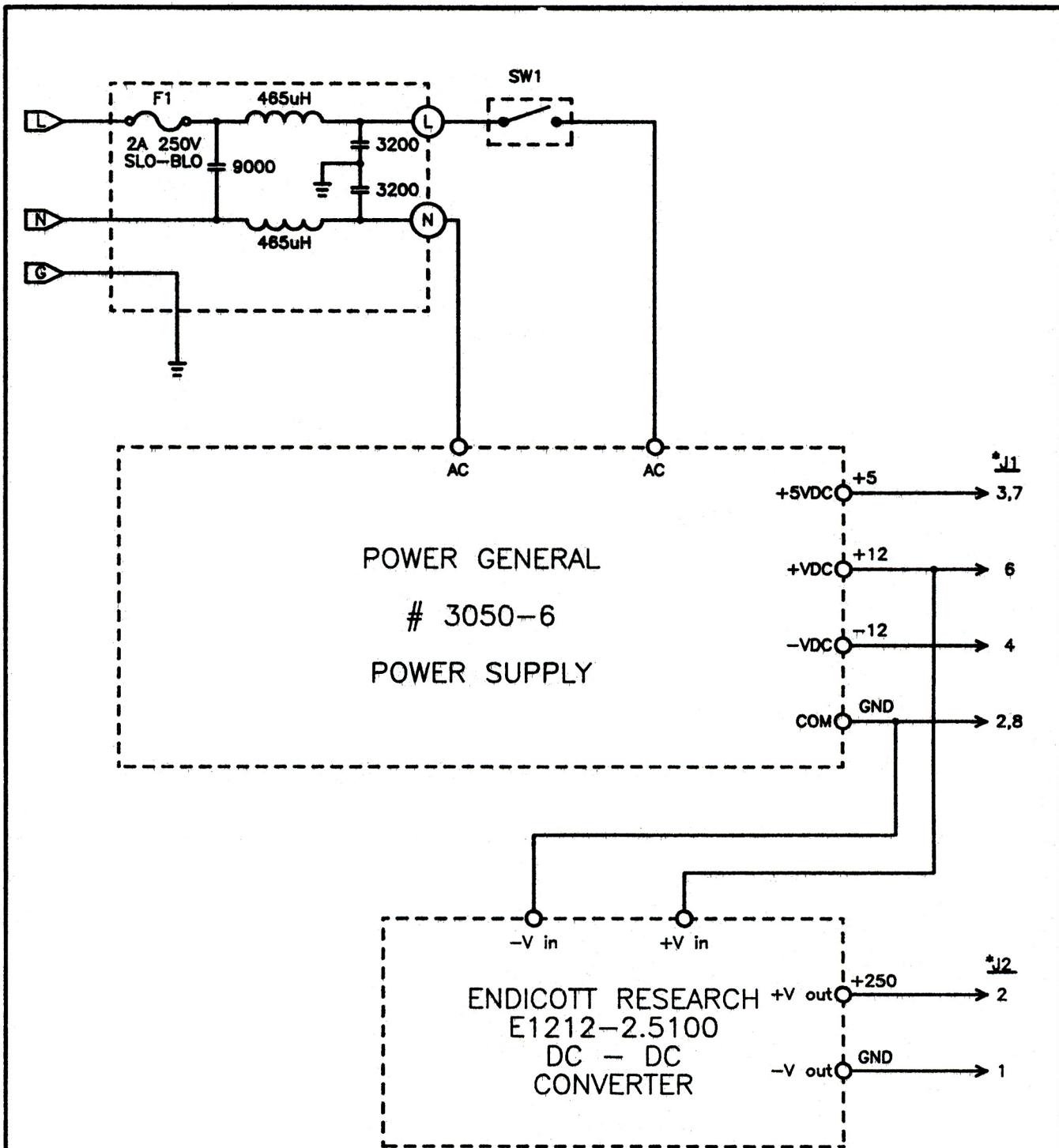
2

REV DRAWING NUMBER
= 0105-0003

**SCHEMATIC - VP-II
POWER PACK W/ ADAPTOR BD**





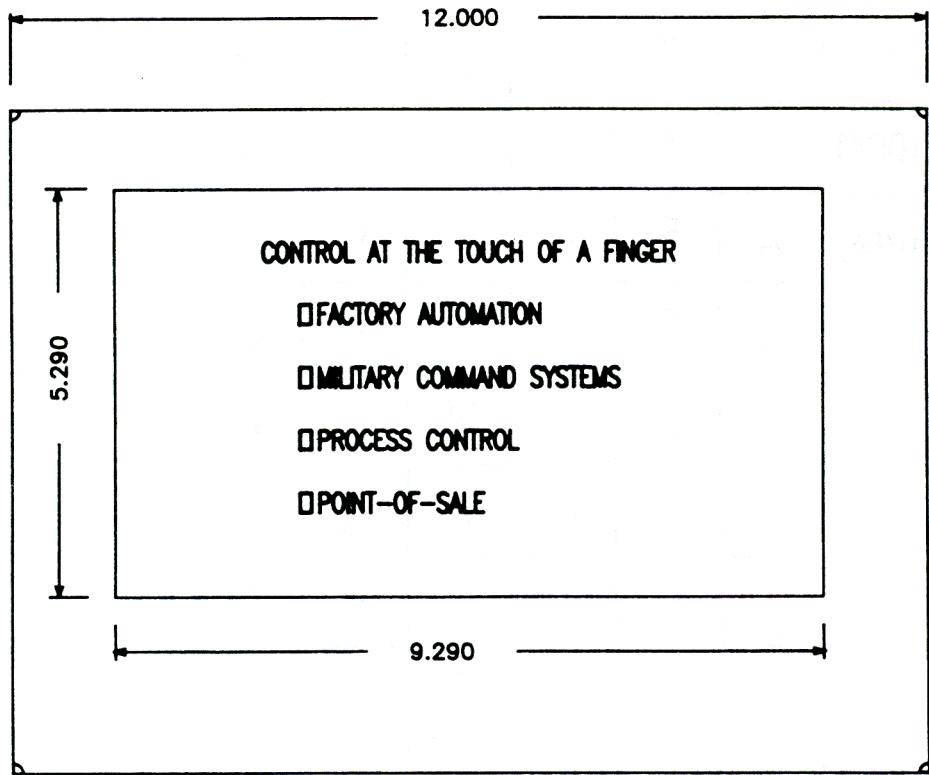


*(J1) 9 Pin conn. mates with 7 Pin conn. on VPII CPU Board, (J1).

*(J2) 3 Pin conn. mates with VPII Plasma Controller Board, (J1).

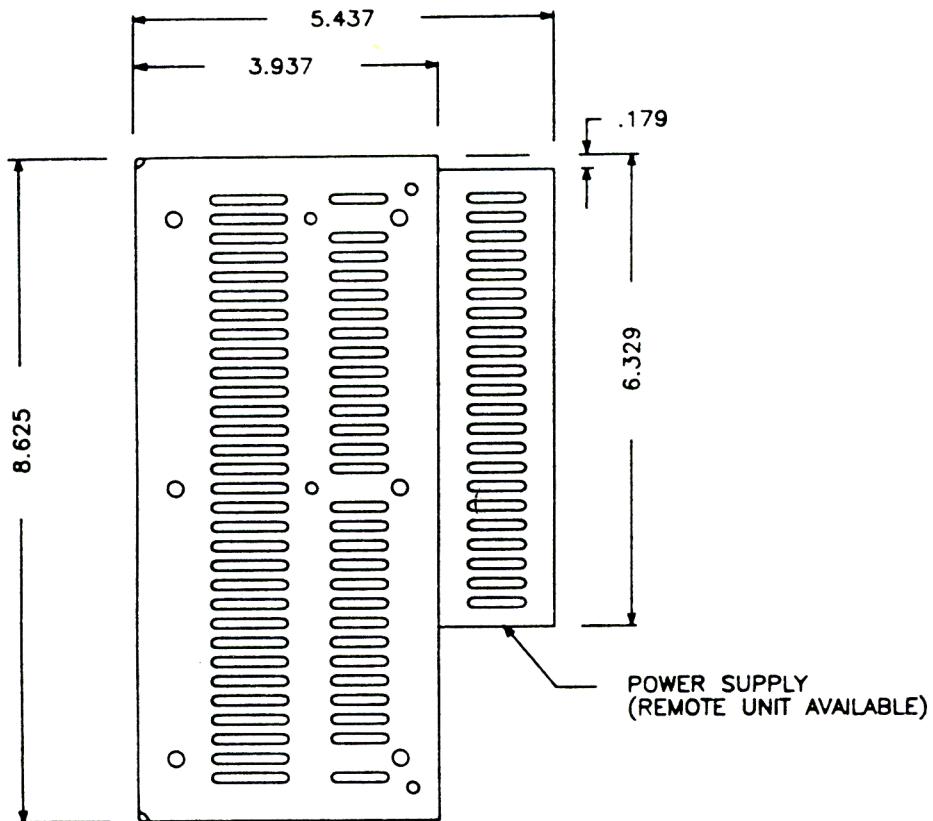
GENERAL DIGITAL CORPORATION	
SCALE <u>NONE</u>	APPROVED BY <u>T. A. C.</u>
DATE <u>1/17/86</u>	DRAWN <u>RM</u> REVISED <u>-</u>
SCHEMATIC VPII EMBEDDED POWER SUPPLY	
REV <u>-</u>	DRAWING NUMBER <u>0105-0005</u>

4.1 VuePoint II Case – Front View



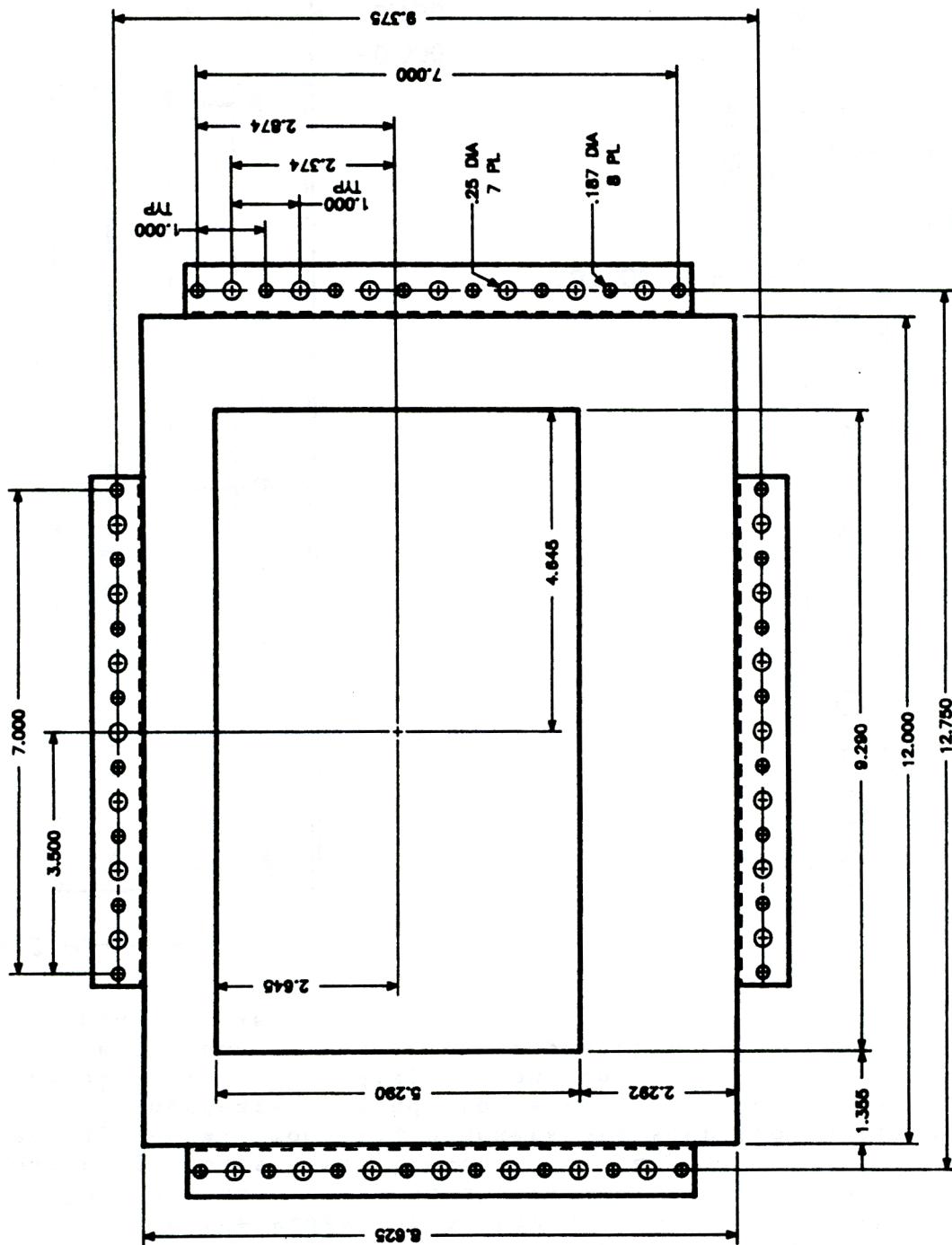
**VUEPOINT II CASE DIMENSIONS
(FRONT VIEW)**

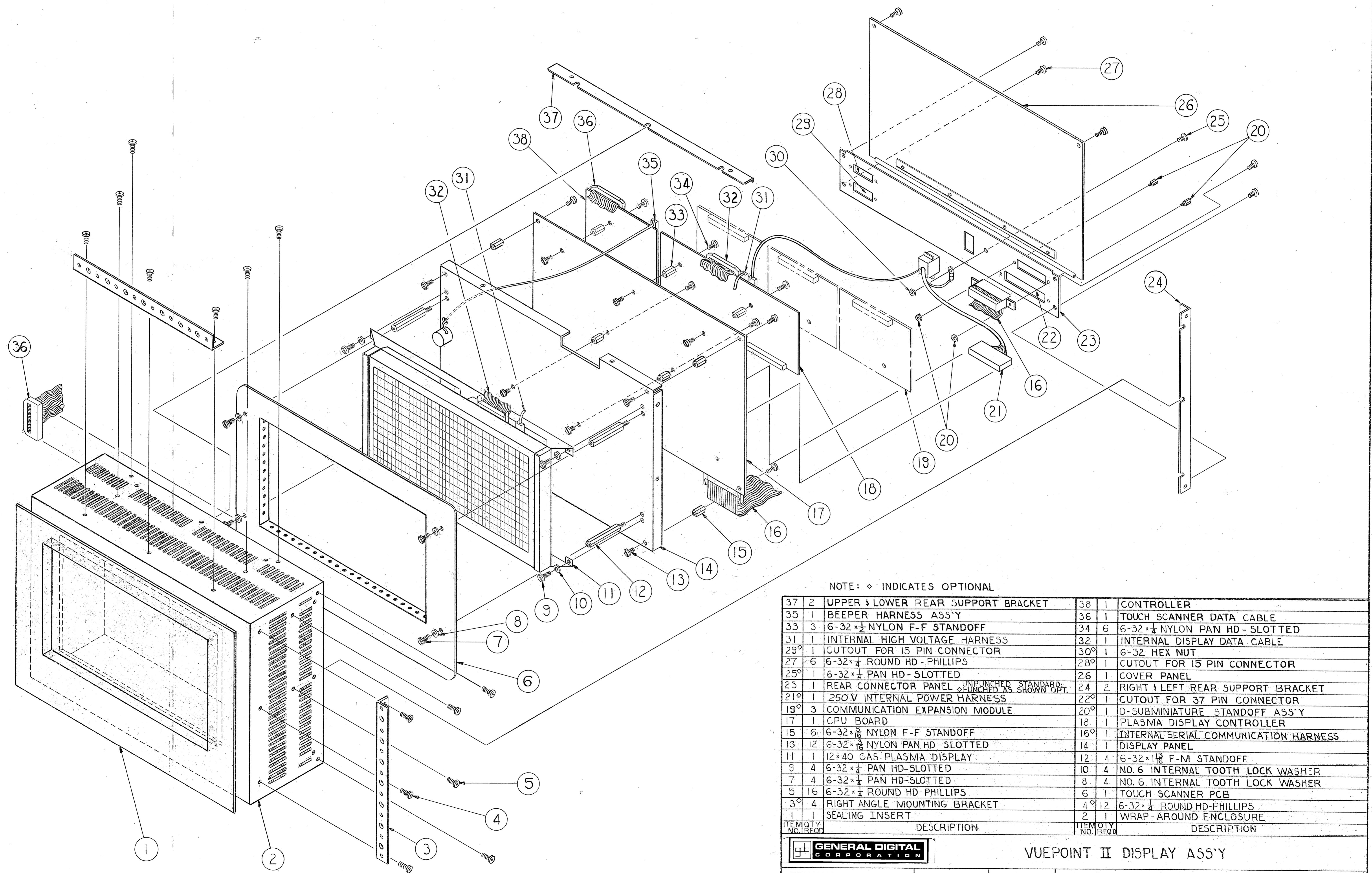
4.2 VuePoint II Case – Side View

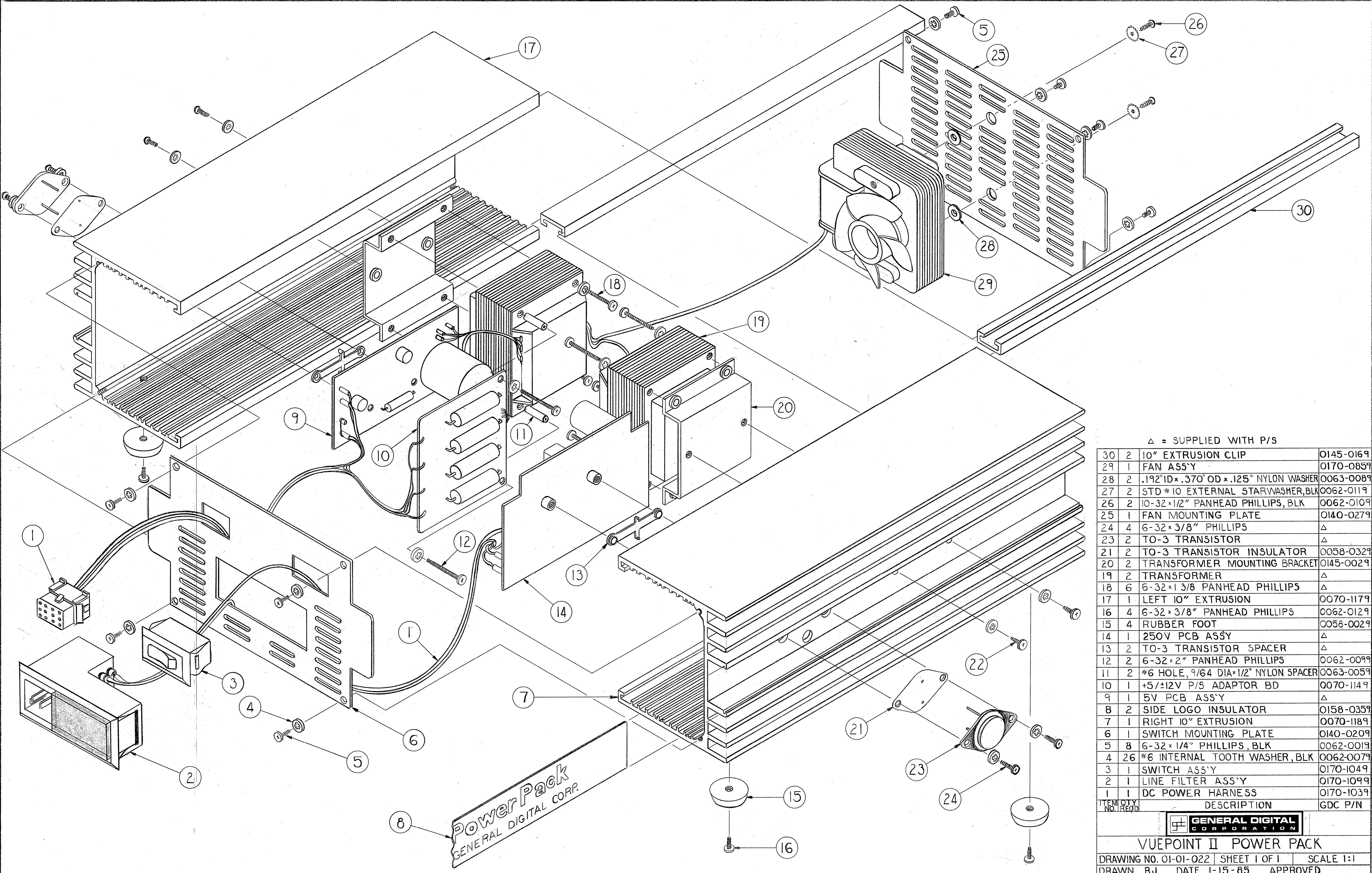


**VUEPOINT II CASE DIMENSIONS
(SIDE VIEW WITH EMBEDDED POWER SUPPLY)**

4.3 VuePoint II Case – Front View with Mounting Brackets







5.0 Contact Information

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We want you to be completely satisfied with your product. Please feel welcome to contact us should you require any of our services.

General Digital™ Corporation
8 Nutmeg Road South
South Windsor, CT 06074

Phone: 860.282.2900
Toll-Free: 800.952.2535
Fax: 860.282.2244

Hours: Monday–Friday, 9:00 A.M.–5:00 P.M. EST

Web: <http://www.GeneralDigital.com/>

Sales

Phone: 860.282.2900, Option 1
Fax: 860.282.2244
E-mail: gd_mn@GeneralDigital.com

Service

Phone: 860.282.2900, Option 4
Fax: 860.282.0198
E-mail: service@GeneralDigital.com

In your correspondence with the Service Department,
please provide the following information:

- Company name
- Company address
- Contact name
- Contact phone and fax numbers

You can expect to receive a reply within one business day.

A.1 Display

- High Brightness (55 fL unfiltered) Gas Plasma Panel with 4.6" H x 8.3" W (117 mm x 211 mm) Viewing Area
- 480 Characters (12 Rows by 40 Columns)
- 5 x 7 Character Matrix with a Character size of 0.26" H (6.6mm) x 0.15" W (3.7mm)
- Wide 120° Viewing Angle

A.2 Operator Interface

- 12 x 20 Resolution Infrared Touch Scanner with Audible Touch Input Feedback
- Visual Touch Input Feedback Signal
- Optional ASCII Keyboard Input
- Optional Barcode Wand Input
- Optional Printer Output

A.3 Functions

- Power-on Setup for Key Operating Parameters
- Software Character Set Selection
- Scroll or Block Data Formats, with Field Protection
- Software Cursor Control and Enable/Disable
- 3 Display Pages Standard; Expandable to Over 527 Pages
- Choice of RAM, Battery-Backed RAM, and EPROM for Display Page Memory
- Independent Page Editing and Display
- Page to Page Copy and Merge
- Software Touch Enable/Disable, for All or Selected Areas
- Programmable Character Intensity and Blink Rate

A.4 Communications

- EIA RS-232C Full Duplex Standard; Options for RS-422A and 20mA Current Loop Operation
- Rates from 300 to 19,200 Baud
- Selectable XON/XOFF Handshaking
- Selectable Parity, Number of Data Bits, and Number of Stop Bits
- Optional Extended Serial Module for RS-232C, RS-422A, and 20mA Current Loop Operation
- Optional Parallel Communications Module

A.5 Physical

- Protective Enclosure with Available Rack Mount Front Panel or Right Angle Mounting Brackets
- Protective Display Shield Provided to Minimize Liquid and Dust Contamination
- 8.625" H x 12.0" W x 4.0" D (219mm x 305mm x 101mm)
- Operating Weight: 7.0 Pounds (3.2 kg)

A.6 Electrical

- +5 VDC @ 2.5 A max.
- ±12 VDC @ 0.050 A max.
- +250 VDC @ 0.100 A max.
- Choice of Optional Internal or External Power Supplies, or Power from User's Equipment

A.7 Environmental

- Operating Temperature: 0 to 50 Degrees Centigrade
- Storage Temperature: -20 to 70 Degrees Centigrade
- Relative Humidity: 0% to 95%, Non-condensing