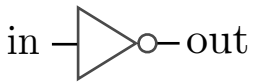
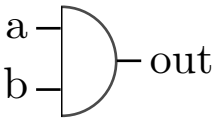
## NOT




out = ¬in [in logic]
= $\overline{\text{in}}$ [in logic]
= ∼ in [in C]
<= not(in) [in vhdl]

| in | out |
|---|---|
| 1 | 0 |
| 0 | 1 |

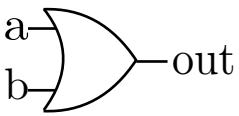
## AND




out = a&b [in logic, C]
<= a and b [in VHDL]

| a | b | out |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

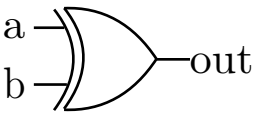
## OR




out = a|b [in logic, C]
<= a or b [in VHDL]

| a | b | out |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

## XOR




out = a ⊕ b [in logic]
= a^b [in C]
<= a xor b [in VHDL]

| a | b | out |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |