EL318: Lecture 2-2

The Pentium 4

A very quick and superficial look at the complexity of a modern processor

Beyond Pentium Pro, PIII

Pentium Pro, PIII	Pentium 4
10 stage pipe	20 stage pipe
256 entry branch target buffer	4k entry branch target buffer Reduced misses 33%
Single speed ALU	Double speed ALU Up to 4.4GHz
Originally, L2 off chip	256/512k 8-way associative L2 cache on chip 42M/55M (0.13µm) transistors 146/217mm² die

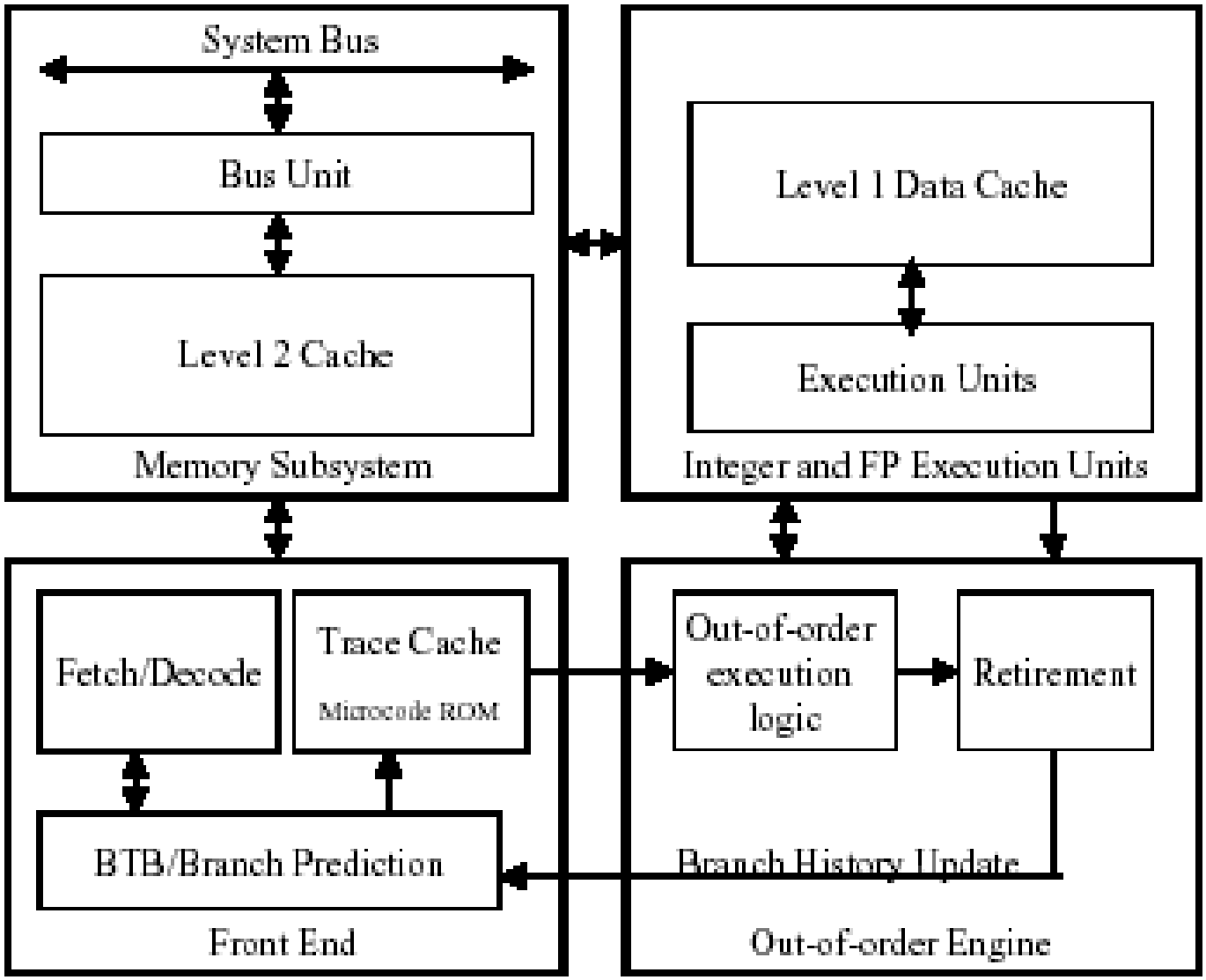
Net Burst Microarchitecture

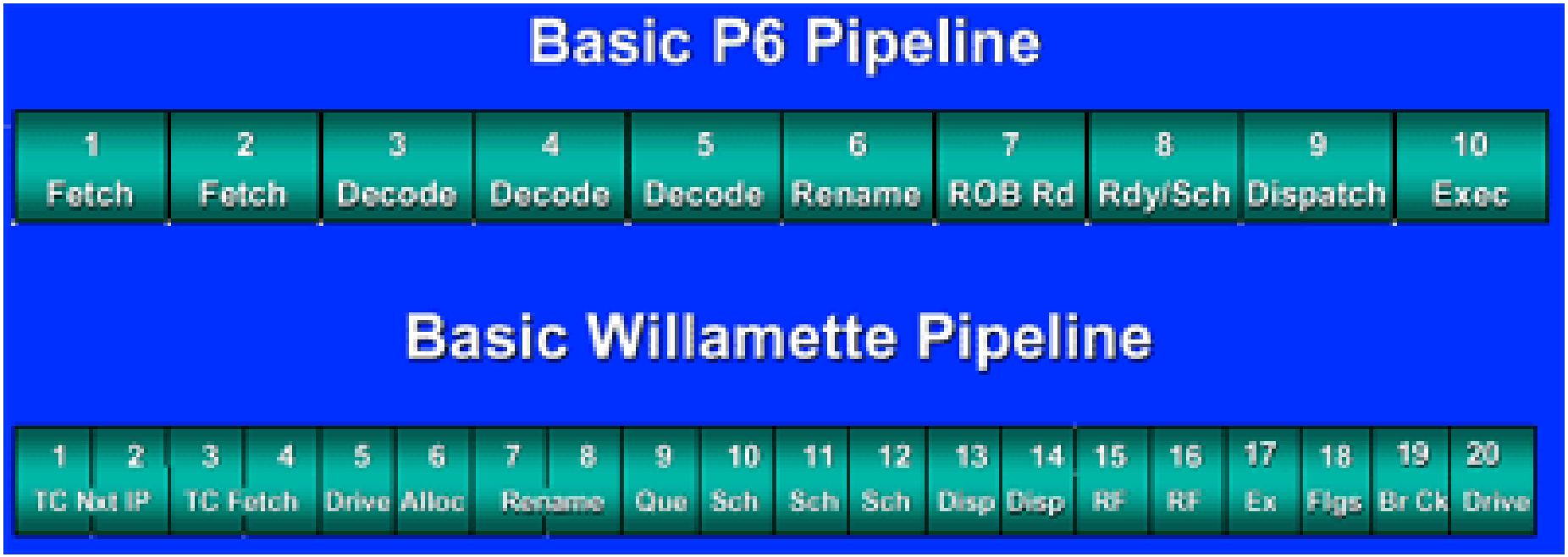
- 20 stage pipe
- 126 instruction out-of-order window (up from 42)
- 400MHz 64bit Front Side Bus (up from 133MHz)
- L1 cache halved to 8k, but latency reduced.
- Execution Trace Cache: An Instruction cache for decoded instructions. It allows branch prediction errors to recover at the micro-op level, rather than at x86 instruction level.

NetBurst pipelining

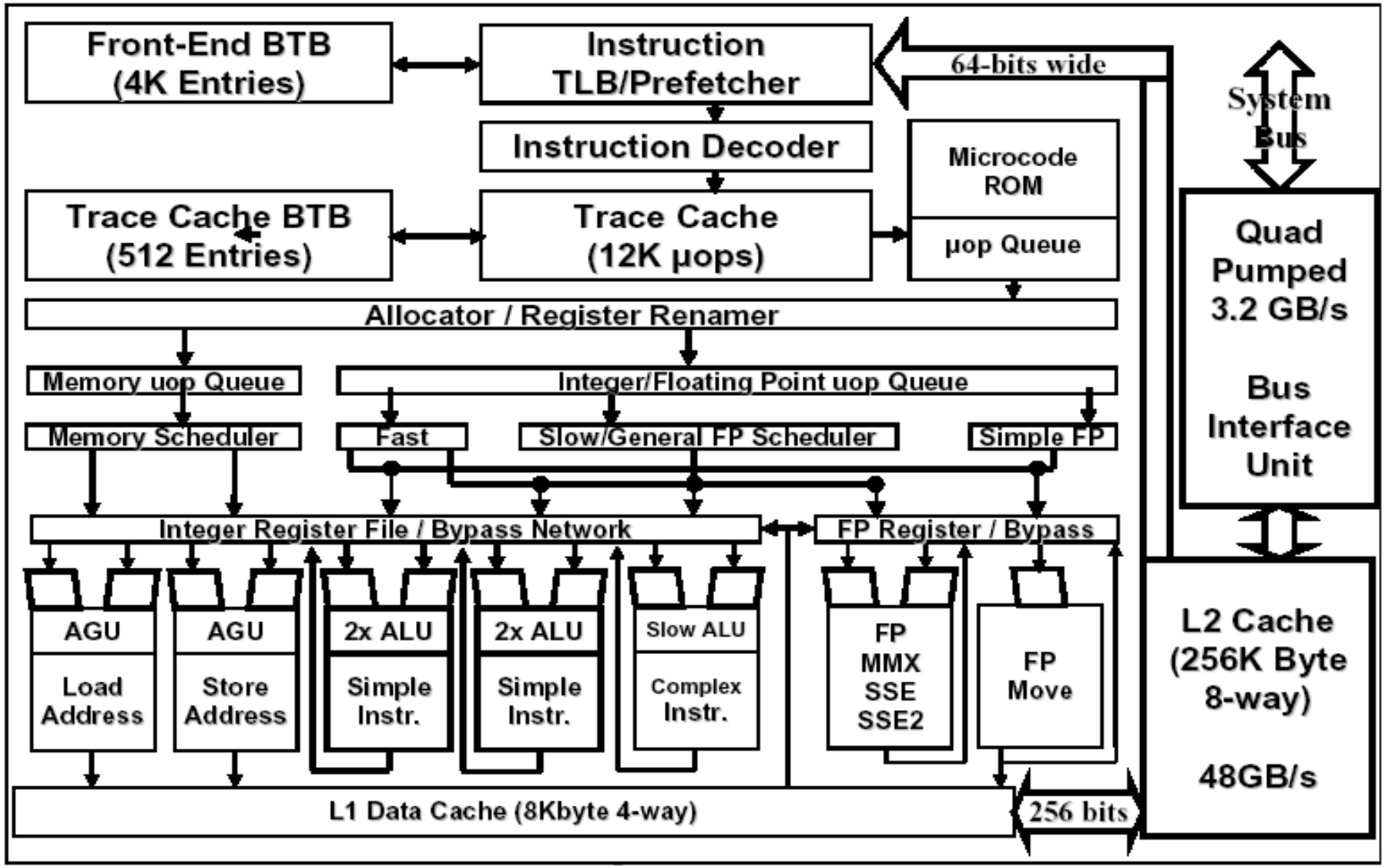
There are effectively three pipelines for instruction execution:

- The instruction decoder pipeline, with a branch predictor working at the iA32 instruction level.
- The µOP execution pipeline, with its own branch predictor, working on trace cache addresses.
- The scheduler pipeline within each functional unit.

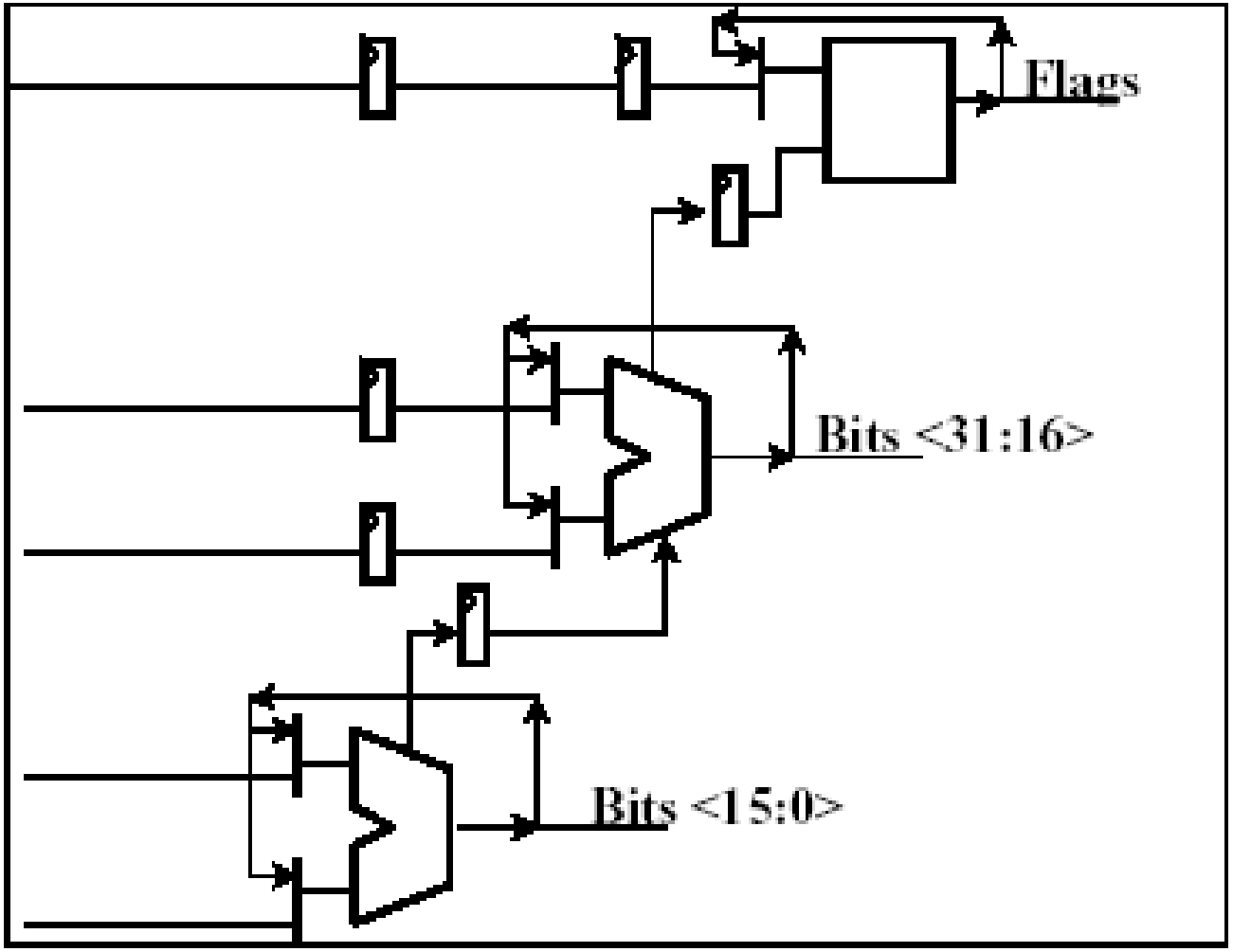




The P4 Willamette had a 20 stage pipeline; the P4 Prescott has 31 stages.



Staggered ALU Add



Execution Trace cache

- The P4 cache holds decoded µOPs.
- It caches the micro-ops in the predicted path of execution.
- Held up to 12k µOPs.
- One iA32 instruction typically becomes 1–4 µOPs.
- Complex instructions generate MROM (Microcode ROM) vectors in the cache.
- Address references in the µOPs point into the cache.
- The decoder pipeline that fills the trace cache is probably 10–30 deep.
- The trace cache has its own branch predictor, separate from the front-end branch predictor.

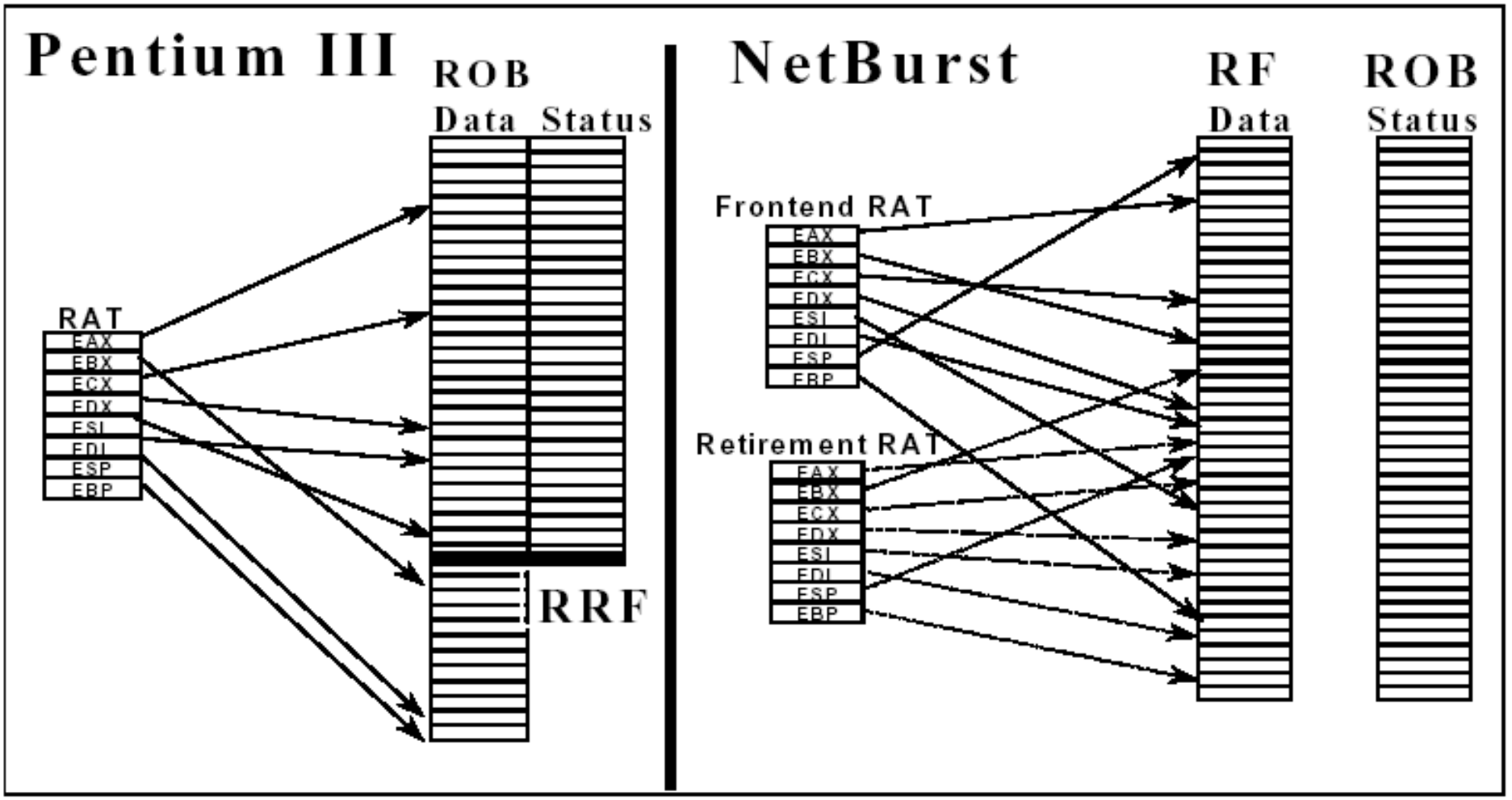
Branch Prediction

Architecture	NetBurst	Earlier Pentium Family Architecture
Size of BTB [entries]	4096	512
Return address stack size	16	16
Static prediction	Backward conditional jumps: Taken, forward conditional jumps: Not taken	Backward conditional jumps: Taken, forward conditional jumps: Not taken
Static branch hint prefixes	Yes	No
Dynamic prediction		
• Fully predicted loops	1-16 loop iterations	1-4 loop iterations
• Number of mispredictions for loops if above loop count exceeded	1 (last iteration)	2 (first and last iteration)
• Taken / Not-Taken pattern length with no misprediction	1-4	1-4
Misprediction penalty [clock cycles]	Min. 20	10-15, max. 26
Penalty for correctly predicted taken branches [clock cycles]	0	1 (for instruction fetch)
Average misprediction rate	~6%	~10%

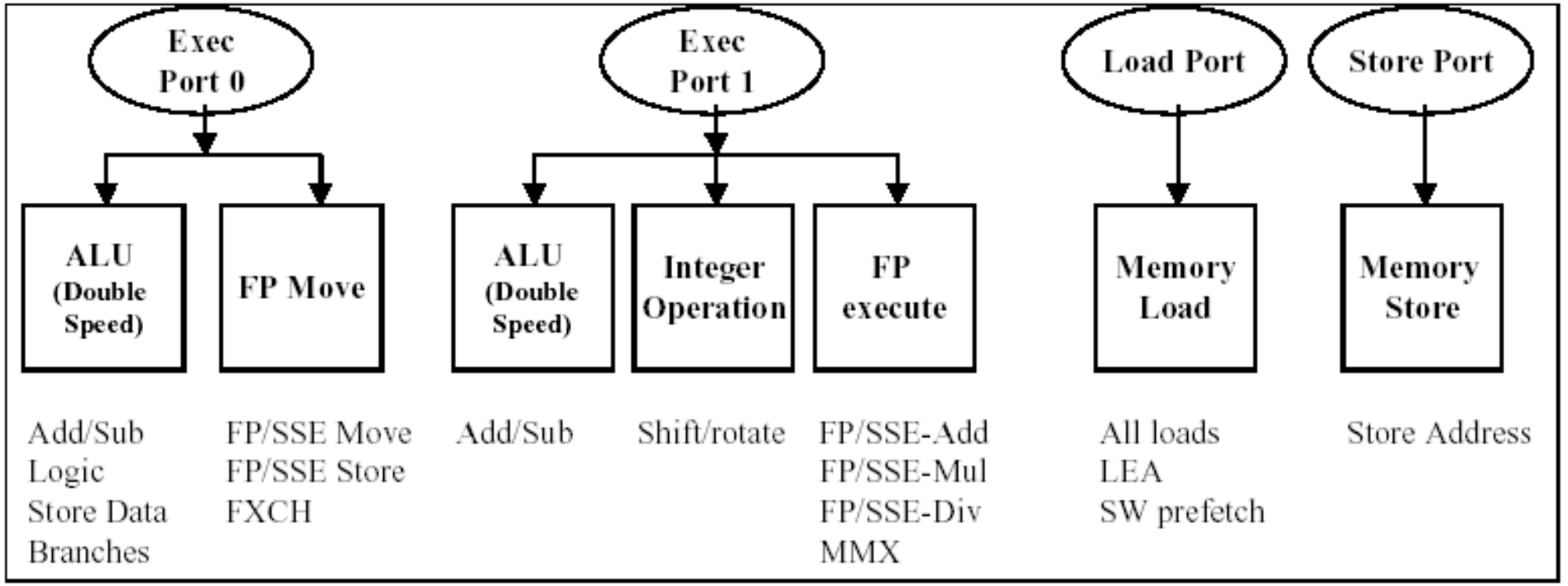
Branch Hints

- 2EH—Branch not taken (used only with *Jcc* instructions).
- 3EH—Branch taken (used only with *Jcc* instructions).

The branch hint prefixes allow a program to give a hint to the processor about the most likely code path that will be taken at a branch. These prefixes can only be used with the conditional branch instructions (*Jcc*). Use of these prefixes with other IA-32 instructions is reserved and may cause unpredictable behaviour. The branch hint prefixes were introduced in the Pentium 4 and Intel Xeon processors as part of the SSE2 extensions.



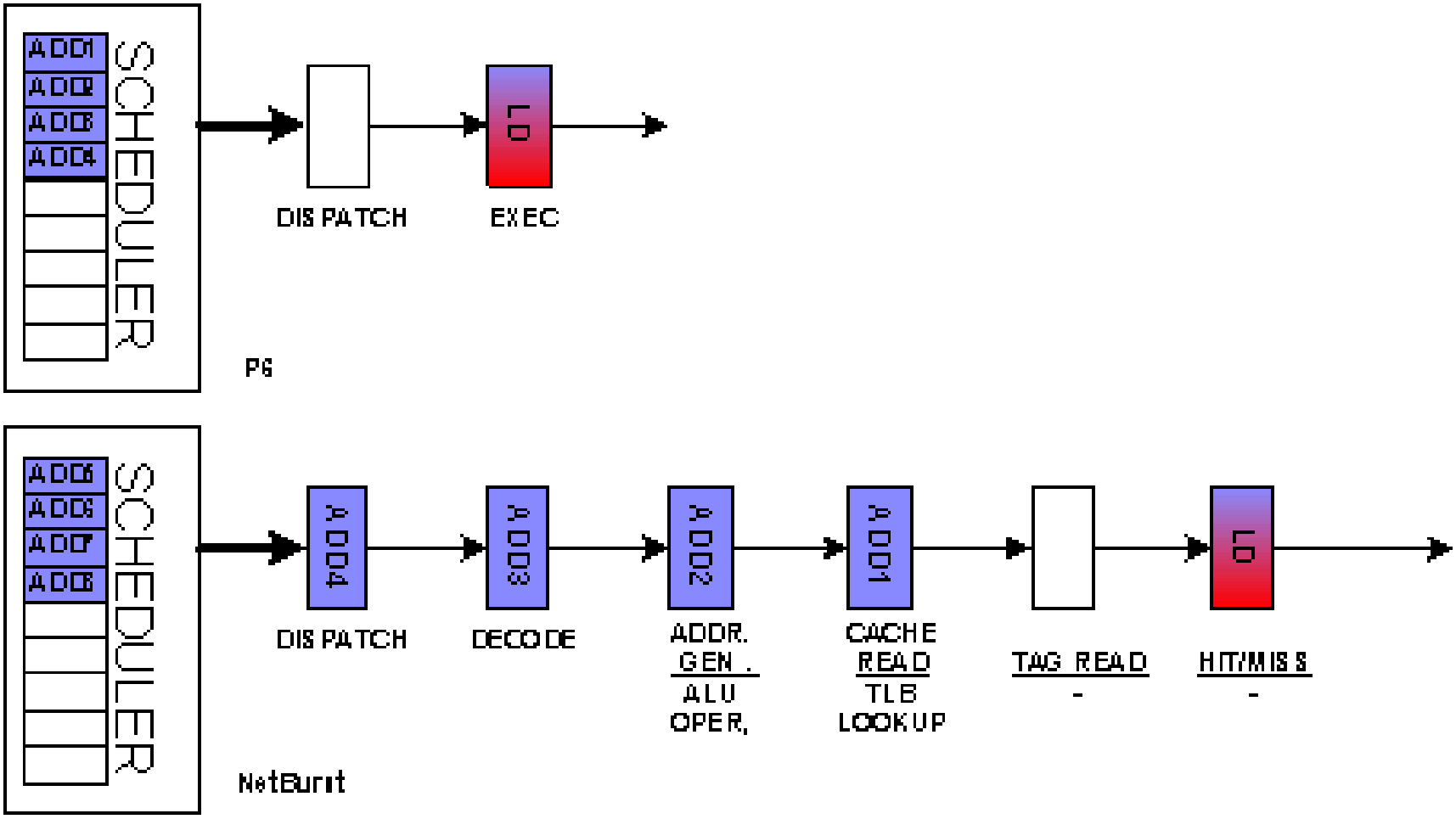
RAT = Register Alias Table, a mapping of architectural registers into the 128 internal registers.



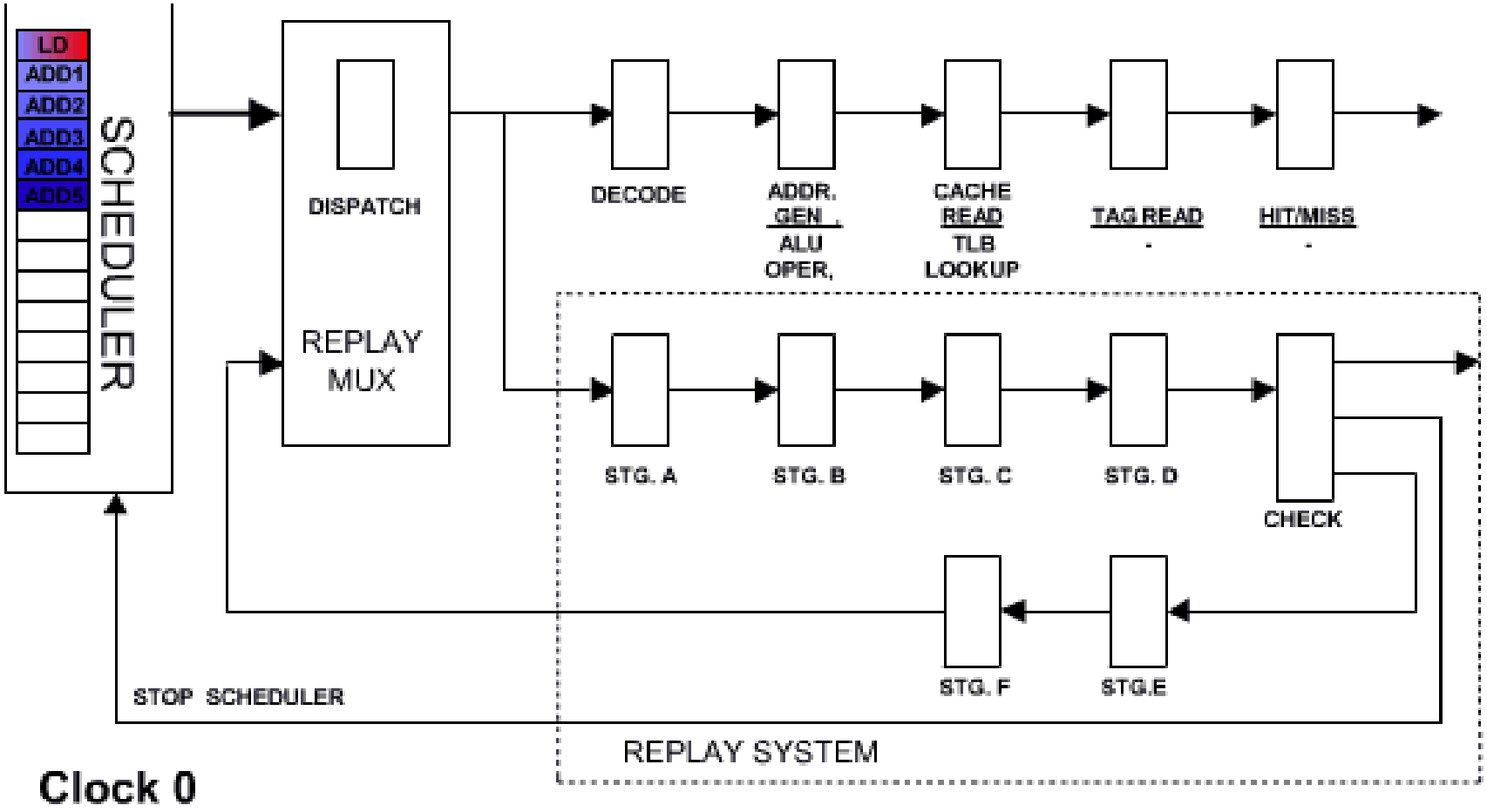
Replay problems

In order to maximize performance for the common case, the Intel NetBurst micro-architecture sometimes aggressively schedules µops for execution before all the conditions for correct execution are guaranteed to be satisfied. In the event that all of these conditions are not satisfied, µOPs must be reissued. This mechanism is called replay. Some occurrences of replays are caused by cache misses, dependence violations (for example, store forwarding problems), and unforeseen resource constraints. In normal operation, some number of replays are common and unavoidable. An excessive number of replays indicate that there is a performance problem.

[http://www.xbitlabs.com/articles/cpu/display/replay.html]

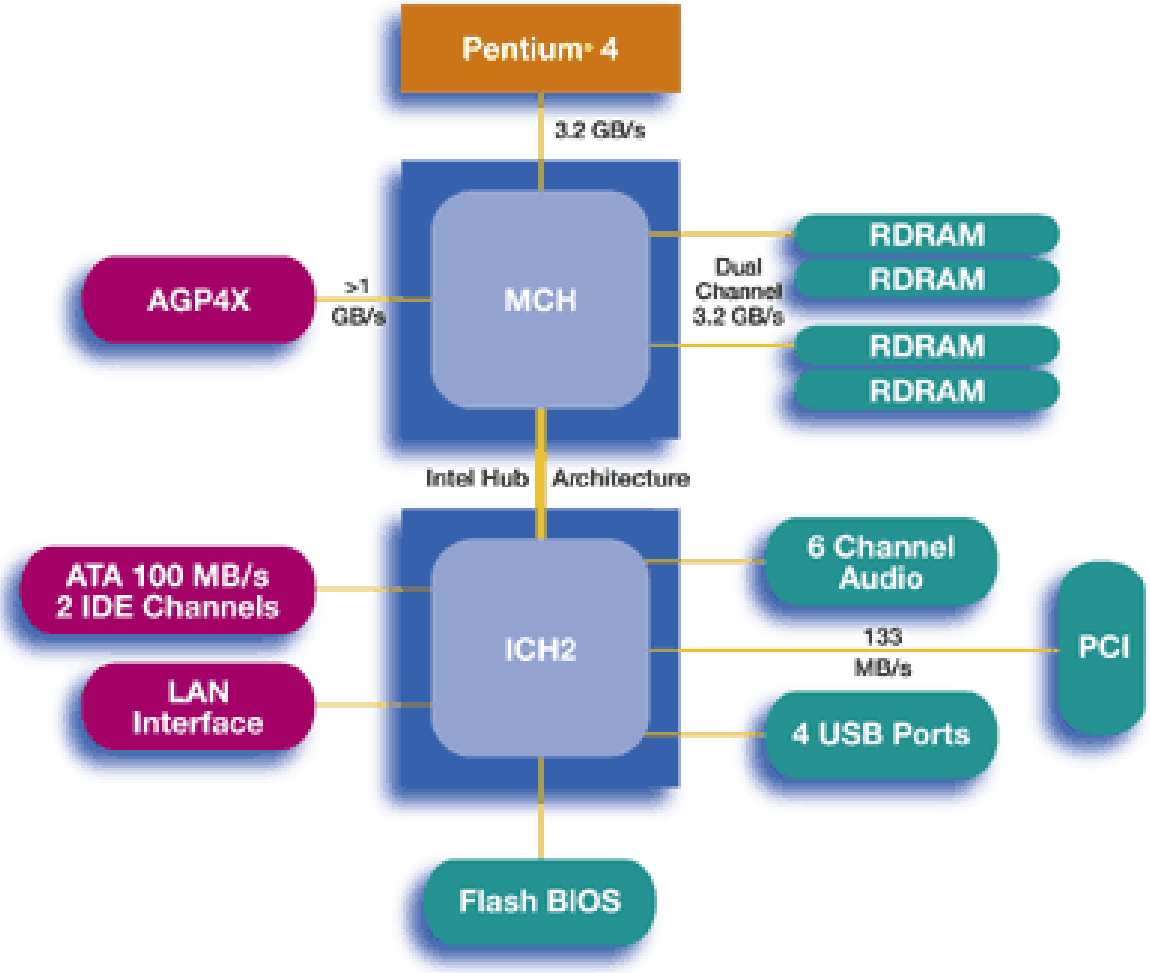


Because of the extra pipeline stages, the netBurst scheduler has to *guess* when data will be ready for execution.



A single instruction can replay multiple times.

Intel 850 chipset



Intel 845 chipset