ELEC3020: Lecture 1-1

Introduction

1.1 Why study Computer Architecture?
1.2 Why are there different Architectures?
1.3 How can we classify modern systems
1.4 Computer architecture review

Timetable

- Monday 15:00

  B6/1081 (Nuffield B)

- Friday 14:00

  B7/3027 (Lanchester F1)

Labwork session will be on a Wednesday morning.

Why study Computer Architecture?

- We will all select and use processors.
- Many of us will design systems.
- Some of us will design embedded processor applications (SoC).
- Understanding the limitations of modern architectures will aid effective use.

Why are there different Architectures?

- There continue to be rapid and exciting advances in individual designs.
- Different application domains:
  - Embedded,
  - Signal processing,
  - Workstation,
  - Supercomputer (Scientific, Cryptographic)
  - Quantum…
- *We don't need more general-purpose processors; there are too many competing vendors already. Probably only two (Intel, AMD?) will survive.*

Syllabus

- Overview of modern processor architectures.
- Processor Design
- Memory Hierarchy
  - Cache and Cache Coherence
  - Bus Architecture
- Types of parallel machine
  - Vector Pipeline Architectures
  - Replicated Architectures
  - Shared Memory and Distributed Memory
- Connectivity
  - Clusters
  - Networks
  - Routing
- Performance Comparison
- Software Issues, including
  - Dataflow
  - Virtual Concurrency
- Case Studies, e.g.
  - AMD64 Opteron
  - Linux clusters
  - Intel Core i7

Additional book

Modern Processor Design

Fundamentals of Superscalar Processors

J P Shen and M H Lipasti

McGraw-Hill Higher Education 2003

ISBN 0-7-282968

How can we classify modern systems

By application domain:

- Embedded:
  - Power Consumption
  - Cost
- Signal Processing:
  - I/O data flow
  - FFT/FIR optimisations

Classify…

- Workstation
  - Graphics
  - Games…
- Supercomputer
  - Weather forecasting: Large data volumes
  - Weapons design: Shock hydrodynamics
  - Cryptography: Autocorrelation, Quantum?

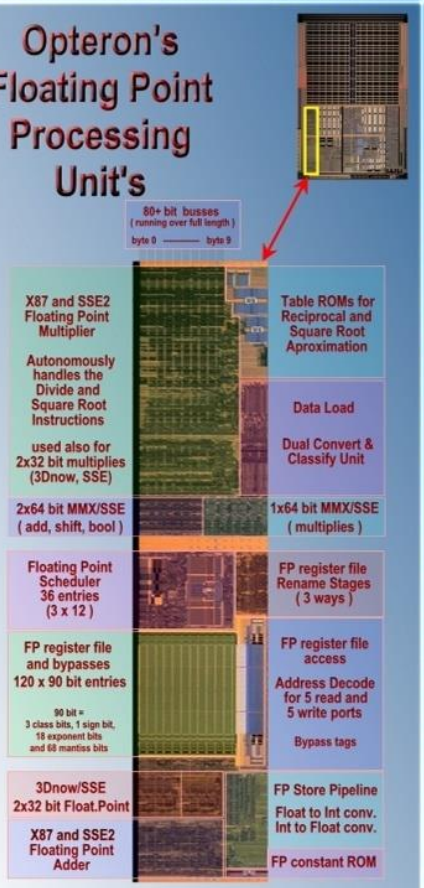
AMD Opteron™

The 64 bit Processor Core of AMD's Opteron

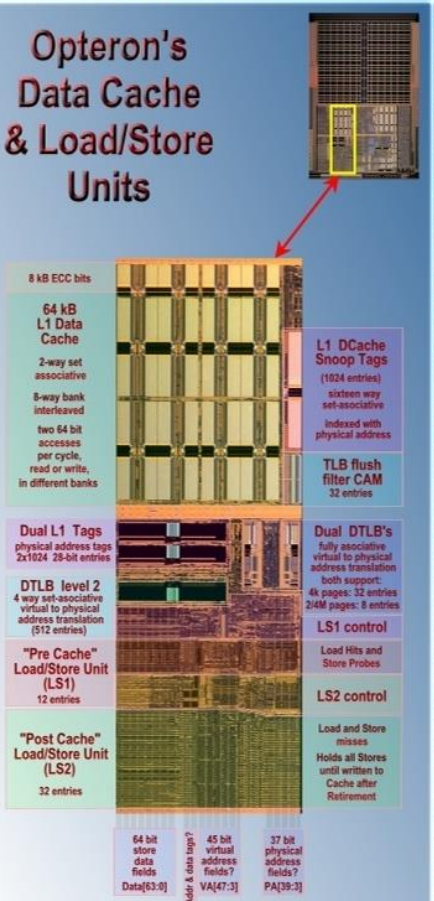
AMD Opteron™

Stage 1	Stage 2	Stage 3	Stage 4	Stage 5	Stage 6	Stage 7	Stage 8	Stage 9	Stage 10	Stage 11	Stage 12	Stage 13	Stage 14	Stage 15	Stage 16	Stage 17	Stage 18	Stage 19	Stage 20
Instruction Address Decode	Instruction Memory Readout	Instruction Byte Pick Selectors	Instruction Decoding Stage 1	Instruction Decoding Stage 2	Instruction Doubles and Pack	Instruction Decoding and Pack	Dispatch and read Future File	ALU & AGU Operation Scheduling	ALU & AGU Operation Execution	Data Cache Address Decode	Data Cache Memory Readout	L2 Cache Access Request	L2 Cache Address to L2 Tags	L2 Cache Obtain,Test L2 Tags	L2 Cache Select Way (1 of 16)	L2 Cache Address Decode	L2 Cache Data Readout	L2 Cache Data Out Selector	L2 Cache Write L1, Forward
								Float Point x87 Stack Rename	Float Point Register Rename	Float Point Write To Scheduler	Float Point Operation Schedule	Float Point Reg. File Access	Float Point Operation Execute 1	Float Point Operation Execute 2	Float Point Operation Execute 3	Float Point Operation Execute 4			

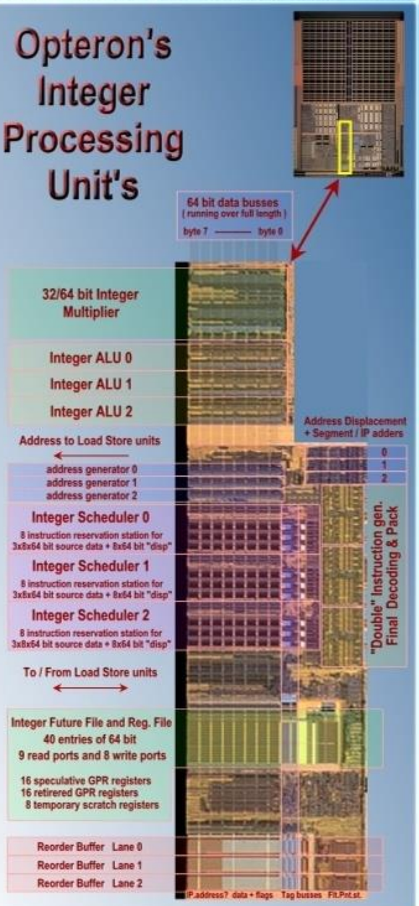
Opteron's Floating Point Processing Unit's


80+ bit busses
(running over full length)
byte 0 —— byte 9
X87 and SSE2 Floating Point Multiplier
Autonomously handles the Divide and Square Root Instructions
used also for 2x32 bit multiplies (3Dnow, SSE)
Table ROMs for Reciprocal and Square Root Aproximation
Data Load
Dual Convert & Classify Unit
2x64 bit MMX/SSE (add, shift, bool)
1x64 bit MMX/SSE (multiplies)
Floating Point Scheduler 36 entries (3 x 12)
FP register file Rename Stages (3 ways)
FP register file and bypasses 120 x 90 bit entries
90 bit = 3 class bits, 1 sign bit, 18 exponent bits and 68 mantiss bits
FP register file access
Address Decode for 5 read and 5 write ports
Bypass tags
3Dnow/SSE 2x32 bit Float.Point
FP Store Pipeline
Float to Int conv. Int to Float conv.
X87 and SSE2 Floating Point Adder
FP constant ROM

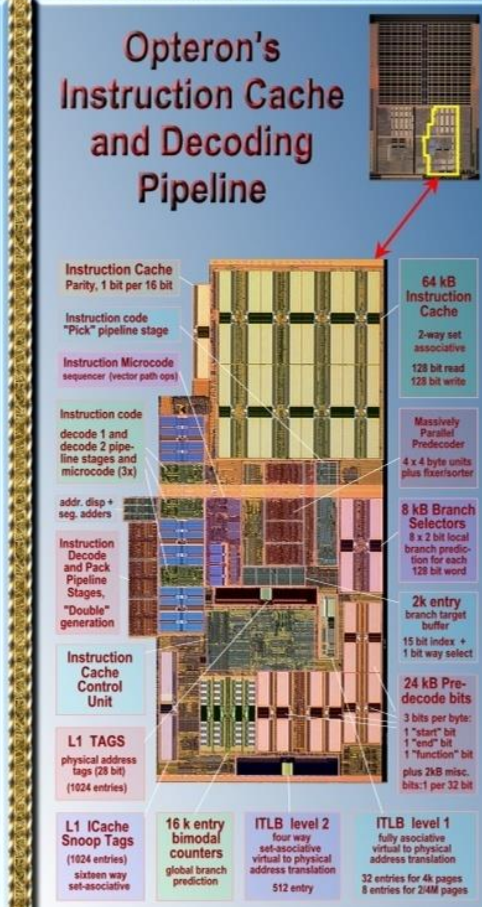
Opteron's Data Cache & Load/Store Units


8 kB ECC bits
64 kB L1 Data Cache
2-way set associative
8-way bank interleaved
two 64 bit accesses per cycle, read or write, in different banks
L1 DCache Snoop Tags
(1024 entries)
sixteen way set-associative
indexed with physical address
TLB flush filter CAM
32 entries
Dual L1 Tags
physical address tags 2x1024 28-bit entries
Dual DTLB's
fully asociative virtual to physical address translation
both support: 4k pages: 32 entries 2/4M pages: 8 entries
DTLB level 2
4 way set-asociative virtual to physical address translation (512 entries)
LS1 control
"Pre Cache" Load/Store Unit (LS1)
12 entries
Load Hits and Store Probes
LS2 control
"Post Cache" Load/Store Unit (LS2)
32 entries
Load and Store misses
Holds all Stores until written to Cache after Retirement
64 bit store data fields Data[63:0]
Addr & data tags?
45 bit virtual address fields? VA[47:3]
37 bit physical address fields? PA[39:3]

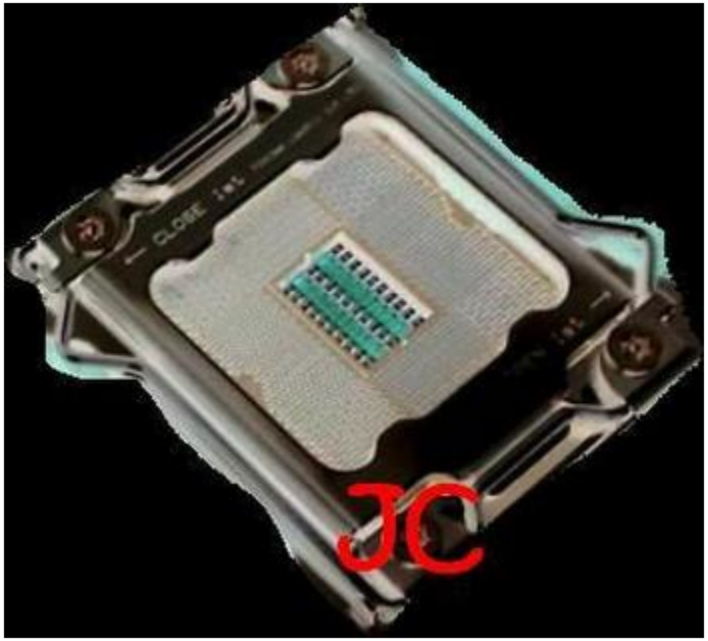
Opteron's Integer Processing Unit's


64 bit data busses
(running over full length)
byte 7 —— byte 0
32/64 bit Integer Multiplier
Integer ALU 0
Integer ALU 1
Integer ALU 2
Address Displacement + Segment / IP adders
0
1
2
Address to Load Store units
address generator 0
address generator 1
address generator 2
Integer Scheduler 0
8 instruction reservation station for 3x8x64 bit source data + 8x64 bit "disp"
Integer Scheduler 1
8 instruction reservation station for 3x8x64 bit source data + 8x64 bit "disp"
Integer Scheduler 2
8 instruction reservation station for 3x8x64 bit source data + 8x64 bit "disp"
"Double" Instruction gen. Final Decoding & Pack
To / From Load Store units
Integer Future File and Reg. File
40 entries of 64 bit
9 read ports and 8 write ports
16 speculative GPR registers
16 retirered GPR registers
8 temporary scratch registers
Reorder Buffer Lane 0
Reorder Buffer Lane 1
Reorder Buffer Lane 2
IP.address? data + flags Tag busses Flt.Pnt.st.

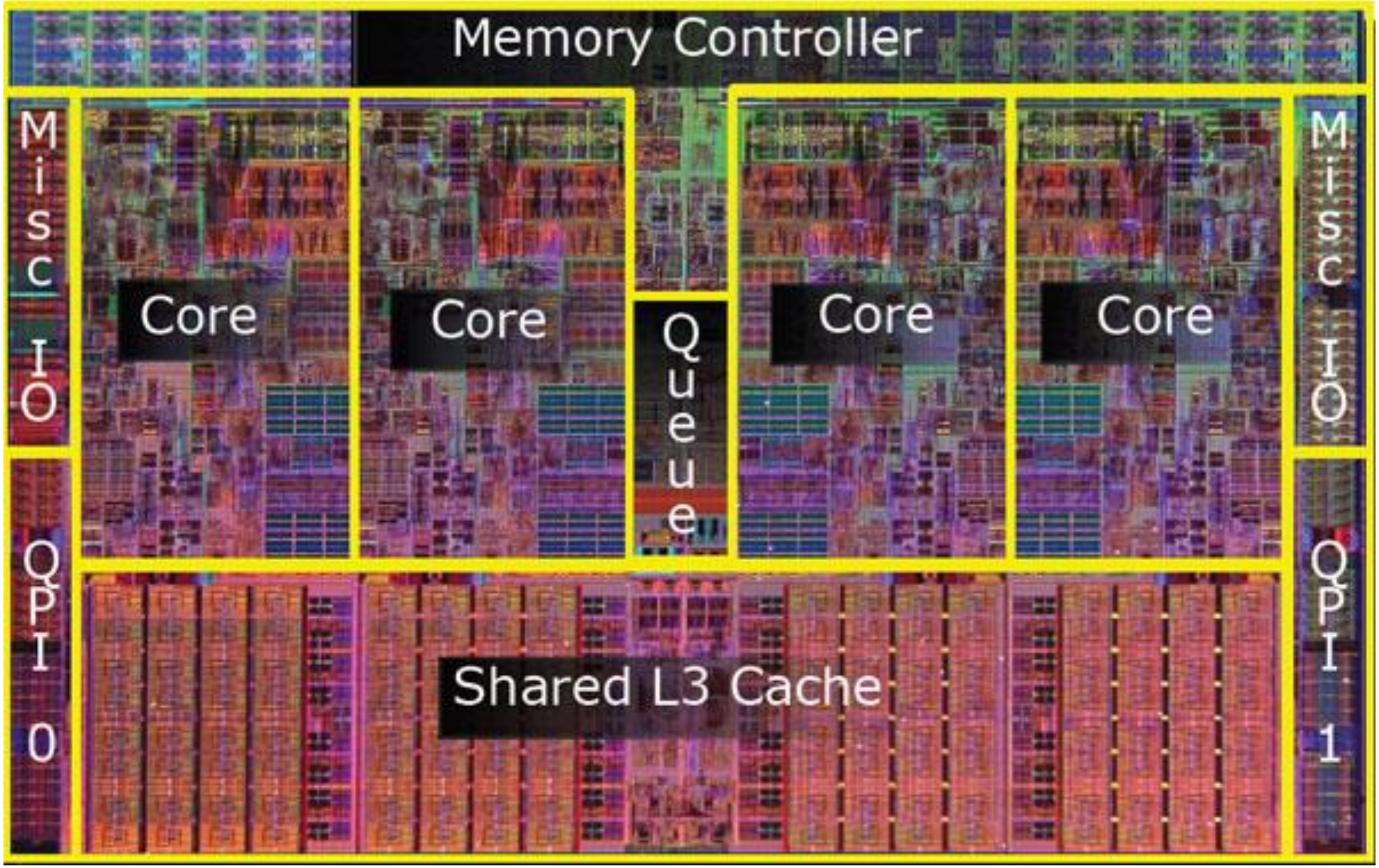
Opteron's Instruction Cache and Decoding Pipeline

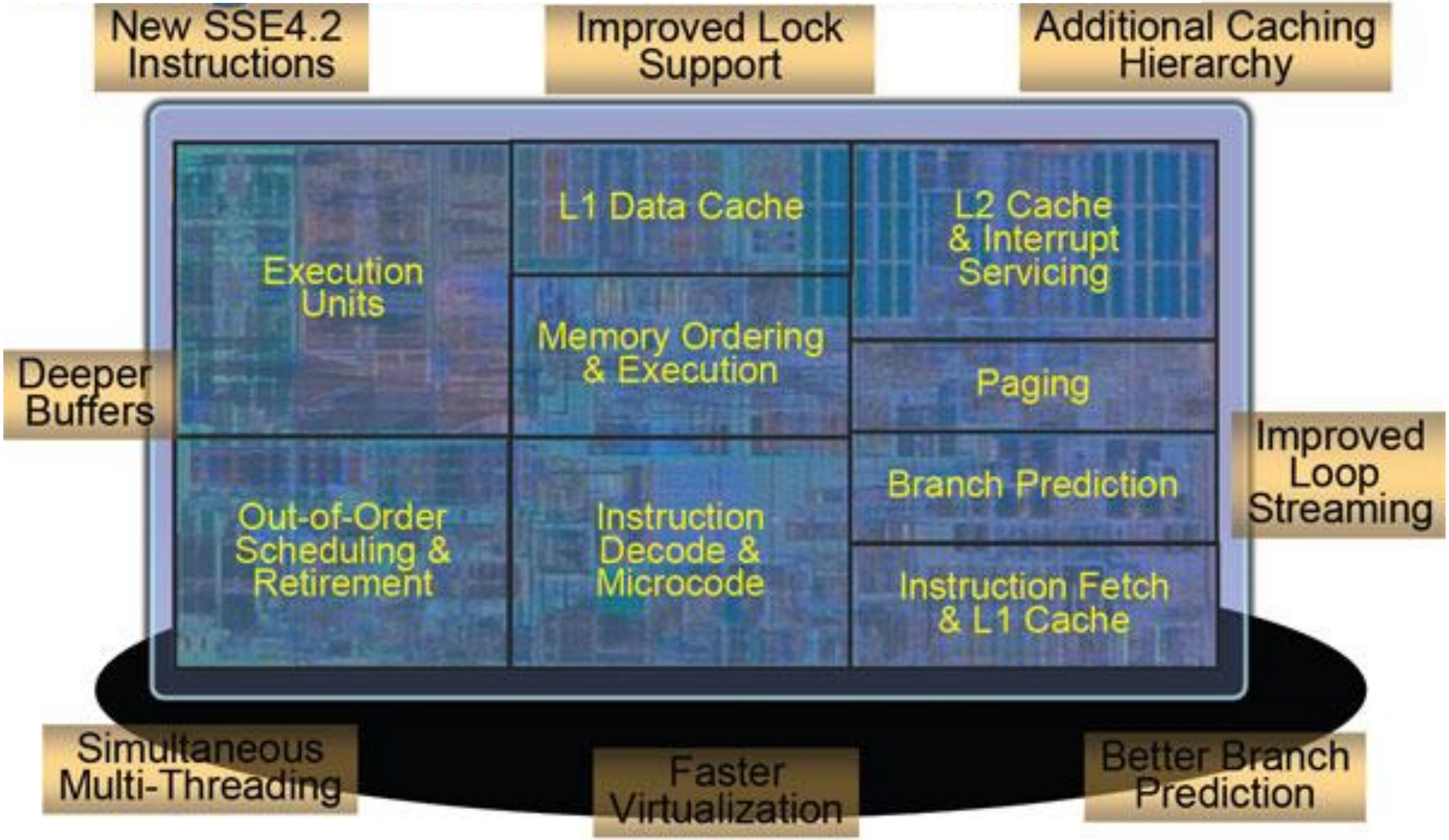

Instruction Cache Parity, 1 bit per 16 bit
Instruction code "Pick" pipeline stage
Instruction Microcode sequencer (vector path ops)
Instruction code
decode 1 and decode 2 pipeline stages and microcode (3x)
addr. disp + seg. adders
Instruction Decode and Pack Pipeline Stages,
"Double" generation
Instruction Cache Control Unit
L1 TAGS
physical address tags (28 bit)
(1024 entries)
64 kB Instruction Cache
2-way set associative
128 bit read
128 bit write
Massively Parallel Predecoder
4 x 4 byte units plus fixer/sorter
8 kB Branch Selectors
8 x 2 bit local branch prediction for each 128 bit word
2k entry branch target buffer
15 bit index + 1 bit way select
24 kB Predecode bits
3 bits per byte: 1 "start" bit 1 "end" bit 1 "function" bit
plus 2kB misc. bits:1 per 32 bit
L1 ICache Snoop Tags
(1024 entries)
sixteen way set-asociative
16 k entry bimodal counters
global branch prediction
ITLB level 2
four way set-asociative virtual to physical address translation
512 entry
ITLB level 1
fully asociative virtual to physical address translation
32 entries for 4k pages
8 entries for 2/4M pages

Intel LGA2011

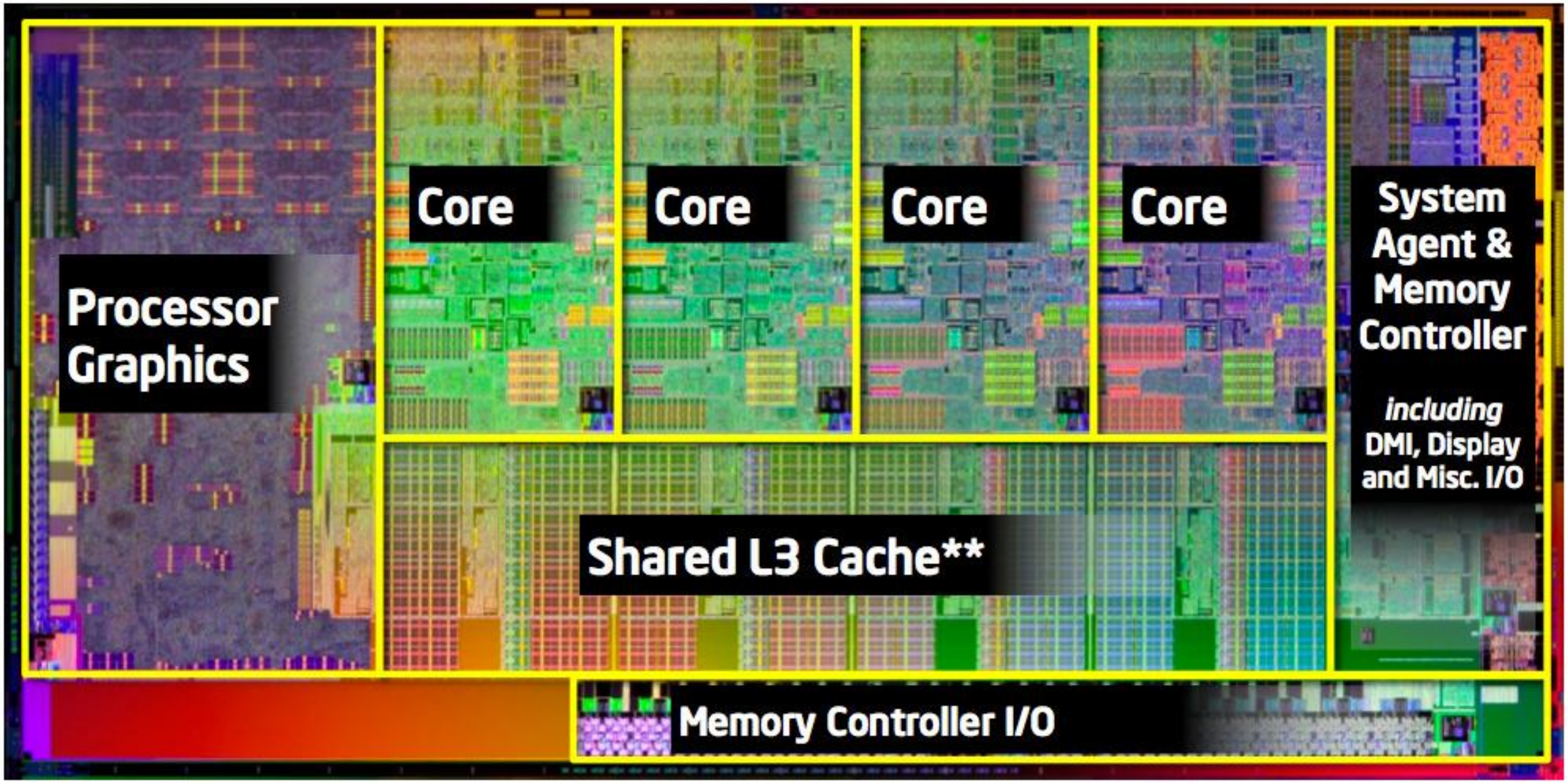


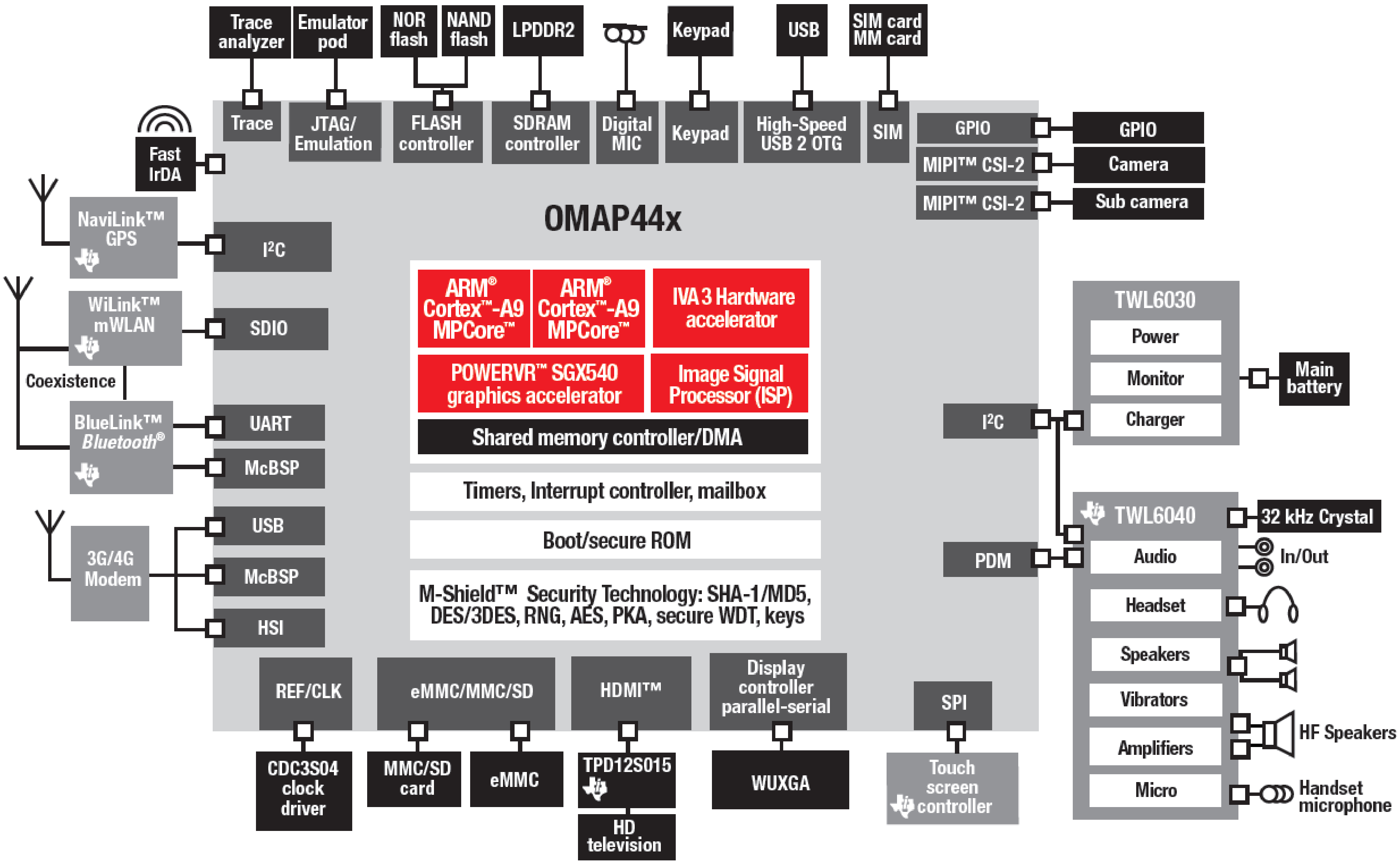
Core i7


Memory Controller
Misc IO
Misc IO
Core
Core
Core
Core
Queue
QPI 0
QPI 1
Shared L3 Cache


New SSE4.2 Instructions
Improved Lock Support
Additional Caching Hierarchy
Execution Units
L1 Data Cache
L2 Cache & Interrupt Servicing
Memory Ordering & Execution
Paging
Deeper Buffers
Improved Loop Streaming
Branch Prediction
Out-of-Order Scheduling & Retirement
Instruction Decode & Microcode
Instruction Fetch & L1 Cache
Simultaneous Multi-Threading
Faster Virtualization
Better Branch Prediction

Sandy Bridge





Trace analyzer
Emulator pod
NOR flash
NAND flash
LPDDR2
Keypad
USB
SIM card MM card

Trace
JTAG/ Emulation
FLASH controller
SDRAM controller
Digital MIC
Keypad
High-Speed USB 2 OTG
SIM

Fast IrDA
NaviLink™ GPS
WiLink™ mWLAN
Coexistence
BlueLink™ *Bluetooth®*
3G/4G Modem

I²C
SDIO
UART
McBSP
USB
McBSP
HSI

OMAP44x

ARM® Cortex™-A9 MPCore™
ARM® Cortex™-A9 MPCore™
IVA 3 Hardware accelerator
POWERVR™ SGX540 graphics accelerator
Image Signal Processor (ISP)
Shared memory controller/DMA
Timers, Interrupt controller, mailbox
Boot/secure ROM
M-Shield™ Security Technology: SHA-1/MD5, DES/3DES, RNG, AES, PKA, secure WDT, keys

GPIO
MIPI™ CSI-2
MIPI™ CSI-2
GPIO
Camera
Sub camera

I²C
PDM

TWL6030
Power
Monitor
Charger
Main battery

TWL6040
32 kHz Crystal
Audio
In/Out
Headset
Speakers
Vibrators
Amplifiers
HF Speakers
Micro
Handset microphone

REF/CLK
eMMC/MMC/SD
HDMI™
Display controller parallel-serial
SPI

CDC3S04 clock driver
MMC/SD card
eMMC
TPD12S015
HD television
WUXGA
Touch screen controller