

# TERM PROJECT 최종 보고서

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## 1. 구현 과정 중 변경된 내용

<10진수, 2진수, 16진수 계산기> -> <10진수 가산기(adder)>로 구현 계획 변경

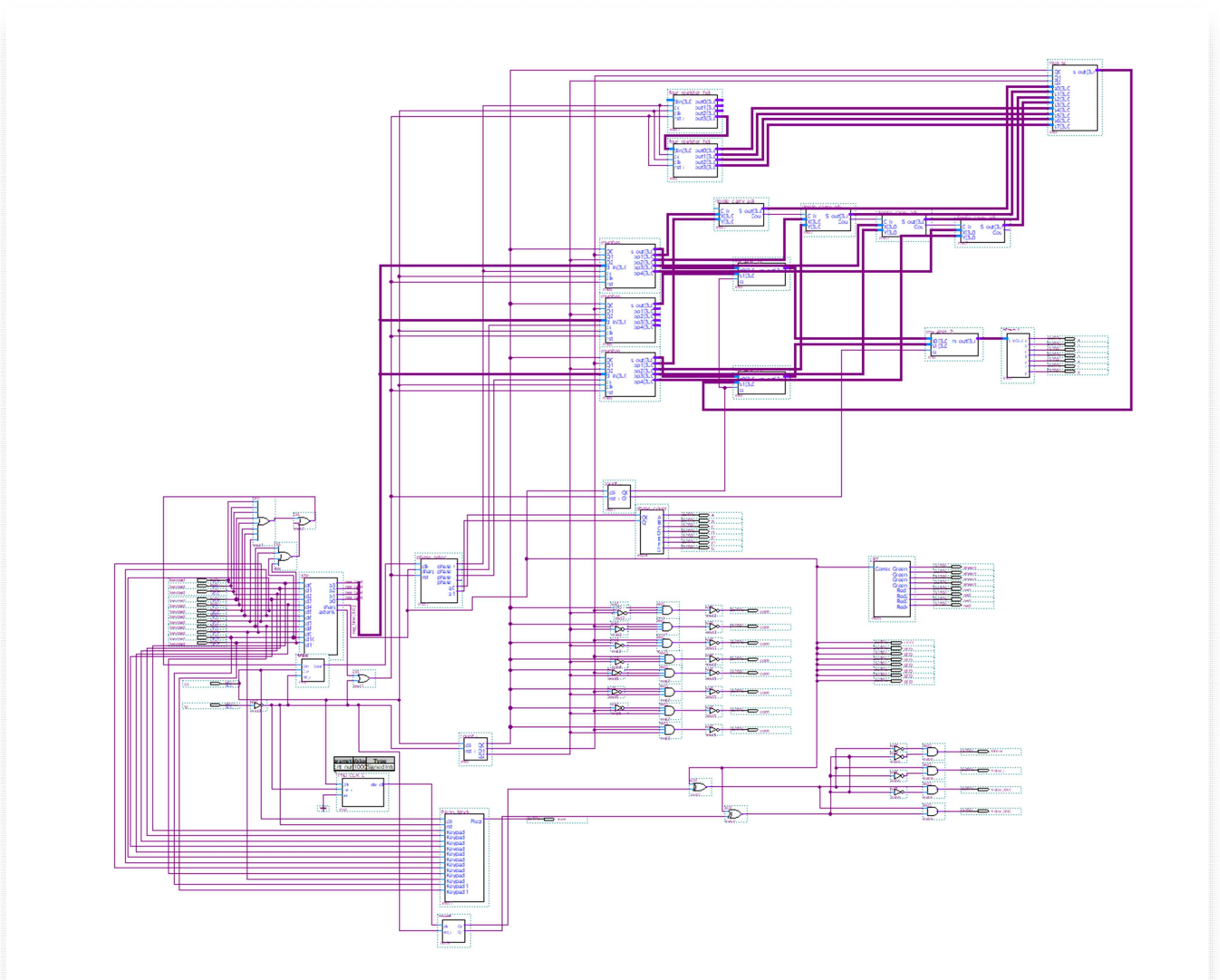
	[기존 과정]	[수정된 과정]
1	첫 번째 피연산자(operand) 입력	
2	연산자(operator) 입력	가산기 부분만 구현하여 별도의 입력 과정 필요하지 않음
3	두 번째 피연산자(operand) 입력	
4	= 을 뜻하는 기호 입력	
5	10, 16, 2진수 값 출력	10진수 값 출력
6	초기화 버튼(*)을 누르면 다시 초기화	
7	이후 다시 과정 반복	

### [출력]

- (1) 8 Array 7-Segment를 이용하여 10진수 계산 결과 출력
- (2) PIEZO 부저를 이용하여 Keypad(0~9, #, \*)를 누를 때 입력 받는 음(도,레,미,파,솔,라,시,도...) 출력
- (3) '#'을 누를 때, 다음 단계(Phase)로 넘어감을 표현하기 위해, 모터 정방향 회전, RGB GREEN 출력, LED 8개 점멸을 활용했음.
- (4) 모터 역방향 회전, RGB RED 출력이 기본값임('#'을 누르지 않을 때)
- (5) '#'을 눌러 phase가 변경될 때, 7-segment에 순서대로 1 ~ 4 표시.

## 2. 구현 과정

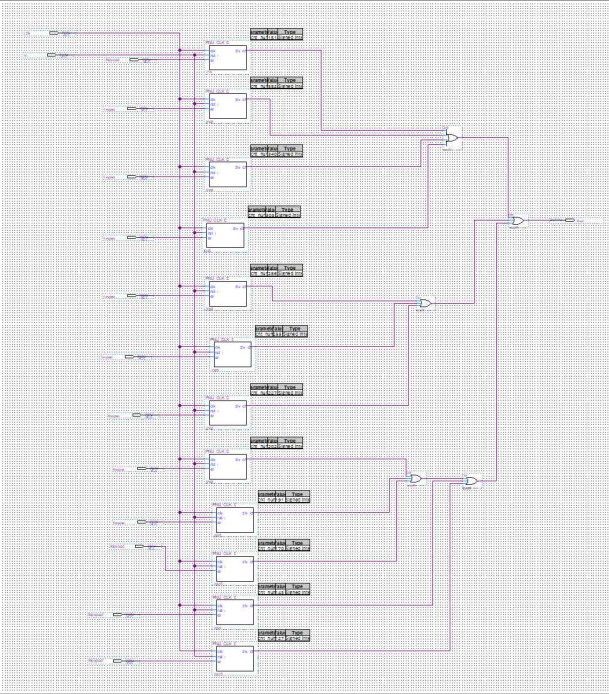
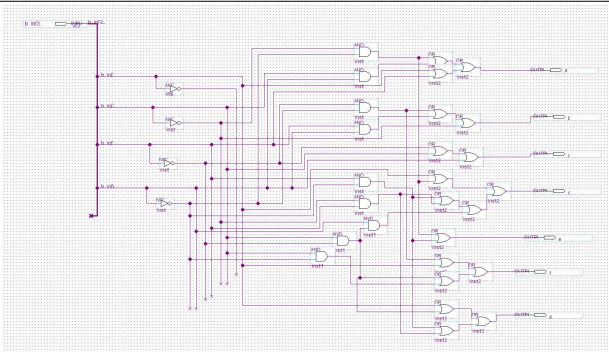
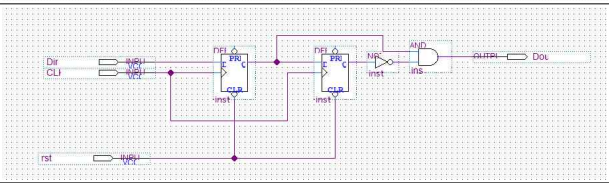
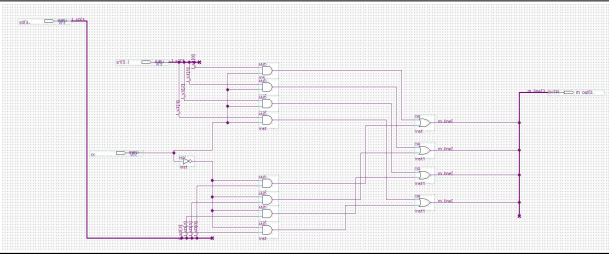
### [전체 회로도]

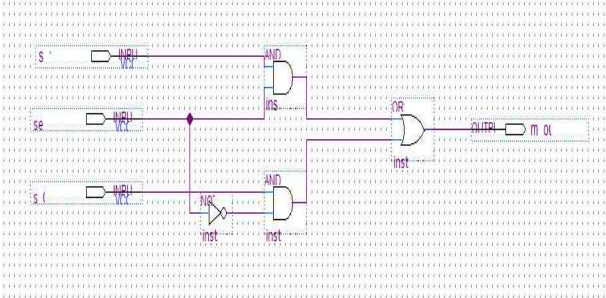
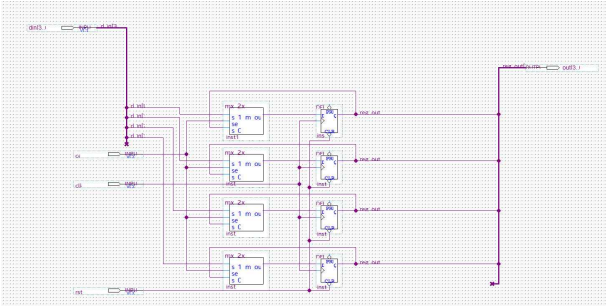
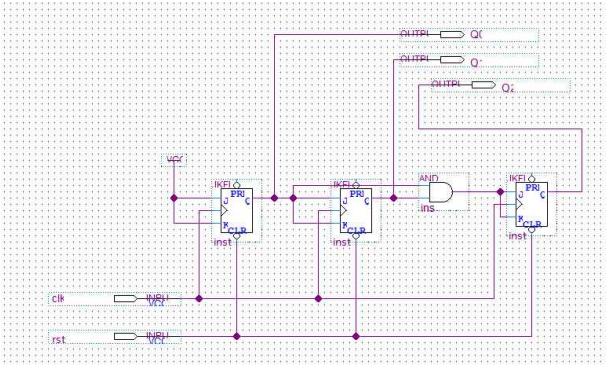
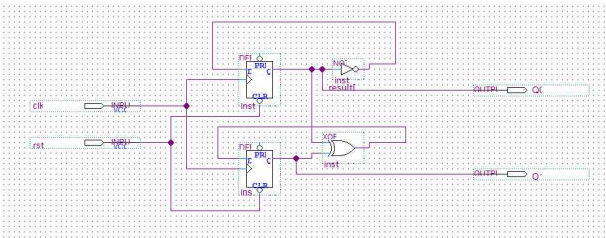
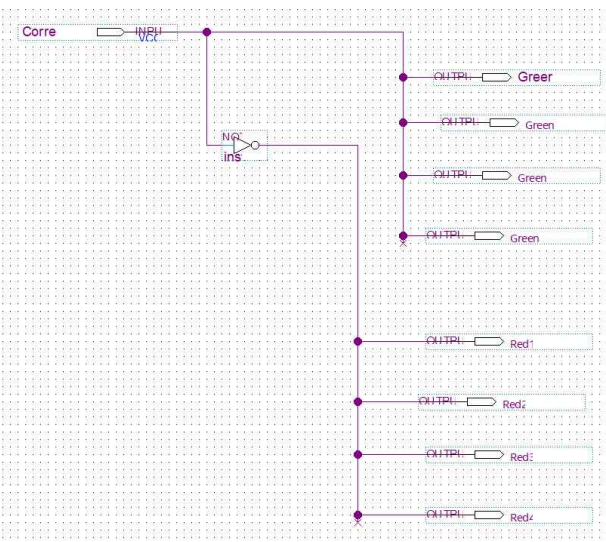


### [전체 File]

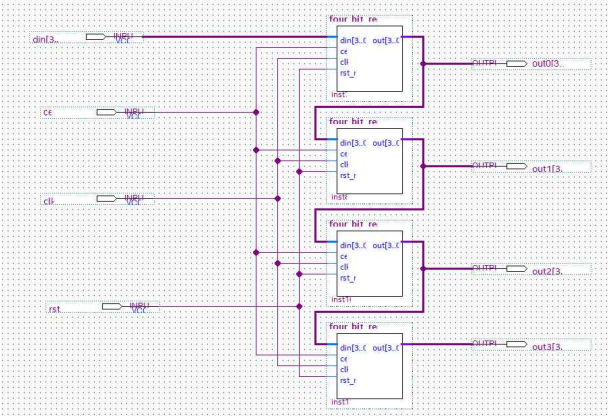
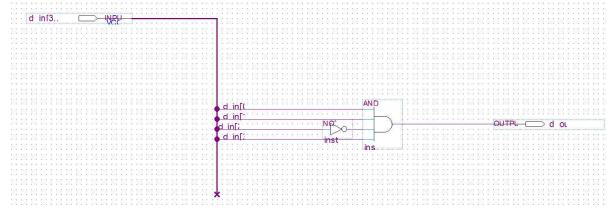
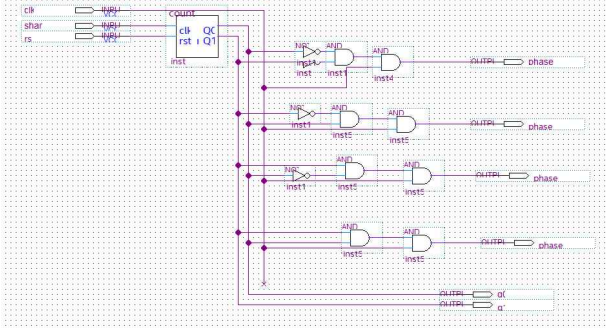
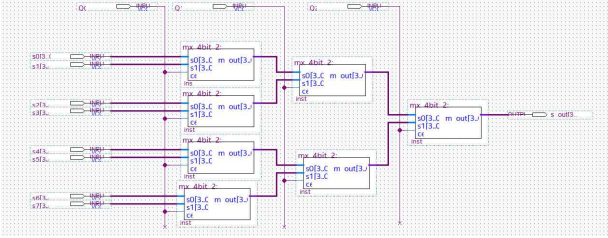
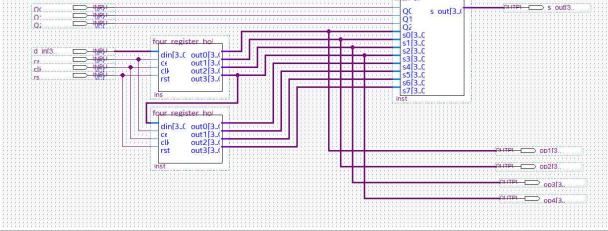
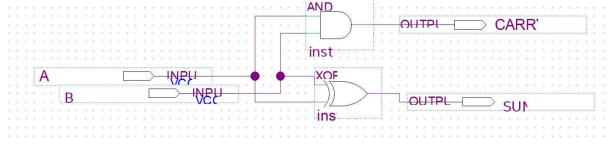
- Piezo\_Module.bdf
- b2seg\_bus.bdf
- trigger.bdf
- mx\_4bit\_2x1.bdf
- mx\_2x1.bdf
- four\_bit\_reg\_ce.bdf
- count\_8.bdf
- count\_4.bdf
- LED.bdf
- four\_register\_holder.bdf

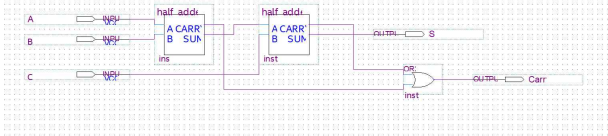
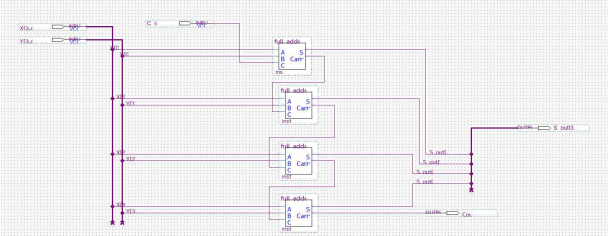
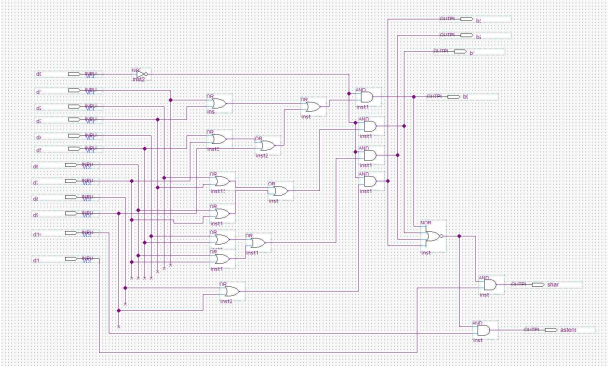
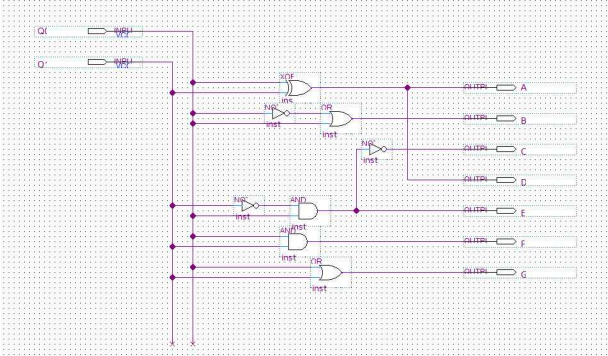
- check\_sharp.bdf
- phase\_selector.bdf
- mux\_set.bdf
- myphase.bdf
- calculator.bdf
- half\_adder.bdf
- full\_adder.bdf
- ripple\_carry\_adder.bdf
- d2b.bdf
- phase\_counter.bdf

Schematic (.bdf)	Circuit Image
Piezo_module	 The circuit diagram for 'Piezo_module' is a complex logic network on a grid background. It features a vertical column of ten 'combinational_logic' blocks, each with a 'Y' output. These blocks are interconnected with a series of logic gates, including AND gates (represented by triangles) and OR gates (represented by circles). The inputs to these gates are derived from the 'Y' outputs and other internal signals. The final output of the circuit is a single signal line on the right side.
b2seg_bus	 The circuit diagram for 'b2seg_bus' shows a multi-bit bus system. It starts with a 16-bit input bus on the left, which is connected to a series of 16 AND gates. Each AND gate's output is connected to a corresponding output bus on the right. The circuit also includes several OR gates and inverters to manage the bus signals.
trigger	 The circuit diagram for 'trigger' is a simple logic circuit. It takes two inputs, 'Dir' and 'CLI', which are connected to two AND gates. The outputs of these AND gates are connected to a single OR gate. The output of the OR gate is connected to a signal line labeled 'DOL'.
mx_4bit_2x1	 The circuit diagram for 'mx_4bit_2x1' is a multi-bit bus system. It features a 4-bit input bus on the left, which is connected to a series of 4 AND gates. Each AND gate's output is connected to a corresponding output bus on the right. The circuit also includes several OR gates and inverters to manage the bus signals.

mx_2x1	 <p>The circuit diagram for 'mx_2x1' shows two input signals, 'S' and 'SE', each connected to an inverter. The outputs of these inverters are connected to two AND gates. The outputs of the AND gates are connected to an OR gate, which produces the final output 'O1'.</p>
four_bit_reg_ce	 <p>The circuit diagram for 'four_bit_reg_ce' is a 4-bit register. It consists of four D flip-flops, each with a clock input 'clk' and a clear input 'rst'. The outputs of the flip-flops are connected to a 4-bit bus 'Q[3:0]'. The circuit also includes a 4-bit input 'D[3:0]' and a 4-bit output 'Q[3:0]'.</p>
count_8	 <p>The circuit diagram for 'count_8' is an 8-bit counter. It consists of eight D flip-flops, each with a clock input 'clk' and a clear input 'rst'. The outputs of the flip-flops are connected to an 8-bit bus 'Q[7:0]'. The circuit also includes an 8-bit input 'D[7:0]' and an 8-bit output 'Q[7:0]'.</p>
count_4	 <p>The circuit diagram for 'count_4' is a 4-bit counter. It consists of four D flip-flops, each with a clock input 'clk' and a clear input 'rst'. The outputs of the flip-flops are connected to a 4-bit bus 'Q[3:0]'. The circuit also includes a 4-bit input 'D[3:0]' and a 4-bit output 'Q[3:0]'.</p>
LED	 <p>The circuit diagram for 'LED' shows a single input signal 'Corre' connected to an inverter. The output of the inverter is connected to a 4-bit bus 'Q[3:0]'. The circuit also includes a 4-bit input 'D[3:0]' and a 4-bit output 'Q[3:0]'. The outputs of the bus are connected to four LEDs labeled 'Greer', 'Green', 'Red1', and 'Red2'.</p>



four_register_holder	
check_sharp	
phase_selector	
mux_set	
myphase	
half_adder	

full_adder	 <p>The diagram shows a full adder circuit implemented using two 'half-adder' blocks. The first half-adder takes inputs A and B, producing a sum output S and a carry output C1. The second half-adder takes inputs S and C, producing a final sum output S and a carry output Carr. The carry output Carr is the result of an OR operation between the carry outputs of the two half-adders.</p>
ripple_carry_adder	 <p>The diagram illustrates a ripple carry adder. It consists of four 'half-adder' blocks. The first two half-adders take inputs X1, X2 and Y1, Y2. Their carry outputs are connected to the inputs of the next two half-adders. The final sum output S and carry output Carr are produced by the last half-adder.</p>
d2b	 <p>The diagram shows a decimal-to-binary (d2b) converter. It takes a decimal input (0-9) and produces a 4-bit binary output (A, B, C, D). The circuit uses a series of AND gates to generate the binary digits from the decimal input.</p>
phase_counter	 <p>The diagram depicts a phase counter circuit. It takes a clock input and produces a 7-bit binary output (A, B, C, D, E, F, G). The circuit uses a series of AND gates to generate the binary digits from the clock input.</p>

### 3. 구현 결과

	구현 과정	성공 여부
1	첫 번째 피연산자(operand) 입력	O
2	가산기 부분만 구현하여 별도의 입력 과정 필요하지 않음	△
3	두 번째 피연산자(operand) 입력	O
4	= 을 뜻하는 기호(#) 입력	O
5	10진수 값 출력	△
6	초기화 버튼(*)을 누르면 다시 초기화 -> left shifter로 대체	X
7	8 Array 7-Segment를 이용하여 10진수 계산 결과 출력	O
8	PIEZO 부저를 이용하여 Keypad(0~9, #, *)를 누를 때 입력 받는 음(도,레,미,파,솔,라,시,도...) 출력	O
9	'#'을 누를 때, 다음 단계(Phase)로 넘어감을 표현하기 위해, 모터 정방향 회전, RGB GREEN 출력, LED 8개 점멸	O
10	모터 역방향 회전, RGB RED 출력이 기본값임('#'을 누르지 않을 때)	O
11	'#'을 눌러 phase가 변경될 때, 7-segment에 순서대로 1 ~ 4 표시.	O

### 4. 기존 계획 대비 완성도

O : 100%, △ : 50%, X : 0%로 계산.

기존 계획 대비 전체 완성도 : 약 82%