FPGA Digital Calculator: Block Diagram

Digital Systems (ELEC ENG 2100)

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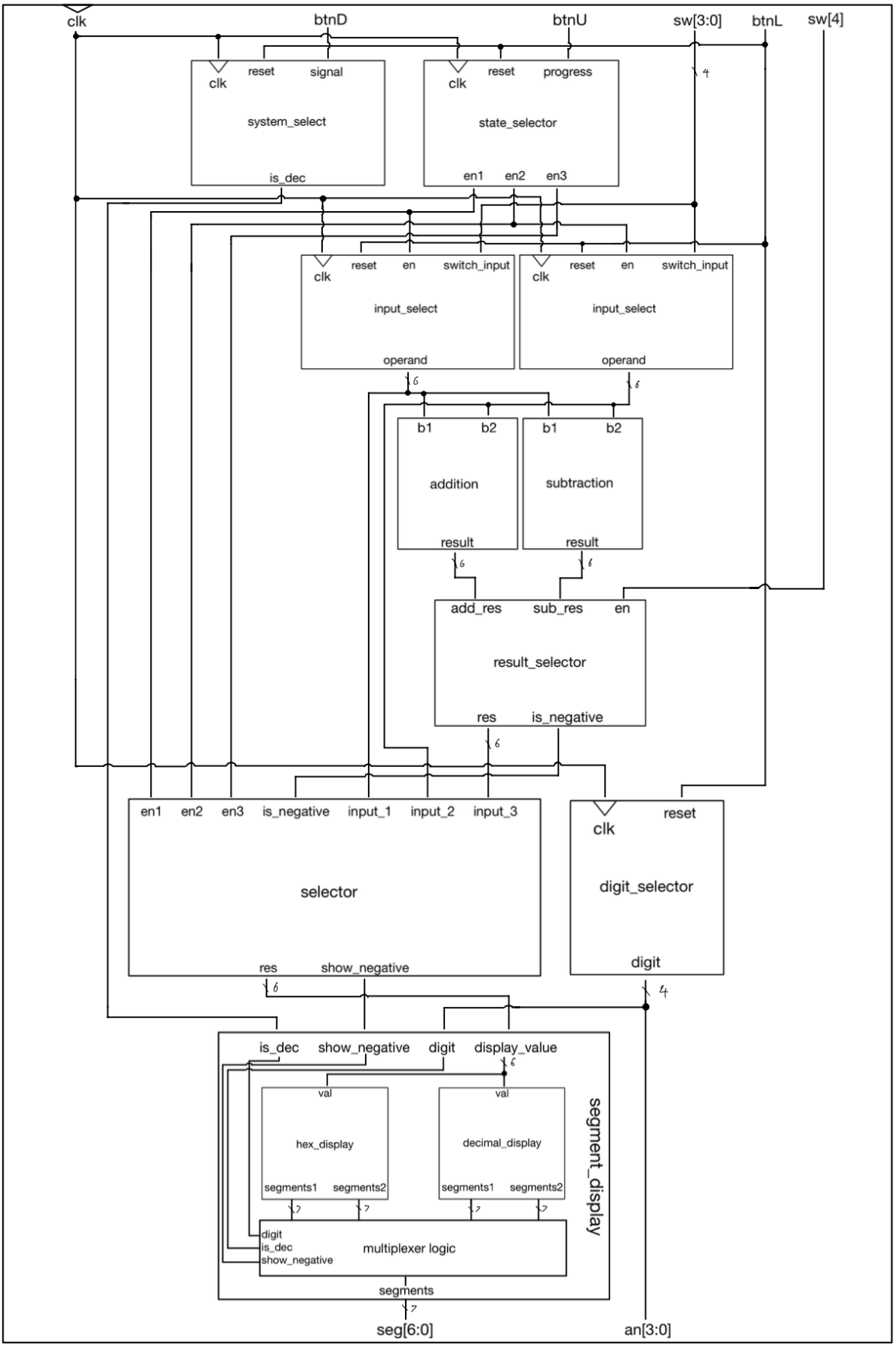

Figure 1: Block diagram displaying contents of the top module.

Module Descriptions

`top` Top-level integration module connecting all submodules. Manages signals between control, datapath, and display components.

`state_selector`
Finite state machine that determines which calculator stage is active (operand 1 input, operand 2 input, or result display). Produces enable signals `en1`, `en2`, and `en3`.

`system_select`
Toggles between hexadecimal and decimal display modes when `btnD` is pressed. Outputs `is_dec`, determining which display decoder is active.

`input_select`
Captures switch input values when enabled. Two instances are used—one for each operand.

`addition` Implements an n-bit ripple-carry adder to compute the sum of two operands.

`subtraction`
Implements two's complement subtraction by inverting the second operand, adding one, and passing both through the adder.

`result_selector`
Selects between addition and subtraction results based on `add_or_sub`. Also detects sign and outputs absolute magnitude and a negative flag.

`selector` Chooses which value to send to the display depending on the calculator state: operand 1, operand 2, or the result.

`digit_selector`
Generates the anode control signals for displaying the 7-segment display so each digit appears continuously lit.

`segment_display`
Drives the 7-segment LEDs. Selects between hexadecimal and decimal display modules and shows a minus sign when `show_negative` is active.

`hex_display`
Generates segment patterns for two hexadecimal digits from a 6-bit value.

`decimal_display`
Generates segment patterns for two decimal digits by converting the 6-bit value into BCD format.