Xilinx Virtex-5 Family FPGAs

		Virtex-5 LX Platform						Virtex-5 LXT Platform						Virtex-5 SXT Platform		
		LX30	LX50	LX85	LX110	LX220	LX330	LX30T	LX50T	LX85T	LX110T	LX220T	LX330T	SX35T	SX50T	SX95T
	Part Number	XC5VLX30	XC5VLX50	XC5VLX85	XC5VLX110	XC5VLX220	XC5VLX330	XC5VLX30T	XC5VLX50T	XC5VLX85T	XC5VLX110T	XC5VLX220T	XC5VLX330T	XC5VSX35T	XC5VSX50T	XC5VSX95T
	EasyPath™ Cost Reduction Solutions (1)	—	—	XCE5VLX85	XCE5VLX110	XCE5VLX220	XCE5VLX330	—	—	XCEVLXT85T	XCE5VLX110T	XCE5VLX220T	XCE5VLX330T	—	XCE5VSX50T	XCE5VSX95T
CLB Resources	CLB Array Size (Row x Column)	80 x 30	120 x 30	120 x 54	160 x 54	160 x 108	240 x 108	80 x 30	120 x 30	120 x 54	160 x 54	160 x 108	240 x 108	80 x 34	120 x 34	160 x 46
	Slices (2)	4,800	7,200	12,960	17,280	34,560	51,840	4,800	7,200	12,960	17,280	34,560	51,840	5,440	8,160	14,720
	Logic Cells (3)	30,720	46,080	82,944	110,592	221,184	331,776	30,720	46,080	82,944	110,592	221,184	331,776	34,816	52,224	94,208
	CLB Flip-Flops	19,200	28,800	51,840	69,120	138,240	207,360	19,200	28,800	51,840	69,120	138,240	207,360	21,760	32,640	58,880
Memory Resources	Maximum Distributed RAM (kbits)	320	480	840	1,120	2,280	3,420	320	480	840	1,120	2,280	3,420	520	780	1,520
	Block RAM/FIFO w/ECC (36kbits each)	32	48	96	128	192	288	36	60	108	148	212	324	84	132	244
	Total Block RAM (kbits)	1,152	1,728	3,456	4,608	6,912	10,368	1,296	2,160	3,888	5,328	7,632	11,664	3,024	4,752	8,784
Clock Resources	Digital Clock Manager (DCM)	4	12	12	12	12	12	4	12	12	12	12	12	4	12	12
	Phase Locked Loop (PLL)/PMCD	2	6	6	6	6	6	2	6	6	6	6	6	2	6	6
I/O Resources	Maximum SelectIO™ Pins	400	560	560	800	800	1,200	360	480	480	680	680	960	360	480	640
	SelectIO™ Banks	13	17	17	23	23	33	12	15	15	19	20	27	12	15	19
	Digitally Controlled Impedance	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	Maximum Differential I/O Pairs	200	280	280	400	400	600	180	240	240	340	340	480	180	240	320
	I/O Standards	HT, LVDS, LVDSEXT, RSDS, BLVDS, ULVDS, LVPECL, LVCMOS33, LVCMOS25, LVCMOS18, LVCMOS15, LVTTL, PCI33, PCI66, PCI-X, GTL, GTL+, HSTL I (1.2V,1.5V,1.8V), HSTL II (1.5V,1.8V), HSTL III (1.5V,1.8V), HSTL IV (1.5V,1.8V), SSTL2 I, SSTL2 II, SSTL18 I, SSTL18 II														
Embedded Hard IP Resources	DSP48E Slices	32	48	48	64	128	192	32	48	48	64	128	192	192	288	640
	System Monitor Blocks	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	PCI Express Endpoint Blocks	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
	10/100/1000 Ethernet MAC Blocks	0	0	0	0	0	0	4	4	4	4	4	4	4	4	4
	RocketIO™ GTP Low-Power Transceivers	0	0	0	0	0	0	8	12	12	16	16	24	8	12	16
	Configuration Memory (Mbits)	8.4	12.6	21.8	29.1	53.1	79.7	9.4	14.1	23.3	31.1	55.1	82.7	13.3	20.0	35.7
Package (4)	Area	I/O	MGT (5)													
FF324	19 x 19 mm	220		220	220											
FF676	27 x 27 mm	440		400	440	440	440									
FF1153	35 x 35 mm	800			560	560	800									
FF1760	42.5 x 42.5 mm	1200					800	800	1200							
FF665	27 x 27mm	360	8					360 (8)	360 (8)					360 (8)	360 (8)	
FF1136	35 x 35mm	640	16						480 (12)	480 (12)	640 (16)				480 (12)	640 (16)
FF1738	42.5 x 42.5mm	960	24								680 (16)	680 (16)	960 (24)			

Notes:
1. EasyPath™ solutions provide a conversion-free path for volume production
2. A single Virtex-5 CLB comprises two slices, with each containing four 6-input LUTs and four Flip-Flops (twice the number found in a Virtex-4 slice), for a total of eight 6-LUTs and eight Flip-Flops per CLB.
3. Virtex-5 logic cell ratings reflect the increased logic capacity offered by the new 6-input LUT architecture.
4. FFA Packages (FF): flip-chip fine-pitch BGA (1.00 mm ball spacing).
5. Number of available RocketIO™ multi-gigabit transceivers (MGTs) for each device/package combination shown in parentheses.
6. Virtex-5 commercial grade devices come in three speedgrades: -1, -2, -3 (-3 being the fastest).
7. Virtex-5 industrial grade devices come in two speedgrades: -1, -2 (-2 being the fastest).

Important: Verify all data in this document with the device data sheets found at *www.xilinx.com/virtex5*