Lecture 12

Intro to Texas Instruments Digital Signal Processors

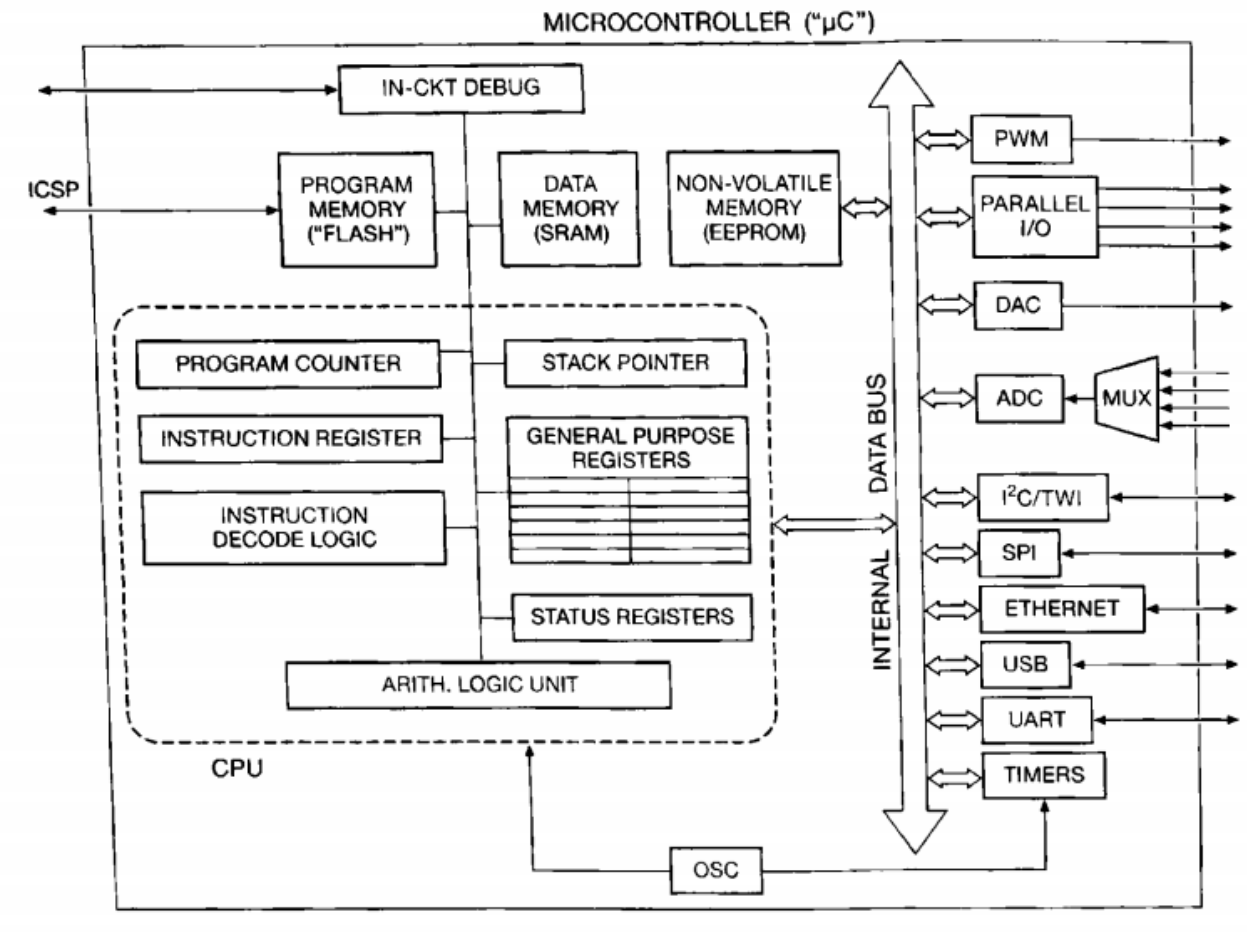
Objectives:

- Discuss the general internal arrangement of modern CPUs and peripherals.
- Give an overview of peripherals and discuss how they are connected to special function registers in the processor memory.
- Explain memory types and how RAM is sectioned into SFRs and GPRs.
- Discuss how PWM is generated by comparing a counter with a constant.
- Discuss setting the PWM frequency, and the duty cycle resolution.

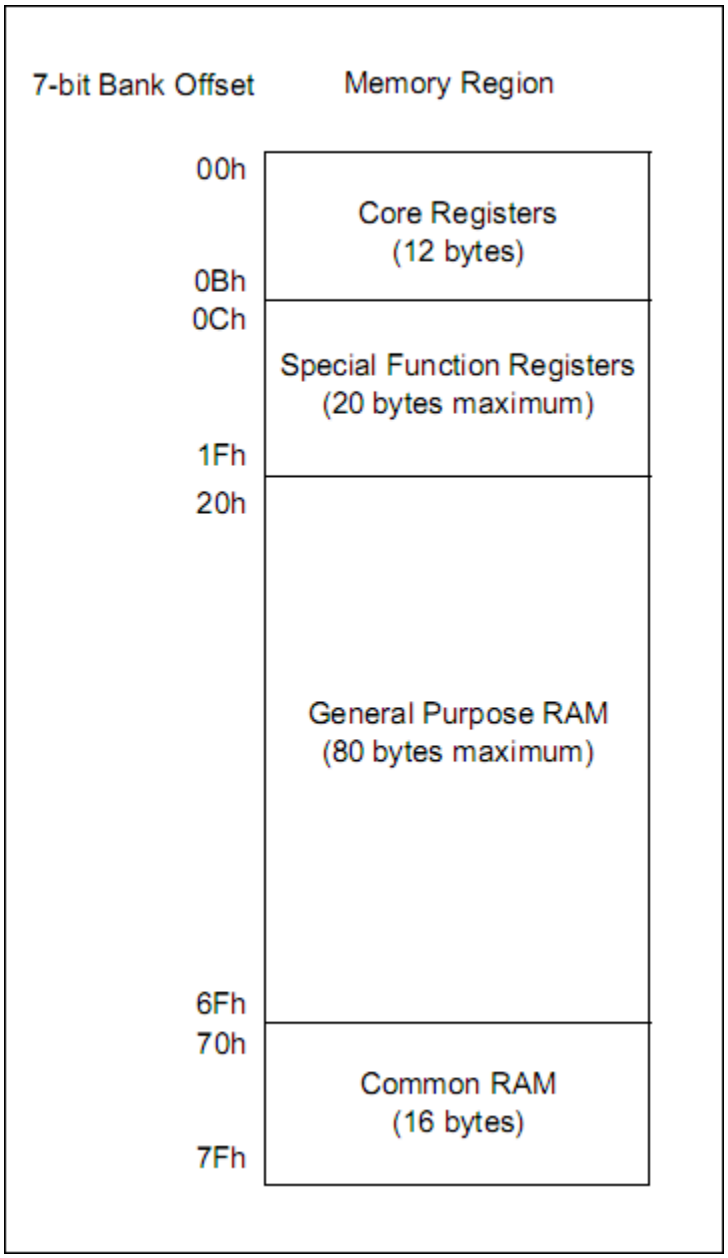
Keywords:

Central Processing Unit (CPU)
Peripheral hardware
Random Access Memory (RAM)
Electrically Erasable Programmable Read-Only Memory (EEPROM)
General purpose register (GPR)
Special function register (SFR)
Counter register (CTR)
Period register (PRD)
Compare-A register (CMPA)
Edge-aligned & Center-aligned PWM
Up-Count, Down-Count, and Up/Down-Count
Duty cycle resolution

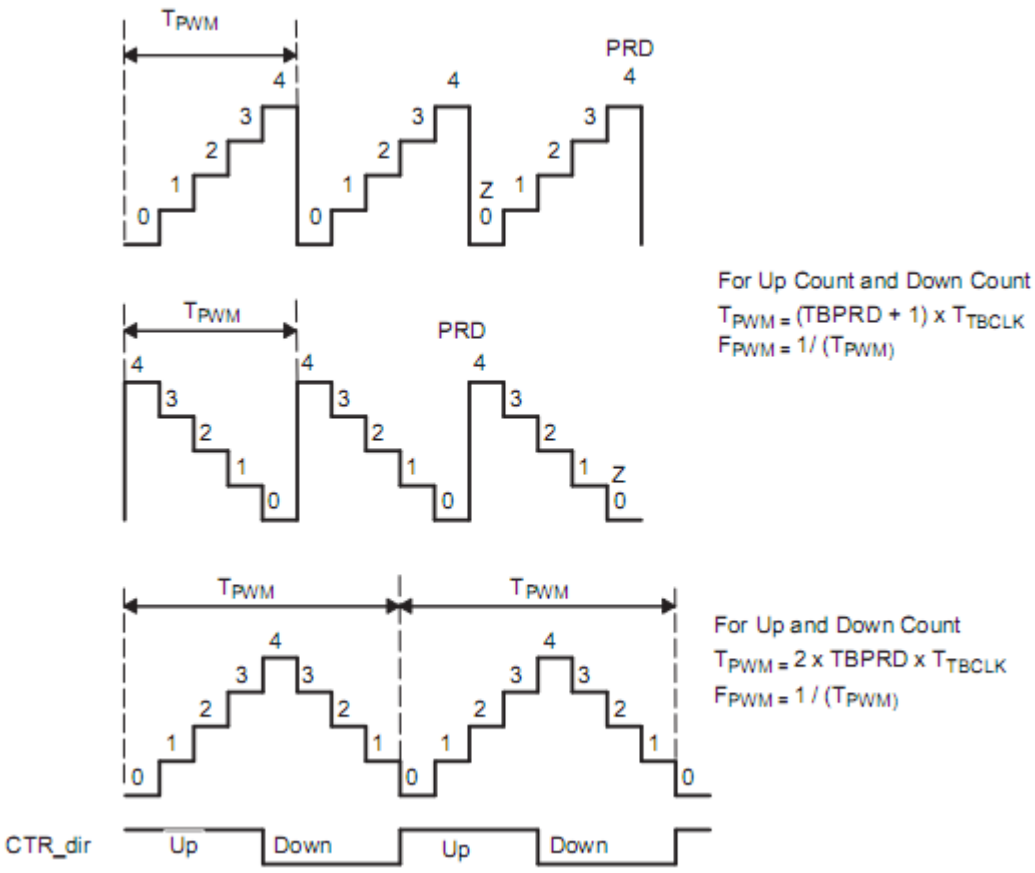
Overview of Microcontroller Architecture



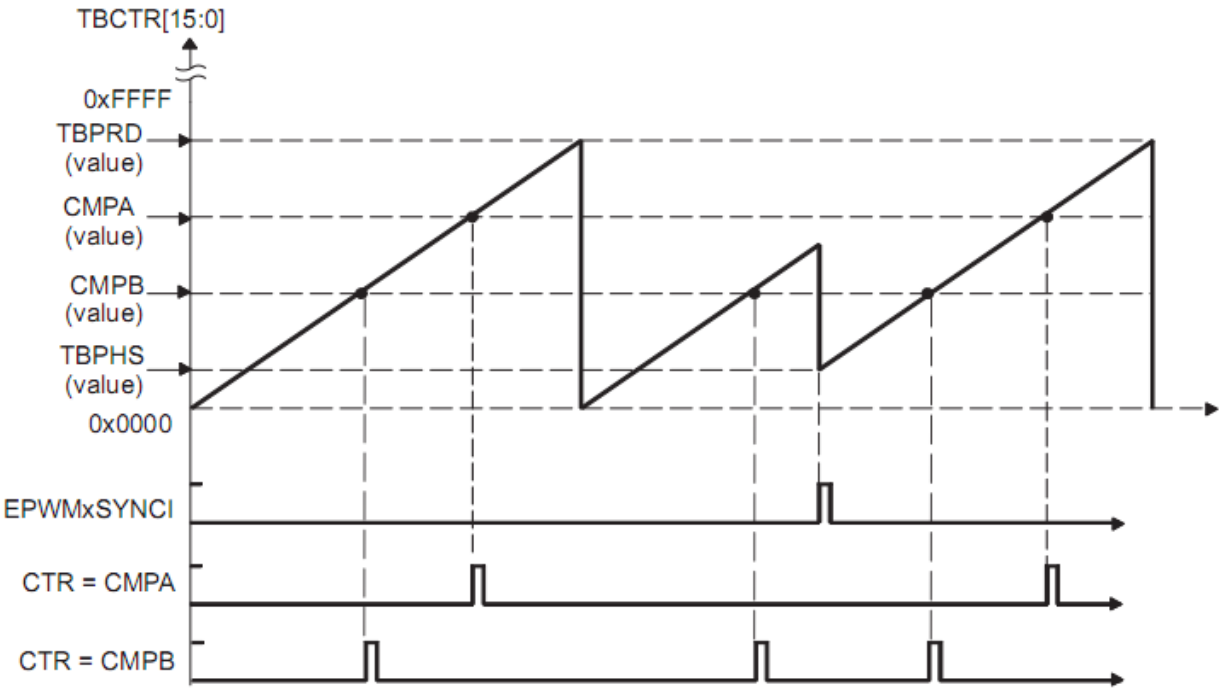
Arrangement of Processor Memory



PWM Counter Values



Controlling the PWM Pin



NOTE: An EPWMxSYNCI external synchronization event can cause a discontinuity in the TBCTR count sequence. This can lead to a compare event being skipped. This skipping is considered normal operation and must be taken into account.