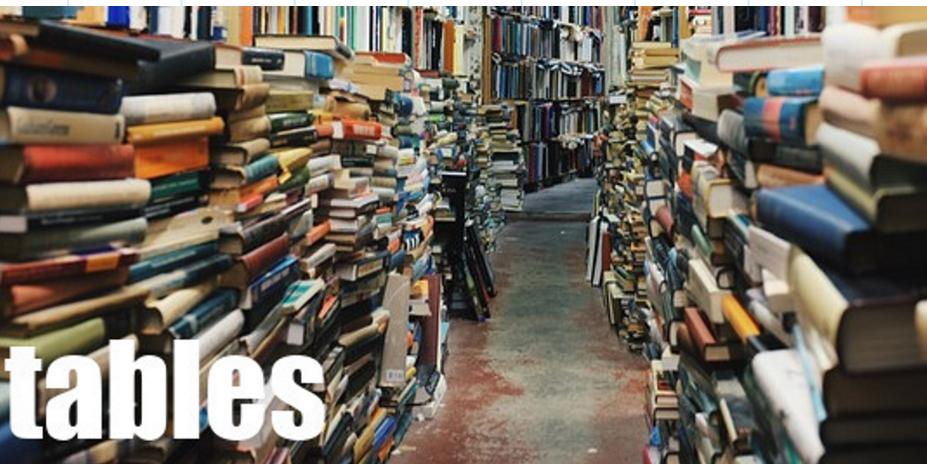
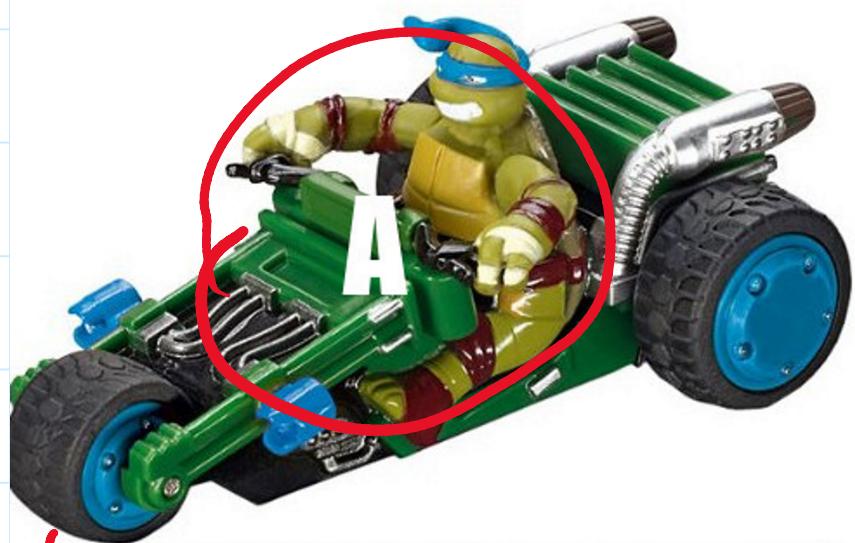


Lecture 17 - Paging, TLBs, and Page directories

July 10, 2019 10:20 AM



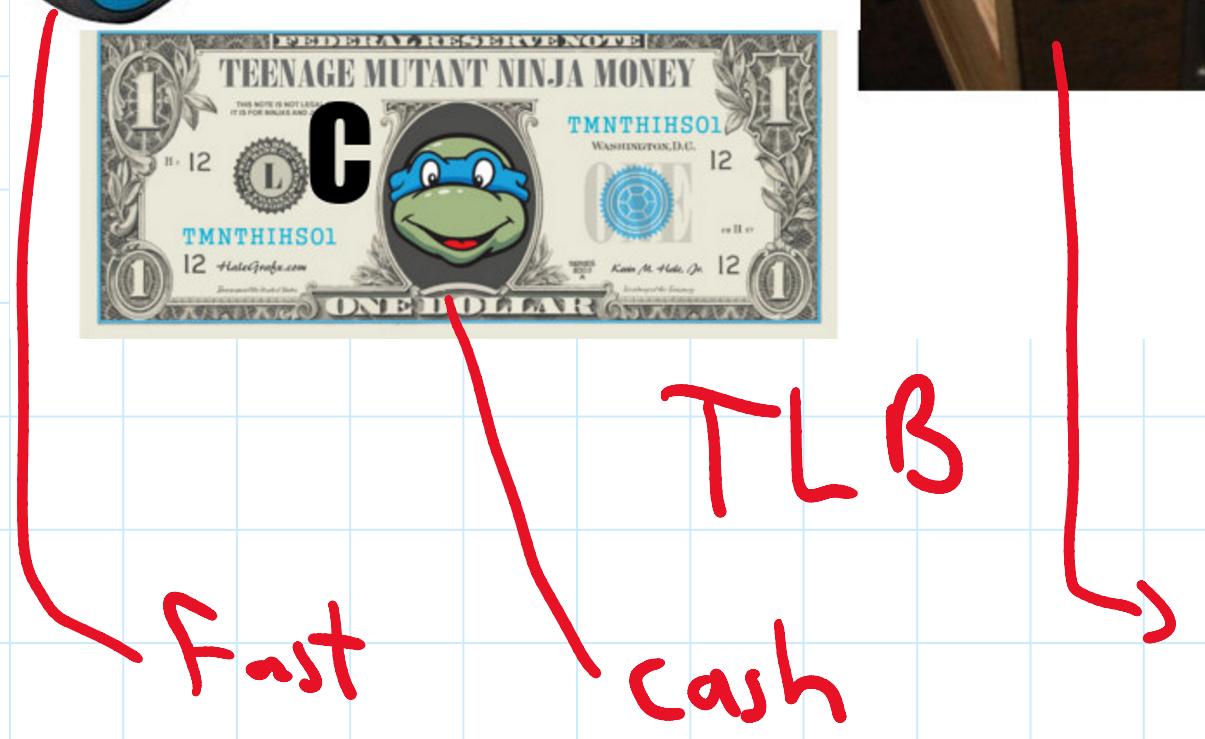
Page tables



B



little look up
table



• Fast

'Cash
Cache

where we store g.

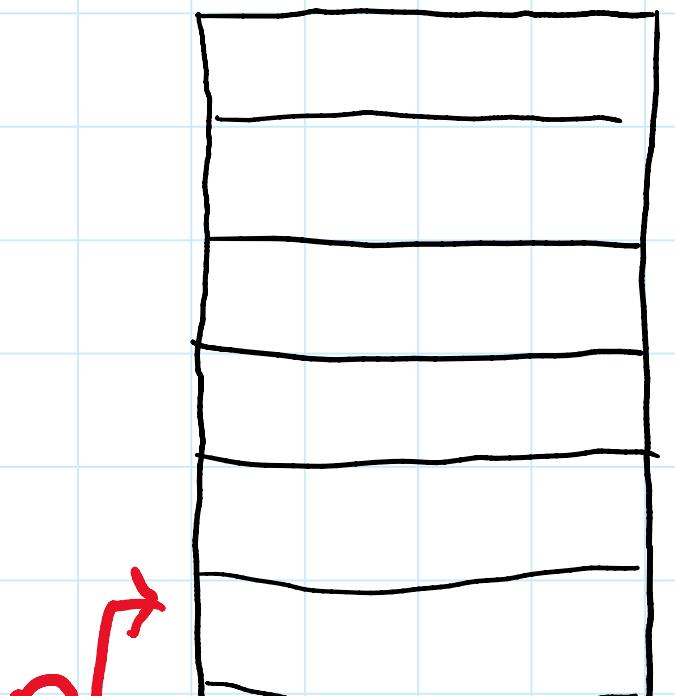
t

How do all of these pieces fit together?

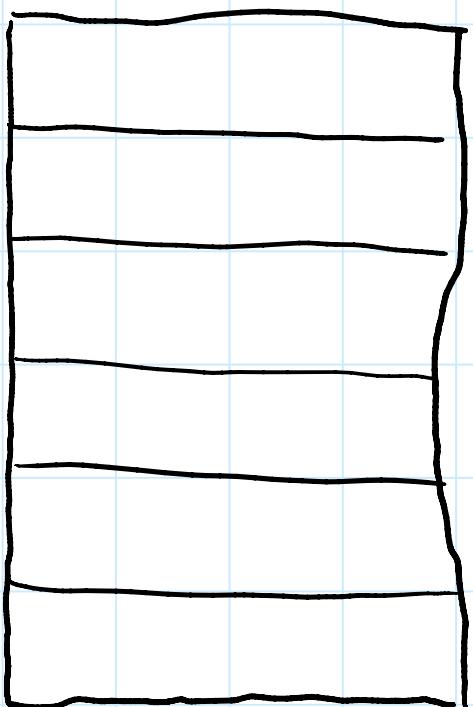
Page Table

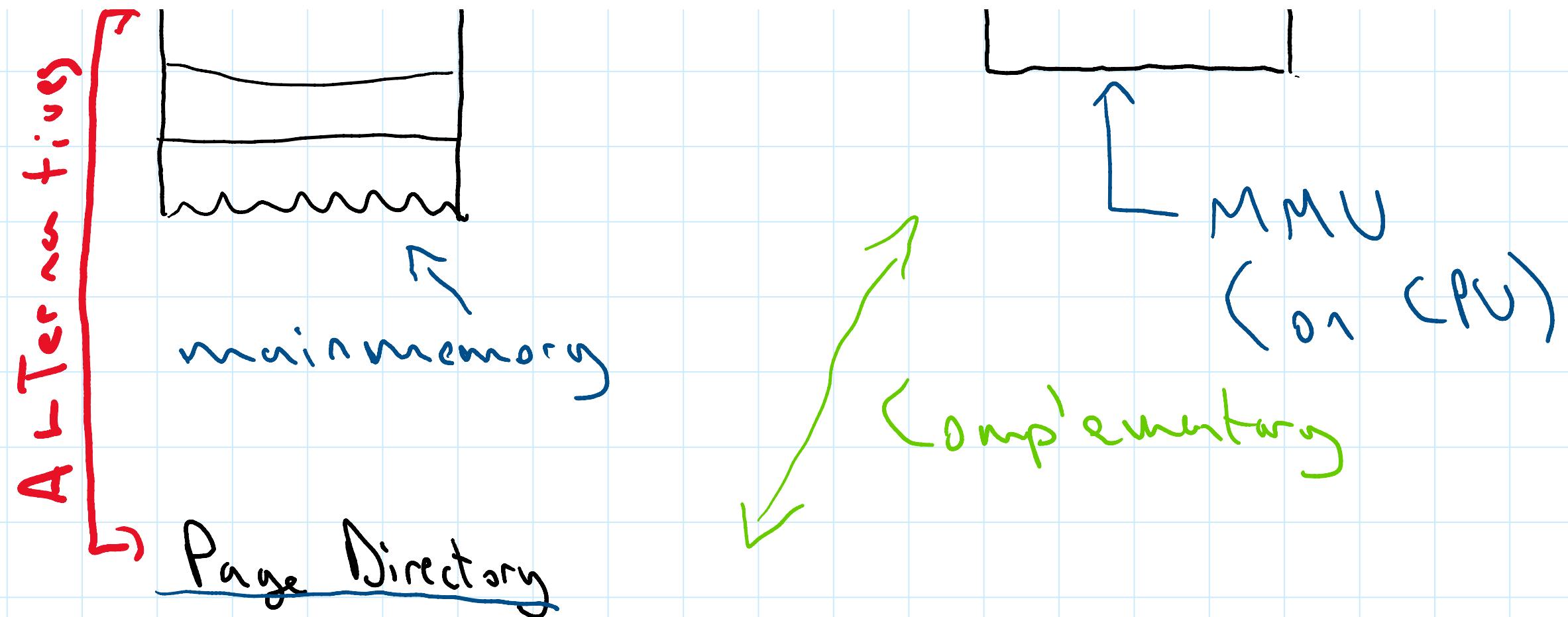
TLB

struct task_struct

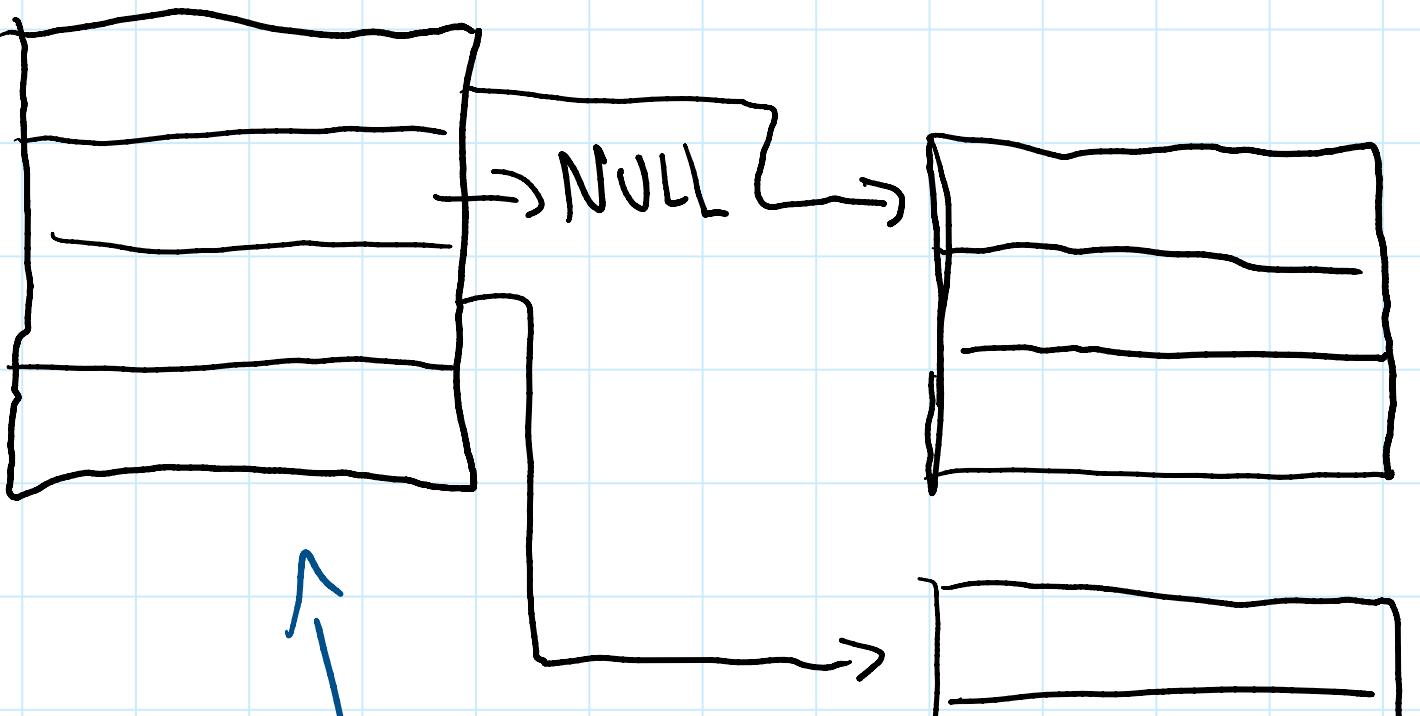


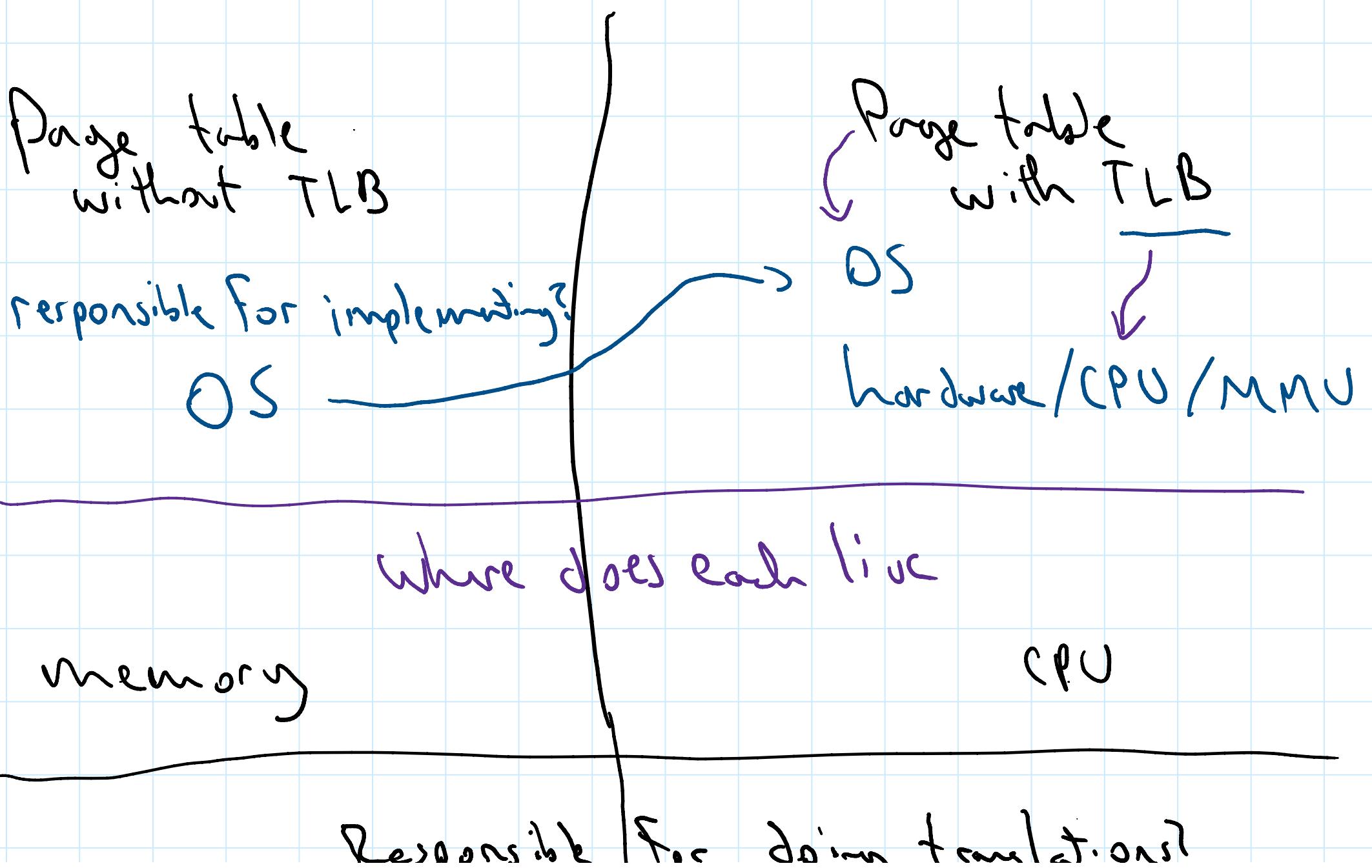
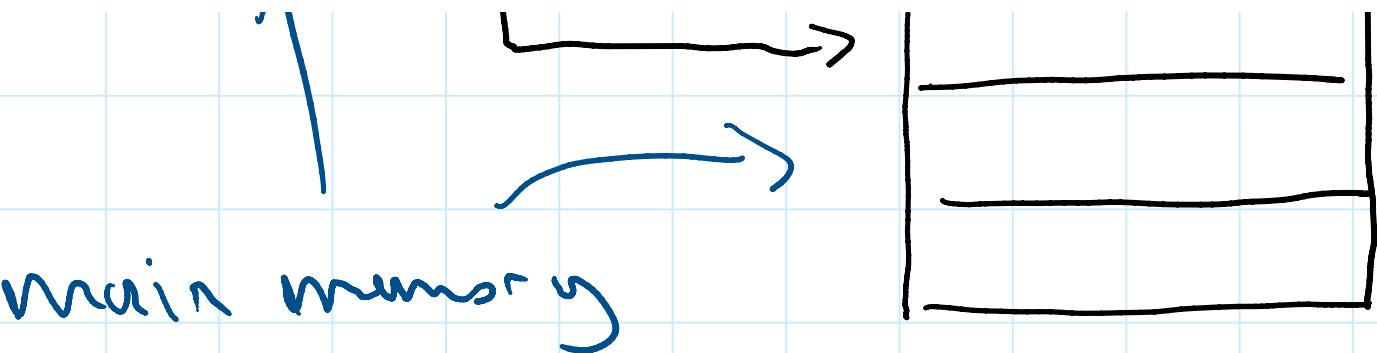
Complementary.
↔





struct task_struct





Responsible for doing translations?

hardware

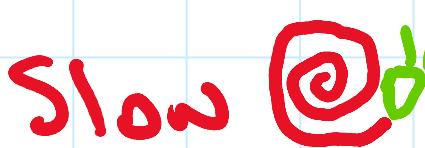
hardware

4. What happens during a translation with a TLB and without?

Page table without
TLB

ADD 10 [A]

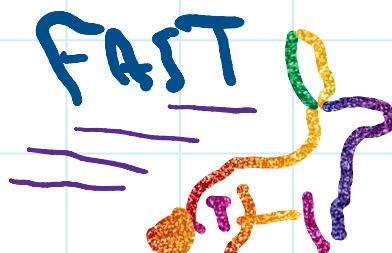
A has a virtual address 0x FFFF8

① Look up 0xFFFF in
pg table **SLOW** @

② Load from memory

Page table with TLB

① see if that translation
is in the buffer
(cache)



yes? great,

② Load from memory
conduct translation

no?

store translation
in cache

COMP 3430

Operating Systems

July 10th, 2019

Cache replacement policy evaluation

```
int sum = 0;  
for (int i = 0; i < 10; i++)  
    sum += a[i];
```

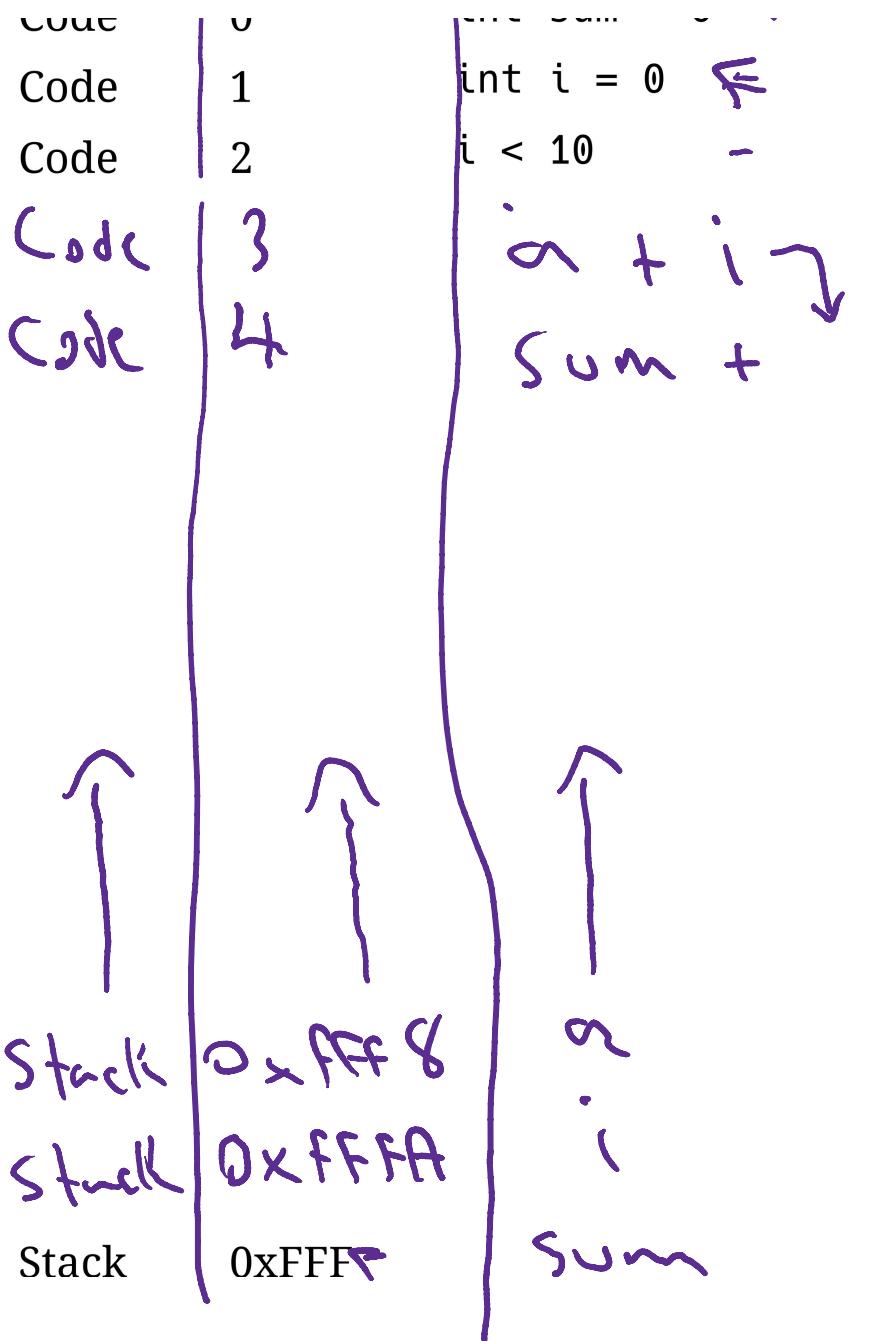
Virtual addresses

Section	Virtual address	Value
Code	0	int sum = 0
Code	1	int i = 0

TLB

Virtual	Physical
4	0xef12 60
3	0x4567 7
0xffff8	0<abcd 9
0xffffa	0xc0de 8





Physical