2.5D Integration Circuits

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1 Need for 2.5D IC's

The technical challenges of 2D scaling in CMOS technology are becoming evident as we reach the practical limits of planar features and new solution utilizing in a variety of ways the third dimension are becoming available at both the device and the package level.

1.1 Input Output Connections

Changes in the field of packaging are driven by I/O to increase the number of input output connections on the chip. The evolution from quadruple flat packages to flip chip ball grid array packages allowed the chip makers to support I/O connection in the range of 1000 to 1500 per chip. 2.5D will enable to increase the I/O connections.

1.2 System Performance

The overall system performance is limited by the bandwidth at which the CPU can communicate with the memory. The bandwidth, number of bits transferred, is limited by the interconnect between the memory and CPU.

$$B \propto \frac{A}{l^2} \tag{1}$$

Presently the interconnects are becoming skinnier, but longer. So 2.5D will enable to have an improved bit rate.

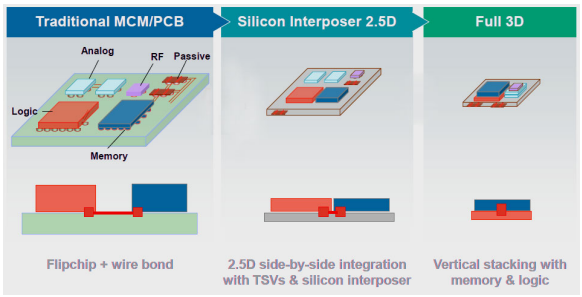

Figure 1: Evolution of different IC technology

1.3 Heterogeneous Integration

Heterogeneous Integration (HI) refers to the assembly and packaging of multiple separately manufactured components onto a single chip in order to improve functionality and enhance operating characteristics. Heterogeneous integration allows for the packaging of components of different functionalities, different process technologies, and sometimes separate manufacturers. This is achieved by stacking the different chips, but is limited by the process flow and varying voltage requirements such as those seen in modern mobile phones. Integration using 2.5D is suitable for such applications.

2 2.5D Technology

2.5D IC is a packaging technology where multiple die are placed face down and side by side on a silicon or organic interposer (Figure 1).An interposer is an electrical interface routing between one socket or connection to another. The purpose of an interposer is to spread a connection to a wider pitch or to reroute a connection to a different connection.

The active surface of the die has micro-bumps (Figure 4) which connect to pads on the surface of the silicon interposer. Connections from these pads, directly connect to TSVs (Through Silicon Vias) which pass through the interposer substrate and connect to the package substrate. The connections from the pads can also be connected through interposer routing to other TSVs that are in-turn connected to pads and micro-bumps of other die on the interposer.

2.5D IC technology helps reduce interconnection length between multiple dies assembled on interposer leading to lower power consumption and lower latency as well as increase the number of interconnection routes on the interposer which results in increased bandwidth compared to traditional 2D off-chip interconnections.

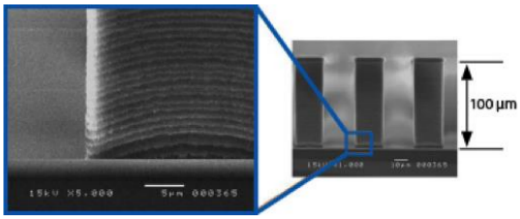

Figure 2: Via formation using deep reactive-ion etching

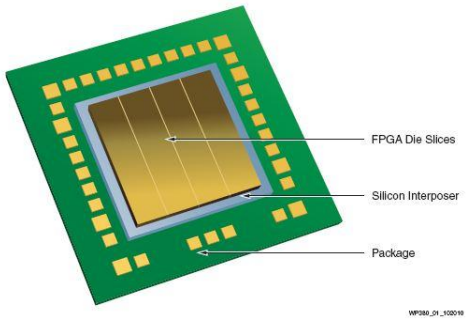

Figure 3: Top view of stacked silicon interconnect die

3 Silicon Interposer Fabrication

A great deal of resources have already been invested to bring TSV into a viable interconnect solution for both 2.5D interposers and 3D stacked-die assembly. In preparation for TSV, small diameter holes are first formed on one side of the silicon wafer. The most common process for this operation uses a deep reactive-ion etching (DRIE) process.(Figure 2)

The via ablation process is also known as 'pulsed' or 'time-multiplexed' etching, a process that alternates repeatedly between two modes to achieve nearly vertical hole structures. During the pulsed etching process a passivation layer is naturally formed onto the vias sidewall to block further chemical attack and to prevent additional etching within the via sidewall. These etch/deposit steps are repeated until the ablation reaches the desired depth. Although it is possible to etch via holes all the way through the silicon base, it is common practice to stop the etching process at a predetermined depth that will better promote via filling during the metalisation process.

4 Application

In 2011 Xilinx released the first commercially available 28nm, 2.5D Stacked Silicon Interconnect (SSI) (Figure 3) device (the Virtex-7 2000T FPGA)

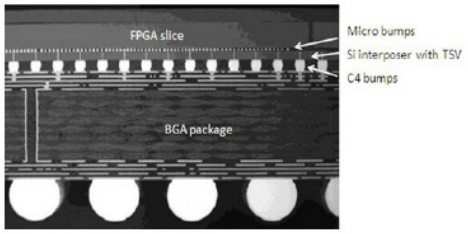

Figure 4: 2.5D interposer for Xilinx FPGA

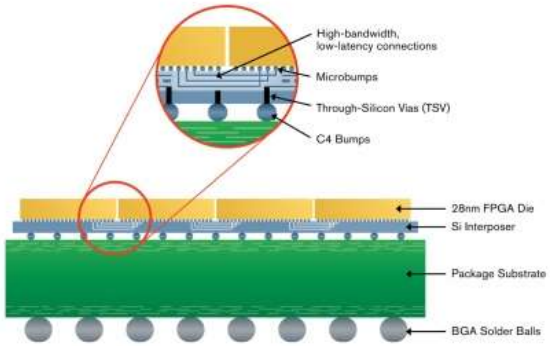

Figure 5: Package substrate

(Figure 4) followed by TSMC announcing full manufacturing and assembly support for 2.5D IC designs.

The use of silicon interposers for advanced packaging, first introduced as a product by Xilinx, used 2.5D integration. The introduction of product with 2.5D integration used a TSV interposer to connect multiple chips side by side and provide high bandwidth connections between the die, (Figure 5) RDL to map the die geometries to the printed circuit board geometries and TSVs to connect the top and bottoms layers of the interposer. The benefits of higher bandwidth, lower power and reduced latency are compelling and several other products are in development using this technology.

The initial selection of this packaging technology was driven by the need for improved performance and it was very successful in achieving that goal.

5 Advantages of 2.5D

The main advantages of this technology are

1. miniaturization
2. enhanced performance

Table 1: Comparison of 2.5D and 3D

	2.5D IC	3D IC
Design Flow	Evolutionary	New Co-Design
Device Impact	None	Stress
Thermal & Reliability	Evolutionary	Challenging
Testing	Evolutionary	New Methods

3. lower latency
4. increased bandwidth
5. power efficiency

2.5D technology allows that the die that are mounted on interposer need not utilize same process node or technology. This helps in using die manufactured in various technology nodes.

6 Challenges for 2.5D

In 2.5D the thermal density is increased, (total power generated per unit surface area) and the surface area to exhaust the heat is reduced, thus we require advanced heat dissipation techniques.

Driving the cost down for the 2.5D technology is a critical challenge since it not only delivers major performance advantages, it also drive the industry down the learning curve for the cost effective adoption for 3D-TSV.

The widespread adoption of this technology has not followed. The primary limitation was the high cost of the interposer incorporating TSVs.

7 2.5D vs 3D

2.5D has marked advantages of capacity, performance, system space and overall system power consumption over traditional single die implementations—3D promises to have even more. (Table 1)

7.1 Design Flow

2.5D method of placing die side by side on a passive interposer is very much like implementing discrete ICs on a printed circuit board but of course on a much smaller scale. True 3D will require a revisiting of the entire design flow.2.5D is much more evolutionary. You really have a much more traditional partitioning of your architecture than you do in 3D.

7.2 Device Impact

Signal and power integrity are both issues in 3D ICs and to a lesser extent in 2.5D. Noise management is an issue that needs to be addressed, power lines can be the source of interference and greatly affect performance and functionality.

7.3 Thermal and Reliability

Thermal tolerance is a concern in all advanced IC designs.Heating and cooling of die in the stack can also create mechanical stresses, as materials have different thermal coefficients of expansion . This becomes a greater concern as you place more die in a 3D stack, especially if those die are made of different materials.

7.4 Testing

2.5D hasn't required any radical changes to testing but 3D ICs will very likely require entirely new test structures as an issue where any defect in a layer of the 3D stack could make the entire device defective.

8 Summary

2.5D IC's offer flexibility to assemble off-the-shelf components onto 2.5D IC's and are desirable for a plethora of applications on mobile communication as well as for data centers/servers.The 2.5D method can allow companies to create devices that far exceed Moore's Law, by increasing the number of transistors on the chip using stacking.

The vision of a 3D IC is truly promising, but 2.5D IC technology is being dismissed as the stepping stone for true 3D design. 2.5D has the distinct advantage of being already available and adopting it will onlt take minor adjustments to current design flows and seemingly the manufacturing chain.