EC304 VLSI : Assignment 2 - CMOS Inverter

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1. Answer to question 1:

   By using C5 process technology scale of 0.3 microns, $L = 0.7\mu m$ means L_N has a scaling factor 2.34. And since $(\frac{W}{L})_N = 1$, $W_N = 2.34$. $(\frac{W}{L})_P = 3(\frac{W}{L})_N$ implies that $W_P = 7$ and $L_P = 2.34$.

   The transfer characteristics of the given inverter in figure 1 is given in figure 2.
   $V_{IL}, V_{IH}, V_{OL}, V_{OH}$ are found my marking the unity gain point where the slope is -1. From figures 3 and 4, marking unity slope gain, we get

   $$V_{IL} = 3.32V$$

   $$V_{IH} = 3.86V$$

   $$V_{OL} = 108mV$$

   $$V_{OH} = 4.74V$$

2. Answer to question 2:

   For $\frac{(\frac{W}{L})_P}{(\frac{W}{L})_N} = 15$, let $W_P = 150$ and $W_N = L_N = L_P = 10$
   From figures 5 and 6, we get

   $$V_{IL} = 3.30V$$

   $$V_{IH} = 3.69V$$

   $$V_{OL} = 198mV$$

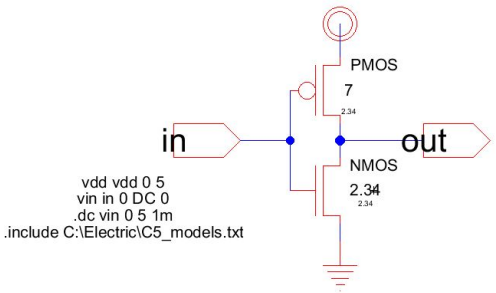

Figure 1: Schematic of inverter in question 1

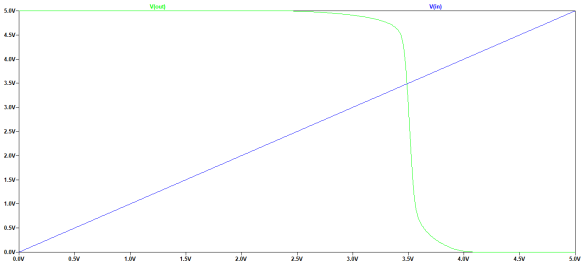

Figure 2: Transfer characteristics of inverter in question 1

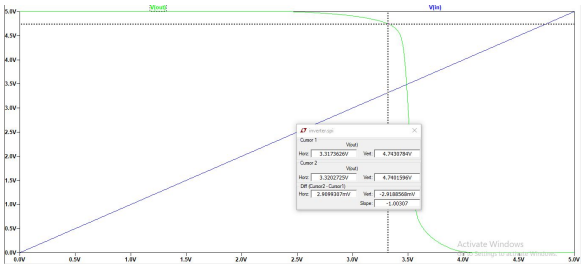

Figure 3: Unity slope gain of inverter in question 1

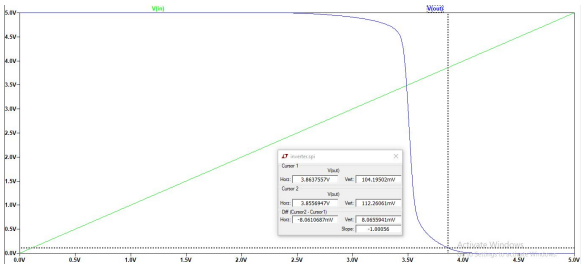

Figure 4: Unity slope gain of inverter in question 1

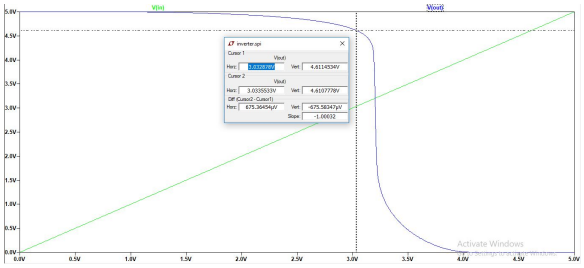

Figure 5: Transfer characteristics of inverter with $\frac{(\frac{W}{L})_P}{(\frac{W}{L})_N} = 15$

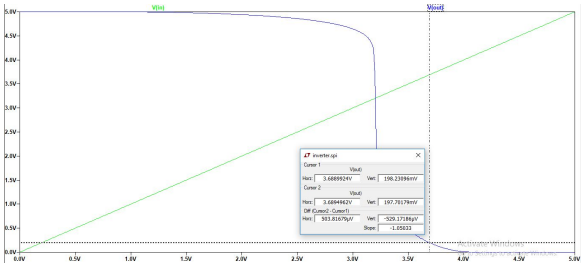

Figure 6: Transfer characteristics of inverter with $\frac{(\frac{W}{L})_P}{(\frac{W}{L})_N} = 15$

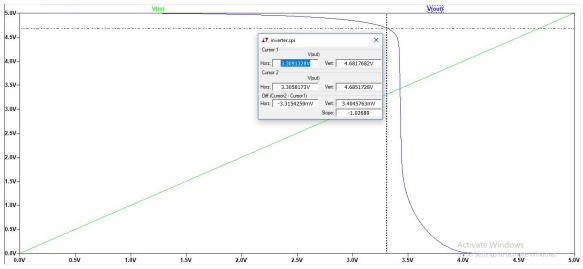

Figure 7: Transfer characteristics of inverter with $\frac{(\frac{W}{L})_P}{(\frac{W}{L})_N} = 30$

$$V_{OH} = 4.61V$$

For $\frac{(\frac{W}{L})_P}{(\frac{W}{L})_N} = 30$, let $W_P = 300$ and $W_N = L_N = L_P = 10$
From figures 7 and 8, we get

$$V_{IL} = 3.03V$$
$$V_{IH} = 3.88V$$
$$V_{OL} = 100mV$$
$$V_{OH} = 4.68V$$

From the simulation, $N_{ML15} = 3.102V$, $N_{MH15} = 920mV$ and $N_{ML30} = 2.93V$, $N_{MH30} = 800mV$. The differences, $V_{IH15} - V_{IL15} = 390mV$ and $V_{IH30} - V_{IL30} = 850mV$, it is desirable to have shorter intermediate region such as in $\frac{(\frac{W}{L})_P}{(\frac{W}{L})_N} = 15$. Also, $\frac{(\frac{W}{L})_P}{(\frac{W}{L})_N} = 15$ has higher noise immunity at the input and output.

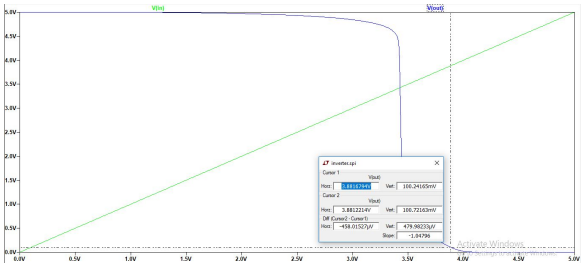

Figure 8: Transfer characteristics of inverter with $\frac{(\frac{W}{L})_P}{(\frac{W}{L})_N} = 30$

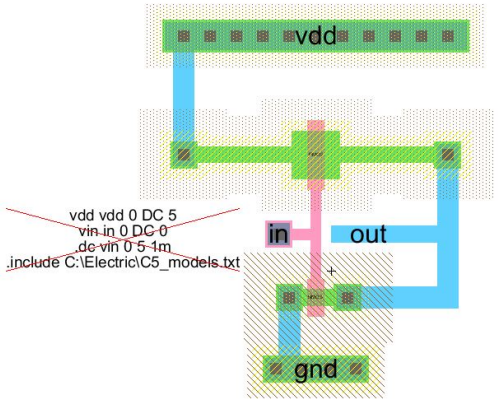

Figure 9: Layout of inverter in question 1

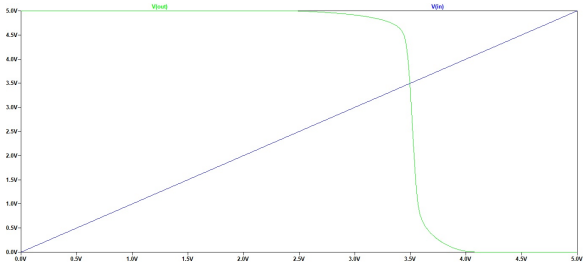

Figure 10: Transfer characteristics of layout

3. Answer to question 3: By changing the technology scale to $233.33\mu m$, and using the scaling factors, $W_N = 3, L_N = 3, W_P = 9, L_P = 3$ a layout of the inverter was made as in figure 9.

   From the simulation of the same, we get the following.

   From figures 12 and 11, we get the values

$$V_{IL} = 3.33V$$

$$V_{IH} = 3.86V$$

$$V_{OL} = 106mV$$

$$V_{OH} = 4.74V$$

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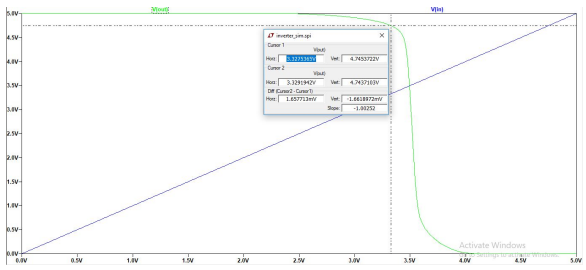

Figure 11: Transfer characteristics of layout

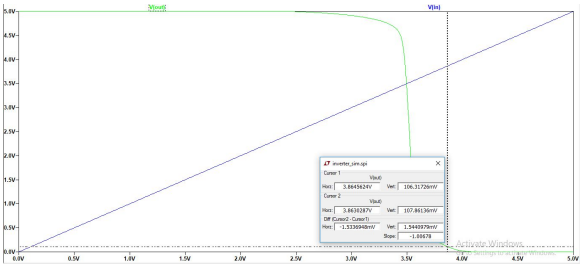

Figure 12: Transfer characteristics of layout

There is no significant difference between the voltages in the schematic and layout simulation, but it is seen that the intermediate region is slightly more in the layout than the schematic, reducing its noise immunity.