
Streaming MANN: A Streaming-Based Inference for Energy-Efficient Memory-Augmented Neural Networks

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Abstract

With the successful development of artificial intelligence using deep learning, there has been growing interest in its deployment. The mobile environment is the closest hardware platform to real life, and it has become an important platform for the success or failure of artificial intelligence. Memory-augmented neural networks (MANNs) are neural networks proposed to efficiently handle question-and-answer (Q&A) tasks, well-suited for mobile devices. As a MANN requires various types of operations and recurrent data paths, it is difficult to accelerate the inference in the structure designed for other conventional neural network models, which is one of the biggest obstacles to deploying MANNs in mobile environments. To address the aforementioned issues, we propose Streaming MANN. This is the first attempt to implement and demonstrate the architecture for energy-efficient inference of MANNs with the concept of streaming processing. To achieve the full potential of the streaming process, we propose a novel approach, called inference thresholding, using Bayesian approach considering the characteristics of natural language processing (NLP) tasks. To evaluate our proposed approaches, we implemented the architecture and method in a field-programmable gate array (FPGA) which is suitable for streaming processing. We measured the execution time and power consumption of the inference for the bAbI dataset. The experimental results showed that the performance efficiency per energy (FLOPS/kJ) of the Streaming MANN increased by a factor of up to about 126 compared to the results of NVIDIA TITAN V, and up to 140 if inference thresholding is applied.

1 Introduction

The use of deep learning applications has been expanding into mobile environments. Because of the demand for extensive computing and storage resources which overwhelms the capacity of mobile devices, conventional implementations often take advantage of servers to train and infer the deep learning models. This suggests several problems: 1) expensive and frequent network communications, 2) network-dependent performance, and 3) high maintenance expenditure of service providers. Thus, extensive studies for on-device inference have been suggested [1–7].

In order to develop efficient inference methods for mobile devices with low latency and energy consumption, it is beneficial to utilize the concept of streaming processing, as in a dataflow architecture (DFA). In DFAs, data flows through processing elements (PEs), which can reduce the amount of memory access which is a major cause of energy consumption [8]. In addition, DFAs can exploit fine-grained parallelism, which enables the efficient implementation of layer-wise parallelization and recurrent paths. Hence, there are a number of studies applying the features of DFAs for efficient inference in resource- and energy-restrictive mobile environments [6, 9–15].

Memory-augmented neural networks (MANNs), including Neural Turing Machine [16], Memory Networks [17], and Differential Neural Computer [18], are neural network models based on recurrent neural networks (RNNs) with external memories. The external memory increases the learning capacity of the models. Unlike other artificial neural networks (ANNs), MANNs require both recurrent and memory operations, such as addressing, read, and write, in each layer. In addition, because the amount of external memory used is dynamically determined, parallel computation is difficult in the memory operations. Due to the recurrent path and dynamically determined memory usage, the inference of MANNs is difficult to optimize for both CPU and GPU.

In this paper, we propose Streaming MANN that is based on DFA for the energy-efficient inference. The proposed architecture utilizes the characteristics of natural language processing (NLP) task which is one of the major applications for MANNs. Furthermore, we propose inference thresholding with an efficient index order. By applying this approach to Streaming MANN, we can reduce the operation time of the output layer which can cause a serious performance degradation, especially in large-class tasks.

A field programmable gate array (FPGA) is an appropriate hardware platform for Streaming MANN because of its streaming, synchronous, and static nature. Hence, we implemented the proposed architecture with the inference thresholding in FPGA, to evaluate our approaches for energy-efficient inference by measuring the actual inference time and power consumption. In comparison, Streaming MANN outperforms the GPU in energy efficiency (FLOPS/kJ) by a factor of up to 126 on the bAbI dataset [19] and approximately 140 with the inference thresholding. The contributions of this paper are as follows:

- **Streaming-based architecture for MANNs** We propose Streaming MANN which is a streaming-based inference architecture. This work is the first attempt towards energy-efficient inference for MANNs.
- **Fast inference method using Bayesian approach** We suggest inference thresholding to reduce the inference time in the proposed architecture.
- **Implementation and validation** We implemented the proposed approaches in FPGA. To validate the energy efficiency, we measured the inference time and power consumption.

2 Related Work

2.1 Memory-Augmented Neural Networks (MANNs)

MANNs were proposed to efficiently perform intriguing tasks, such as question and answer (Q&A) and algorithms, by increasing the storage capability of RNNs [16–18]. A MANN consists of the external memory and its controller; it learns how to read and write information in the memory through data. Although most studies have only focused on improving the performance of MANNs across various tasks, only a few studies have been conducted on an architectural exploration of MANNs in search of efficient operation.

The only relevant research to date is from [2] which applied quantization to MANNs and also presented a novel memory addressing method that is robust to the quantization error. Although a quantization method can reduce the energy consumption substantially in both training and inference, their approach was focused mainly on the efficient training of a quantized MANN. Moreover, the analysis of the energy consumption was based on calculations, rather than actual measurements. Thus, there is still a need for improvement in the inference efficiency.

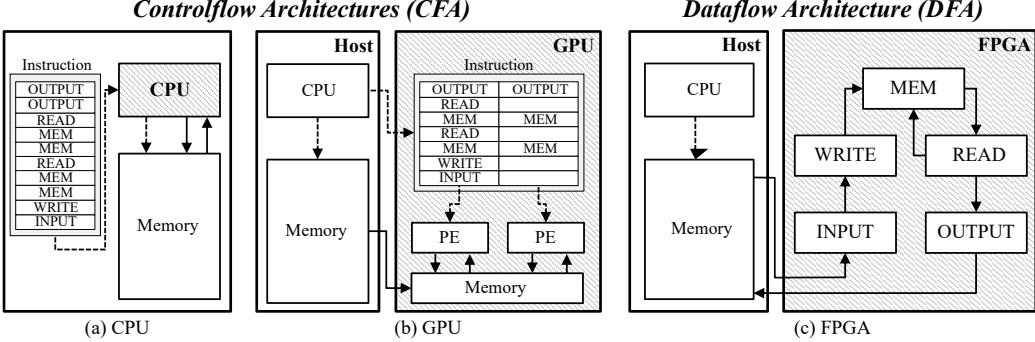


Figure 1: An example of inference for a MANN in various architectures. The operation can be divided into several modules: INPUT, WRITE, MEM, READ, and OUTPUT. Arrows, dotted lines, and solid lines represent the operation dependency, controlflow, and dataflow, respectively. Assuming that MEM and OUTPUT consume two instructions and the other modules consume one instruction, (a) the CPU operates sequentially, and (b) the GPU can perform parallel operations on multiple PEs with inefficiency. (c) FPGAs can implement fine-grained parallelism and recurrent paths efficiently [20].

2.2 Controlflow vs. Dataflow Architecture

As depicted in Fig. 1, modern computer architecture can be divided into controlflow and dataflow architecture. Controlflow architecture (CFA) controls the operation of PEs through instructions while using shared memory to hold instructions and data. There are two main architectures of CFA: CPUs and GPUs as depicted in Fig. 1-(a) and -(b), respectively. The GPUs, which offer a high degree of parallelism, are well-suited for deep learning training, where the matrix multiplications account for most of the operations. Hence, deep learning frameworks, such as Tensorflow [21] and Caffe [22], provide GPU implementations of different ANN models in order to speed up the training process.

Although GPUs are a perfect fit for training deep learning models, they are inefficient in inference when compared to DFA. This inefficiency becomes clear in MANNs, wherein each layer requires different types of computations. In such a case, PE utilization becomes lower, as shown in Fig. 1-(b). The data movement between the HOST and GPU is inevitable but results in huge performance degradation, especially in the inference process, where the data is used only once. Thus, DFA-based architectures are well-suited for the inference in a MANN, as shown in 1-(c).

The DFA offers several advantages to be applied to the inference in MANNs: 1) It can support streaming-based processing which can transfer data between layers without memory access. 2) It allows the efficient implementation of recurrent connections. 3) It provides fine-grained parallelism, which can enable efficient computing in the case where each layer requires various kinds of computations [20, 23].

2.3 Efficient Inference Methods for Deep Neural Networks

Efficient inference methods of deep neural networks for restrictive environments, such as mobile devices and embedded hardware platforms, have been covered extensively in the literature [2, 6, 9–15, 24–26]. These studies focused primarily on energy-efficient inference from the both algorithmic and architectural perspectives.

Algorithmic approaches to efficient inference mainly aimed to reduce the model size and the complexity of computation by sparsity or bit-width optimization [2, 24, 25]. On the other hand, DFA-based architectures have been proposed to improve the efficiency of inference. Several studies [6, 10–12] proposed architectures that could efficiently perform matrix multiplications to accelerate the inference speed in CNN models. Furthermore, [6, 9, 13–15] presented efficient inference architectures that considered RNN models, such as LSTM [27] and GRU [28]. However, there are few studies on the efficient inference of MANNs. Quantized MANN [2] was proposed in order to reduce the model size and computations, but there is no additional consideration on the energy-efficient inference.

In a large-class problem (e.g., NLP), parallelism can be troublesome as the output layer demands a significant amount of hardware resources [29]. To overcome such limitations, [30–33] aimed to reduce the amount of computation at the output layer. These studies have tended to focus on

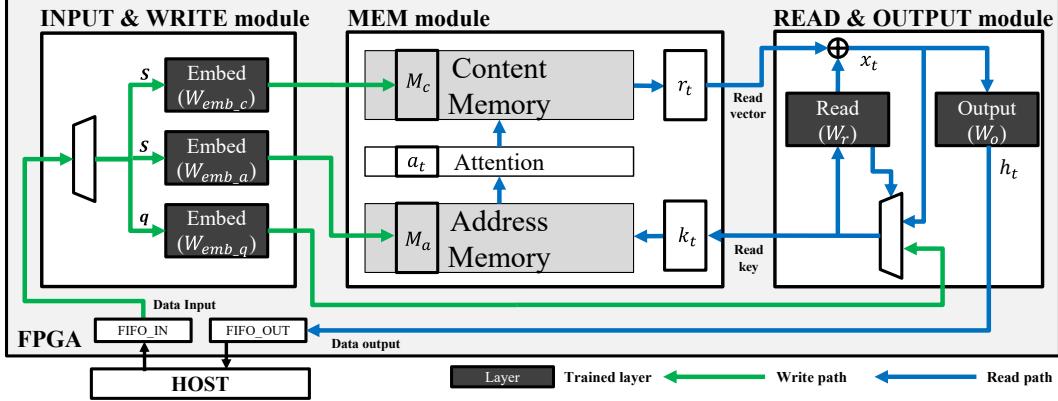


Figure 2: Architecture of Streaming MANN

approximating softmax operations through sampling and hierarchical structures. Shim et al. [34] claimed to improve the inference speed by applying singular vector decomposition in the output layer. However, it required the memory access for reading all of the weight indices, and this raised serious concerns about the memory-access time and energy consumption.

3 Proposed Approach

3.1 Streaming Memory-Augmented Neural Networks

In this paper, we propose a DFA-based architecture for energy-efficient inference of MANNs, called Streaming MANN. The details of the proposed architecture and the data flow are depicted in Fig. 2. The operations in the inference of the MANN include the INPUT, WRITE, MEM, READ, and OUTPUT module, and each module requires different types of arithmetic operations (Supp. C). First, Streaming MANN receives inference data and trained models (W_{emb} , W_r , W_o) from the HOST in the form of streams via a FIFO. The received data and the pre-trained model are passed to each module through the specified datapath, as shown in Fig. 2. The HOST controls the operations of the proposed architecture through the data. For example, in a Q&A task, the data is passed along the write path, as sentences (S) that are the context of Q&A task and a question (q) are transferred in the stream format. When the input data stream is finished, the READ module generates a read key (k_t), and the MEM module uses this key to read a vector (r_t) from the content memory. The READ and OUTPUT modules can read the content memory recurrently from the MEM module because they are composed of RNNs. After several read operations, the OUTPUT module sends an answer for the question to the HOST though the FIFO.

In an NLP task, which is one of the main applications of a MANN, discrete and sparse word vectors (e.g., bag-of-words) are converted into dense embedded vectors through the embedding layer. Thus, if we use the word vectors as the input of the proposed architecture, the efficiency of the embedding operations in the INPUT and WRITE modules can be improved, as in [6]. The embedding operation using the properties of the input vector can be described as follows:

$$S_E = \text{Embed}(S) = W_{emb}S = W_{emb}(\sum_{\text{idx} \in S} e_{\text{idx}}) = \sum_{\text{idx} \in S} W_{emb,\text{idx}}, \quad (1)$$

where S is the input vector, S_E is the embedded vector, Embed is the embedding layer, W_{emb} is the embedding weight, idx is an index of word in the sentence, and e_{idx} is a basis vector of the index. Using Eq. 1, we only need to read the columns of the embedding weight corresponding to the indices in the embedding weight. This leads to a reduction in the amount of memory access for reading the embedding weights and multiplication for calculating embedding vector. Thus, the embedding layer (Embed) can be implemented with low energy consumption, if a stream of word indices is used as the input of the proposed architecture based on DFA.

The MEM module consists of the address memory that supports content-based addressing and the content memory that generate a read vector (r_t) by soft-addressing based on the attention (a_t) from the address memory. Since the MEM module requires the operations that demand considerable hardware

Algorithm 1: Inference Thresholding

Input : Training dataset $\mathcal{D} = \{x_n, y_n\}_{n=1}^N$, Inference dataset $\tilde{\mathcal{D}} = \{\tilde{x}_n, \tilde{y}_n\}_{n=1}^{\tilde{N}}$, Output : Inferred label \hat{y} Notations: H, \tilde{H} : Hypothesis (training, inference dataset), $p(H_i max_i)$: PDF of H_i when $i = arg max_k H_k$, M : Pre-trained model, I : Dimension of output vector, θ : Inference threshold, ρ : Thresholding constant, A : Address table, HG : Histogram Step 1: Estimate the hypothesis distributions for (x_s, y_s) in \mathcal{D} do $H \leftarrow$ Do forward pass $M(x_s)$ $y \leftarrow arg max_i H_i$ if $y == y_s$ then for i in $1 : I$ do if $i == y$ then Update $HG_{max_i} \leftarrow H_i$ else Update $HG_{non-max_i} \leftarrow H_i$ end end end end	for i in $1 : I$ do Estimate $p(H_i max_i)$ from HG_{max_i} end Step 2: Set the inference thresholds $p(max_i H_i) \leftarrow p(H_i max_i)p(max_i)$ for i in $1 : I$ do $\theta_i \leftarrow min(\{H_i p(max_i H_i) \geq \rho\})$ end Step 3: Set the efficient index order for i in $1 : I$ do $S_i \leftarrow$ Silhouette of $\{HG_{max_i}, HG_{non-max_i}\}$ end $A \leftarrow$ sorted indices by S_i in descending order Step 4: Apply inference thresholding for $(\tilde{x}_s, \tilde{y}_s)$ in $\tilde{\mathcal{D}}$ do Do forward pass $M(\tilde{x}_s)$ until output layer for i in $1 : I$ do if $\tilde{H}_i > \theta_i$ then return $\hat{y} \leftarrow i$ end end return $\hat{y} \leftarrow arg max_i \tilde{H}_i$ end
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cost such as softmax, it is not suitable for exploit sufficient parallelism. Thus, we implemented the MEM module with element-wise sequential operations exploiting fine-grained parallelism.

The READ and OUTPUT modules consist of RNNs. The READ module generates a read key value (k_t) to calculate the attention (a_t) in the MEM module and receives a read vector (r_t) as an input. As highlighted in the read path (blue line) of Fig. 2, such recurrent path can be implemented efficiently. The OUTPUT module calculates the hypothesis (H) based on the read vector. The hypothesis can be obtained by matrix multiplication of the input vector (x_t) and the weight of the output layer (W_o). The matrix multiplication can be implemented as a series of dot products because the parallelism of the operation is hard to exploit with the large dimensions in a limited-resource environment. Thus, in the OUTPUT module of the proposed architecture, each index's hypothesis is sequentially calculated, which takes a considerable part of the total inference time.

3.2 Inference Thresholding

If a MANN is implemented based on DFA, we can efficiently exploit the fine-grained parallelism of each layer. However, in the case of a NLP task where the dimension of output (I) is much larger than that of embedding (E), it is hard to parallelize the operations at the output layer [29]. Thus, when calculating the hypothesis vector (H) in the output layer, we must sequentially calculate each index's hypothesis (H_i), as shown in Fig. 3-(a). In this case, the hypotheses (H_i) of all the indices (i) are obtained by sequentially calculating the dot product of the input (X) and the weight vector corresponding to the index (W_i). Because the operation time of the output layer is $O(I)$, the total inference time increases when I gets larger.

In this paper, we propose a method to shorten the inference time by applying inference thresholding based on Bayesian approach when calculating the output layer sequentially. The inference thresholding was motivated from our observations on the hypothesis distribution of the trained model. After finishing the training, the hypothesis (H_i) was observed to be fitted to the mixture models, as shown by the histograms in Fig. 3-(b) (Supp. B). To predict if the hypothesis (H_i) was the maximum value in the hypothesis vector (H) of the inference, we assumed that there were two different distributions: one in which hypothesis was the maximum value among hypothesis vector of the inference and the other in which hypothesis (H_i) was not. From this assumption, we could estimate conditional probability density functions (PDFs), $p(H_i|max_i)$, by using kernel density estimation (Algo. 1, Step 1). The PDFs obtained from the training dataset can be approximated as those of the inference dataset.

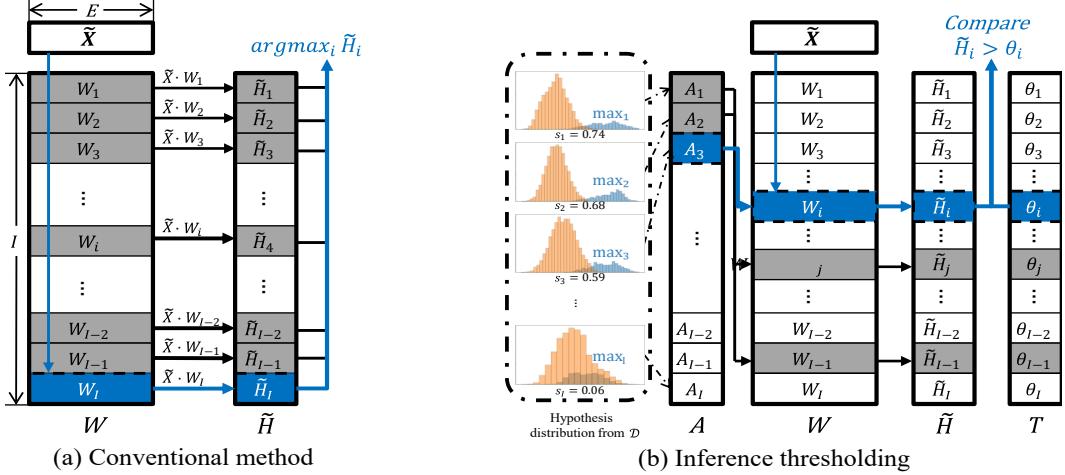


Figure 3: Hypothesis calculation of output layer. (a) Conventional method: We need to calculate the hypothesis of all the indices to find the index with max value among all hypothesis. In this case, if i is large then the inference takes a long time. (b) Inference thresholding: In the case of $H_i > \theta_i$, we can stop the inference by estimating index i as the index of the hypothesis with the max value. In addition, the inference time can be shortened further by applying an efficient index order.

Applying Bayesian approach to the approximated PDFs, we can infer the posteriors of the hypothesis for the inference dataset as follows:

$$p(\max_i | \tilde{H}_i) \approx p(\max_i | H_i) \propto p(H_i | \max_i) P(\max_i), \quad (2)$$

where $P(\max_i)$ is the probability that the hypothesis of the index (i) is the maximum value among the hypothesis vector (H) and H and \tilde{H} are the hypothesis vectors of the training and inference dataset, respectively. From Eq. 2, we can estimate the probability that the hypothesis (\tilde{H}_i) is a maximum value of the hypothesis vector (\tilde{H}) in the inference.

In order to reduce the inference time by applying the estimated value to the inference process of the output layer, the computational overhead required for the estimation should be sufficiently small. Thus, we set the threshold as a hypothesis value in which the estimated posterior probability is larger than a certain probability, as follows:

$$\tilde{H}_i > \theta_i \approx \min(\{H_i | p(\max_i | H_i) \geq \rho\}), \quad (3)$$

where ρ is a thresholding constant (Algo. 1, Step 2). With this straightforward operation that compares the hypothesis of inference with the pre-set threshold value from Eq. 3, we can approximately determine whether the hypothesis is the answer or not. Hence, we halted the sequential computation of $\tilde{X} \cdot W_i$ when the Eq. 3 is satisfied. This inference thresholding can reduce the amount of memory access and computation to shorten the operation time of the output layer (Fig. 3-(b)) without any degradation in the accuracy of the inference.

3.3 Efficient Index Order for Inference Thresholding

Inference thresholding is an inference method without sequential calculation of every element in the hypothesis. If we can sort indices in order of increasing thresholding effect, the benefit of inference thresholding will be substantially greater. Thus, we propose an efficient index order method for inference thresholding. The inference thresholding of each hypothesis can be regarded as a binary clustering problem, whether the hypothesis belongs to the class of \max_i or not. The inference thresholding will be more effective for indices whose inter-class distance is large and intra-class distance is small. Hence, we sorted the indices by a silhouette [35] values in descending order, so that we can achieve more reliable inference thresholding (Algo. 1, Step 3).

The proposed inference thresholding, combined with efficient index order, is illustrated in Fig. 3 and Algo. 1. Fig. 3-(a) describes the conventional method that computes each hypothesis in the order of

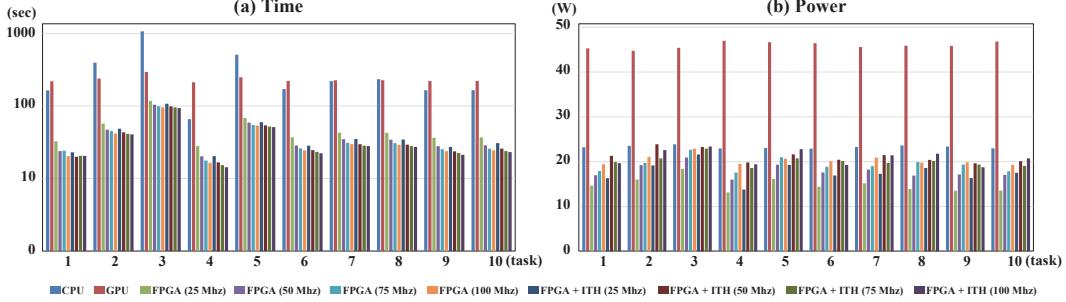


Figure 4: Measurement results of the inference on the bAbI dataset (task 1—10) for various configurations (ITH: inference thresholding).

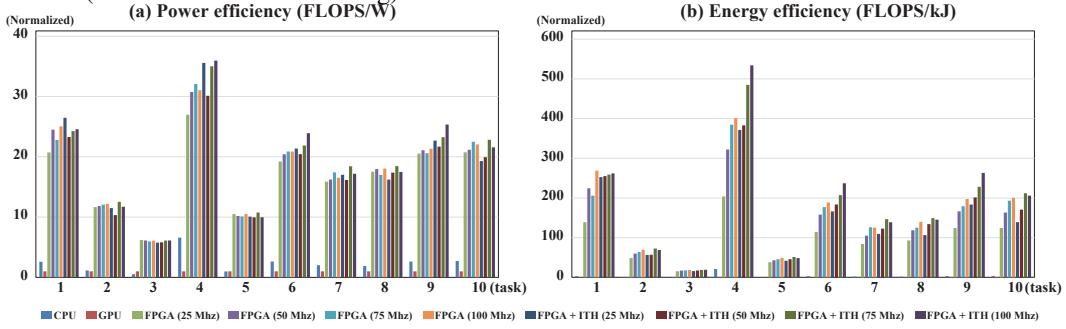


Figure 5: Efficiency of the inference on the bAbI dataset (task 1—10) for various configurations (ITH: inference thresholding).

output index (i) when it is not possible to parallelize the matrix multiplication of the input vector (X) and weight matrix of the last layer (W). In this case, we must calculate the entire hypotheses in order to find the index of the maximum hypothesis value. When I is large, this can cause a serious delay in inference. On the other hand, the proposed method speeds up the inference without any degradation of accuracy by using the efficient index order, as described in Fig. 3-(b).

4 Experimental Results

We implemented the proposed structure and method in FPGA to evaluate its performance. The experiments were performed to measure the inference time and power consumption in HOST (CPU), HOST-GPU, and HOST-FPGA configurations, as shown in Fig. 1. We implemented the optimized model for each configuration. The latest CPU (Intel Core i9-7900X) and GPU (NVIDIA TITAN V) were used for the experiments in order to fairly compare the inference efficiency of the proposed architecture implemented in FPGA (Xilinx Virtex UltraScale VCU108 board).

The inference time and power measurements contained all the parts consumed for the inference, including the transmission of the pre-trained model and inference data to the GPU and FPGA. For accurate measurements in each task, we calculated the average of the inference time for 100 repetitions and that of power for 5 min, respectively. We verified the performance of a MANN implemented in each configuration with the bAbI dataset [19] which is widely used in Q&A tasks. We implemented FPGA with various clock frequencies of 25, 50, 75, and 100 MHz to evaluate the effect of the HOST-FPGA interface and energy-efficient configuration. Please refer to the Supp. A for the measurements of inference time, power, and actual picture of implementation.

The inference time and power measured in each configuration with various tasks are shown in Fig. 4. In most tasks, Streaming MANN implemented in FPGA showed the fastest performance, and the inference time was reduced further when inference thresholding was applied. The GPU showed similar inference times between tasks due to the large data-transfer overhead. Fig. 4-(b) shows that the GPU consumed more power than the other configurations. The efficiency of the inference was evaluated in terms of power and energy, and each value was normalized to that of the GPU (Fig. 4). As depicted in the figure, Streaming MANN implemented in FPGA showed much higher inference efficiency than the models implemented in both CPU and GPU.

Table 1: Experimental results of the inference on the bAbI dataset for various configurations and the performance efficiency gain (ITH: Inference thresholding)

Configurations	Measurement (avg.)			Gain ^a		
	Time (s)	Power (W)	Energy (kJ)	FLOPS	FLOPS/W	FLOPS/kJ
CPU	242.767	23.275	5.650	0.935	1.822	1.703
GPU	226.904	45.363	10.293	1.000	1.000	1.000
FPGA (25 MHz)	43.544	14.708	0.640	5.211	16.071	83.744
FPGA (50 MHz)	34.954	17.527	0.613	6.492	16.801	109.062
FPGA (75 MHz)	31.960	19.017	0.608	7.100	16.936	120.236
FPGA (100 MHz)	30.284	20.097	0.609	7.493	16.912	126.719
FPGA + ITH (25 MHz)	35.364	17.355	0.614	6.416	16.771	107.611
FPGA + ITH (50 MHz)	30.813	20.106	0.620	7.364	16.615	122.350
FPGA + ITH (75 MHz)	29.183	20.183	0.589	7.775	17.475	135.872
FPGA + ITH (100 MHz)	28.533	20.528	0.586	7.952	17.573	139.745

^a normalized to the result of GPU

For each configuration, the average values of the measurement results with all tasks are listed in Tab. 1. The proposed architecture implemented in FPGA was 5.211 times faster than that of the GPU at the lowest operating frequency (25 MHz) and 7.493 times faster at the fastest operating frequency (100 MHz). We applied inference thresholding to Streaming MANN to reduce the inference time without a loss of accuracy. When the inference thresholding was applied, there was a decrease of about 18 % in the inference time at the low operating frequency (25 MHz) and about 6 % in high operating frequency (100 MHz). Compared to the results of GPU, the inference speed was improved by a factor of up to about 8.

We measured the dynamic power consumption in each experiment to obtain the energy consumption of the inference. As a result of the measurement, the GPU showed the highest power consumption and the FPGA with low operating frequency (25 MHz) consumed the lowest power. The GPU had a shorter inference time than the CPU, but it consumed more energy. Thus, the CPU was 1.7 times more efficient than the GPU in terms of performance per energy (FLOPS/kJ). Streaming MANN could improve the performance per energy by more than 74 times compared to the GPU. Furthermore, we could achieve an energy efficiency up to 140 times that of the GPU by applying inference thresholding.

5 Discussion

The benefit of inference thresholding was emphasized at a low operating frequency. At a low operating frequency (25 MHz), the performance per energy increased by approximately 28% whereas 6% at a high operating frequency (100 MHz). This indicates that as the operating frequency increases, the inference time is bounded by the interface between HOST-FPGA. These findings suggest that higher interface speed can achieve better performance. According to our analysis, we can expect that proposed approach surpasses the GPU by 162 times in energy per performance efficiency, if the inference performance is not bounded by the interface speed. The inference thresholding did not have a significant effect on the inference time in the CPU or GPU environments. This is because, in the CPU, the output layer only occupies a small portion of the overall inference computation, whereas the GPU has the capability to parallelize the output layer efficiently.

6 Conclusion

To the best of our knowledge, this work is the very first attempt to perform energy-efficient inference in MANNs. We proposed an architecture and formulated a novel algorithm, which are called Streaming MANN and inference thresholding, respectively. A proposed architecture based on DFA enables high levels of parallelism that can enhance the performance of models, such as MANNs, where different computations are required in each layer. In addition, we can efficiently speculate the index with the maximum hypothesis value by applying inference thresholding to the output layer which is difficult to parallelize. This enables energy-efficient inference by shortening the inference time while maintaining the accuracy with a small computational overhead. This work has revealed that complex tasks, such as Q&A, can be employed in a mobile device by adopting our proposed architecture.

Finally, the proposed inference thresholding method can be adopted to perform a large-class task without a significant computational overhead.

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Supplementary Material

A Experimental Results

A.1 Power Measurement Method

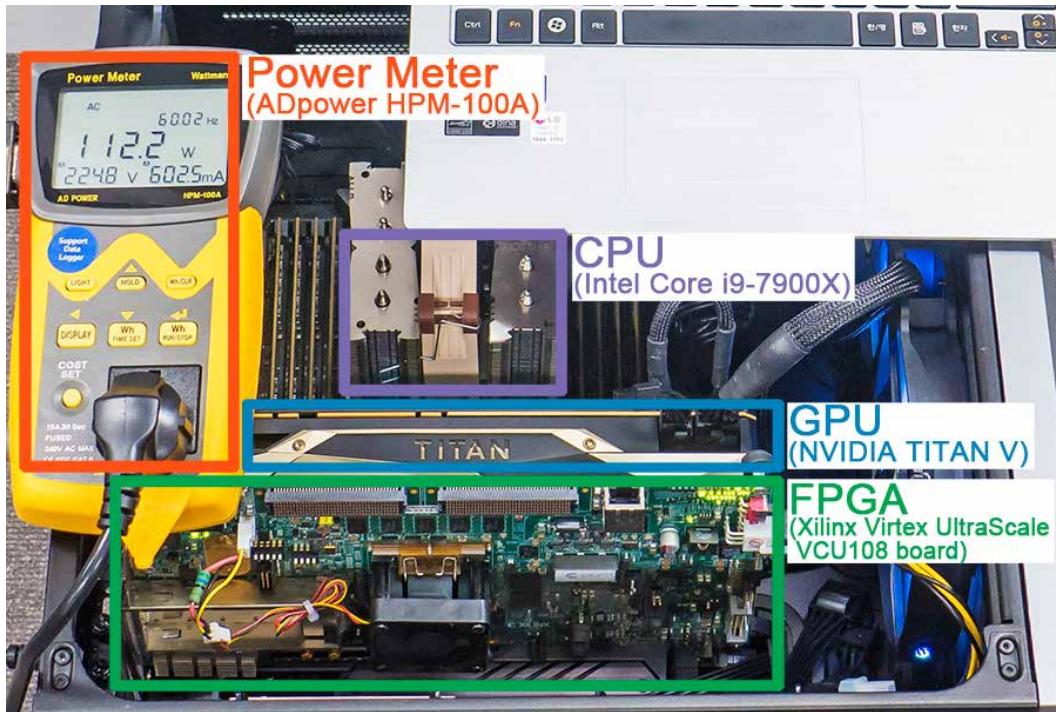


Figure 6: The for the actual power measurement of our hardware platform. It is combined with CPU, GPU and FPGA.

A.2 Power Measurement Results

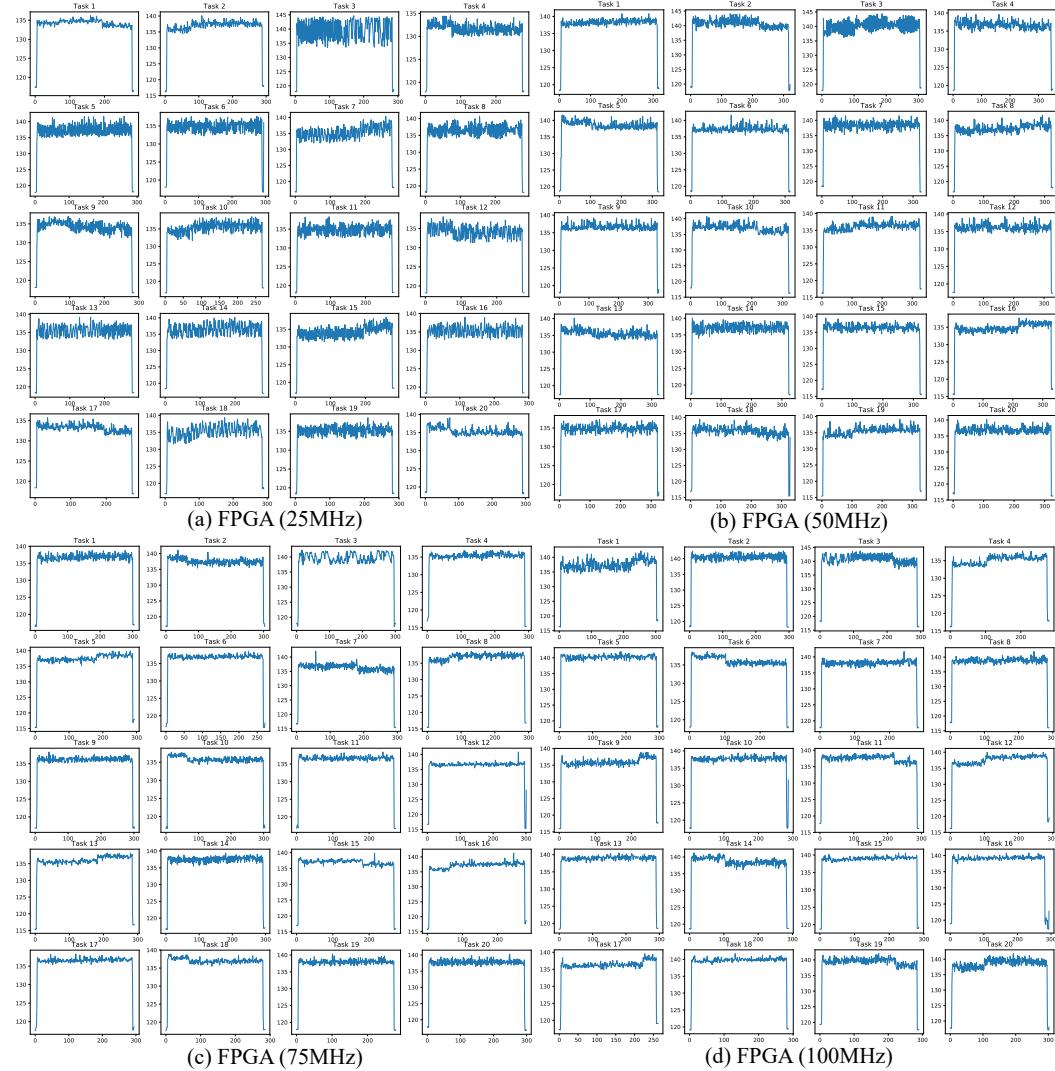


Figure 7: Power measurement results. x-axis: Elapsed time(sec), y-axis: Power (W)

Table 2: Time(sec.) measurement of the inference on the bAbI dataset(task 1-20)

task	CPU	GPU	FPGA(25MHz)	FPGA(50MHz)	FPGA(75MHz)	FPGA(100MHz)	FPGA+ITH(25MHz)	FPGA+ITH(50MHz)	FPGA+ITH(75MHz)	FPGA+ITH(100MHz)
1 1 supporting fact	163.956	218.901	32.639	23.682	24.228	20.371	22.939	19.979	20.512	20.519
2 2 supporting facts	369.456	239.218	57.291	47.077	44.939	41.690	48.575	43.368	41.195	40.481
3 3 supporting facts	1069.354	294.340	117.657	104.389	98.898	95.844	107.408	98.838	95.540	93.495
4 2 argument relations	65.782	212.280	28.076	20.256	17.695	16.435	20.332	16.694	15.323	14.292
5 3 argument relations	508.346	248.942	68.391	58.987	54.803	53.514	59.803	53.981	52.049	51.108
6 yes/no questions	170.864	220.816	37.034	28.521	26.023	24.434	28.378	24.573	23.289	22.262
7 counting	219.570	226.069	42.732	34.852	31.148	29.811	35.024	29.706	28.366	27.963
8 lists/sets	234.169	226.457	42.638	34.246	30.700	29.172	34.438	29.311	27.958	27.251
9 simple negation	164.828	220.267	36.395	27.923	25.318	23.812	27.235	23.674	22.440	21.227
10 indefinite knowledge	165.357	221.505	36.877	28.702	25.773	24.379	30.686	25.860	23.838	23.179
11 basic coreference	165.493	221.330	36.925	28.617	25.826	24.468	28.398	24.563	23.187	22.181
12 conjunction	166.376	221.481	37.326	29.614	26.611	25.180	26.645	23.905	22.697	22.859
13 compound coreference	166.476	221.434	38.173	30.098	26.986	25.463	31.419	26.781	24.566	24.309
14 time reasoning	211.148	226.333	42.868	35.059	31.093	29.693	35.924	30.994	28.727	28.413
15 basic deduction	212.261	221.837	38.137	29.978	26.829	25.518	28.950	25.288	24.371	23.199
16 basic induction	235.016	221.892	38.187	29.662	26.818	25.358	31.887	26.837	24.425	24.159
17 positional reasoning	67.093	213.839	29.870	21.626	19.103	17.930	22.815	18.259	16.819	16.421
18 size reasoning	169.530	221.994	38.883	30.847	27.429	26.120	32.371	27.309	25.434	24.636
19 path finding	141.622	219.667	35.592	27.600	24.404	23.220	29.468	24.495	22.399	21.862
20 agent's motivation	161.639	219.475	35.494	27.163	24.575	23.262	24.575	21.817	20.522	20.842
Average error (%)	242.767	226.904	43.544	34.954	31.960	30.284	35.364	30.813	29.183	28.533

Table 3: Power(W) measurement of the inference on the bAbI dataset(task 1-20)

task	CPU	GPU	FPGA(25MHz)		FPGA(50MHz)		FPGA(75MHz)		FPGA(100MHz)		FPGA+ITH(25MHz)		FPGA+ITH(50MHz)		FPGA+ITH(75MHz)		FPGA+ITH(100MHz)	
			FPGA(25MHz)	FPGA(50MHz)	FPGA(75MHz)	FPGA(100MHz)	FPGA(25MHz)	FPGA(50MHz)	FPGA(75MHz)	FPGA(100MHz)	FPGA(25MHz)	FPGA(50MHz)	FPGA(75MHz)	FPGA(100MHz)	FPGA(25MHz)	FPGA(50MHz)	FPGA(75MHz)	FPGA(100MHz)
1 1 supporting fact	23.239	45.289	14.661	16.971	17.942	19.435	16.328	21.314	19.925	19.661								
2 2 supporting facts	23.508	44.749	16.030	19.241	19.728	21.081	19.173	23.893	20.751	22.584								
3 3 supporting facts	23.896	45.430	18.363	20.939	22.663	22.922	21.614	23.269	22.908	23.392								
4 2 argument relations	22.978	46.983	13.168	16.016	17.574	19.541	13.793	19.834	18.593	19.408								
5 3 argument relations	23.073	46.671	16.167	19.346	20.996	20.681	19.294	21.634	20.753	22.808								
6 yes/no questions	22.915	43.458	14.413	17.617	18.884	20.122	16.914	20.437	20.146	19.273								
7 counting	23.274	45.584	15.195	18.231	19.001	20.919	17.302	21.479	19.724	21.442								
8 lists/sets	23.642	45.895	13.916	16.900	19.916	19.748	18.607	20.405	20.156	21.802								
9 simple negation	23.379	45.846	13.514	17.157	19.359	19.873	16.340	19.653	19.351	18.763								
10 indefinite knowledge	22.983	46.817	13.559	17.071	17.886	19.288	17.513	20.114	19.066	20.746								
11 basic coreference	23.104	46.116	14.308	17.000	18.884	19.988	16.920	19.156	19.807	20.040								
12 conjunction	22.890	43.740	14.124	17.631	19.469	20.067	16.261	19.292	19.820	20.261								
13 compound coreference	23.019	44.692	13.486	17.223	18.305	19.258	17.594	18.701	19.300	20.922								
14 time reasoning	23.151	44.681	15.978	18.307	19.683	21.239	18.470	20.213	20.757	20.122								
15 basic deduction	23.389	44.536	15.366	17.574	18.428	19.945	16.364	19.544	20.207	20.159								
16 basic induction	23.619	43.931	15.577	16.355	18.852	19.398	17.363	18.017	20.340	20.533								
17 positional reasoning	23.475	44.967	13.500	15.810	17.341	19.146	15.192	17.949	19.761	18.217								
18 size reasoning	22.935	44.178	14.492	17.247	17.993	19.590	17.363	18.863	20.259	20.746								
19 path finding	23.292	45.551	15.058	16.795	19.071	20.144	17.283	18.503	21.128	19.965								
20 agent's motivation	23.736	45.138	13.293	17.118	18.357	19.548	17.402	19.839	20.916	19.718								
Average error (%)	23.275	45.363	14.708	17.527	19.017	20.097	17.355	20.106	20.183	20.528								

Table 4: Power efficiency (FLOPS/W) of the inference on the bAbI dataset (task 1-20) for various configuration

task	CPU	GPU	FPGA(25MHz)	FPGA(50MHz)	FPGA(75MHz)	FPGA(100MHz)	FPGA+ITH(25MHz)	FPGA+ITH(50MHz)	FPGA+ITH(75MHz)	FPGA+ITH(100MHz)
1 1 supporting fact	2.602	1.000	20.718	24.481	22.806	25.040	26.469	23.281	24.257	24.574
2 2 supporting facts	1.149	1.000	11.656	11.818	12.074	12.180	11.494	10.331	12.522	11.708
3 3 supporting facts	0.523	1.000	6.189	6.118	5.966	6.087	5.760	5.814	6.110	6.114
4 2 argument relations	6.598	1.000	26.977	30.749	32.073	31.056	35.564	30.121	35.007	35.956
5 3 argument relations	0.991	1.000	10.508	10.181	10.097	10.498	10.069	9.949	10.756	9.967
6 yes/no questions	2.620	1.000	19.219	20.417	20.875	20.865	21.371	20.428	21.865	23.910
7 counting	2.016	1.000	15.871	16.218	17.411	16.525	17.005	16.151	18.419	17.187
8 lists/sets	1.877	1.000	17.517	17.958	16.988	18.041	16.219	17.377	18.444	17.493
9 simple negation	2.621	1.000	20.533	21.079	20.604	21.340	22.692	21.684	23.255	23.910
10 indefinite knowledge	2.729	1.000	20.740	21.165	22.496	22.054	19.297	19.936	22.816	21.566
11 basic coreference	2.669	1.000	19.319	20.980	20.928	20.870	21.242	21.692	22.224	22.962
12 conjunction	2.544	1.000	18.376	18.554	18.699	19.172	22.359	21.007	21.535	20.917
13 compound coreference	2.582	1.000	19.224	19.091	20.034	20.181	17.902	19.759	20.873	19.458
14 time reasoning	2.069	1.000	14.765	15.756	16.525	16.036	15.241	16.142	16.960	17.688
15 basic deduction	1.990	1.000	16.860	18.753	19.983	19.411	20.855	19.990	20.062	21.125
16 basic induction	1.756	1.000	16.388	20.093	19.281	19.817	17.606	20.160	19.621	19.651
17 positional reasoning	6.105	1.000	23.846	28.124	29.026	28.011	27.742	29.340	28.931	32.144
18 size reasoning	2.522	1.000	17.540	18.434	19.872	19.166	17.449	19.038	19.033	19.188
19 path finding	3.033	1.000	18.670	21.586	21.499	21.392	19.647	22.074	21.143	22.924
20 agent's motivation	2.582	1.000	20.996	21.305	21.959	21.786	23.165	22.888	23.079	24.106
Average error (%)	2.579	1.000	17.795	19.143	19.460	19.476	19.457	19.358	20.346	20.700

Table 5: Energy efficiency (FLOPS/kJ) of the inference on the bAbI dataset (task 1-20) for various configuration

task	CPU	GPU	FPGA(25MHz)	FPGA(50MHz)	FPGA(75MHz)	FPGA(100MHz)	FPGA(125MHz)	FPGA(150MHz)	FPGA+ITH(25MHz)	FPGA+ITH(50MHz)	FPGA+ITH(75MHz)	FPGA+ITH(100MHz)
1 1 supporting fact	3.474	1.000	138.950	224.577	206.055	269.075	252.586	255.076	258.867	255.076	258.867	262.159
2 2 supporting facts	0.693	1.000	48.670	60.054	64.274	69.890	56.604	56.986	72.717	69.195	69.195	69.195
3 3 supporting facts	0.144	1.000	15.483	17.249	17.756	18.692	15.785	17.315	18.823	18.823	19.247	19.247
4 2 argument relations	21.293	1.000	203.970	322.241	384.769	401.124	371.310	383.021	484.969	534.053	534.053	534.053
5 3 argument relations	0.485	1.000	38.247	42.967	45.866	48.836	41.914	45.880	51.444	48.547	48.547	48.547
6 yes/no questions	3.386	1.000	114.595	158.076	177.136	188.561	166.301	183.566	207.316	237.159	237.159	237.159
7 counting	2.076	1.000	83.961	105.200	126.370	125.315	109.765	122.911	146.791	138.952	138.952	138.952
8 lists/sets	1.816	1.000	93.035	118.750	125.388	140.052	106.655	134.257	149.392	145.369	145.369	145.369
9 simple negation	3.502	1.000	124.265	166.276	179.253	197.404	183.522	201.556	228.270	263.107	263.107	263.107
10 indefinite knowledge	3.655	1.000	124.577	163.337	193.343	200.379	139.295	170.766	212.011	206.086	206.086	206.086
11 basic coreference	3.570	1.000	115.800	162.267	179.358	188.782	165.555	195.463	212.140	229.124	229.124	229.124
12 conjunction	3.386	1.000	109.036	138.762	155.630	168.638	185.850	194.628	210.138	202.655	202.655	202.655
13 compound coreference	3.435	1.000	111.512	140.453	164.388	175.503	126.172	163.376	188.143	177.248	177.248	177.248
14 time reasoning	2.218	1.000	77.955	101.719	120.286	122.232	96.024	117.877	133.620	140.900	140.900	140.900
15 basic deduction	2.080	1.000	98.070	138.775	165.226	168.751	159.805	175.361	182.615	202.006	202.006	202.006
16 basic induction	1.658	1.000	95.223	150.312	159.528	173.409	122.517	166.686	178.252	180.489	180.489	180.489
17 positional reasoning	19.458	1.000	170.710	278.090	324.922	334.065	260.023	343.612	367.836	418.593	418.593	418.593
18 size reasoning	3.303	1.000	100.917	132.660	160.830	162.894	119.664	154.760	166.128	172.906	172.906	172.906
19 path finding	4.705	1.000	115.226	171.802	193.516	202.0377	146.456	197.978	207.350	230.340	230.340	230.340
20 agent's motivation	3.506	1.000	129.829	172.144	196.116	205.551	206.879	230.245	246.826	253.845	253.845	253.845
Average error (%)	4.392	1.000	105.502	148.286	167.001	178.076	151.634	175.566	196.182	206.599	206.599	206.599

B Histogram

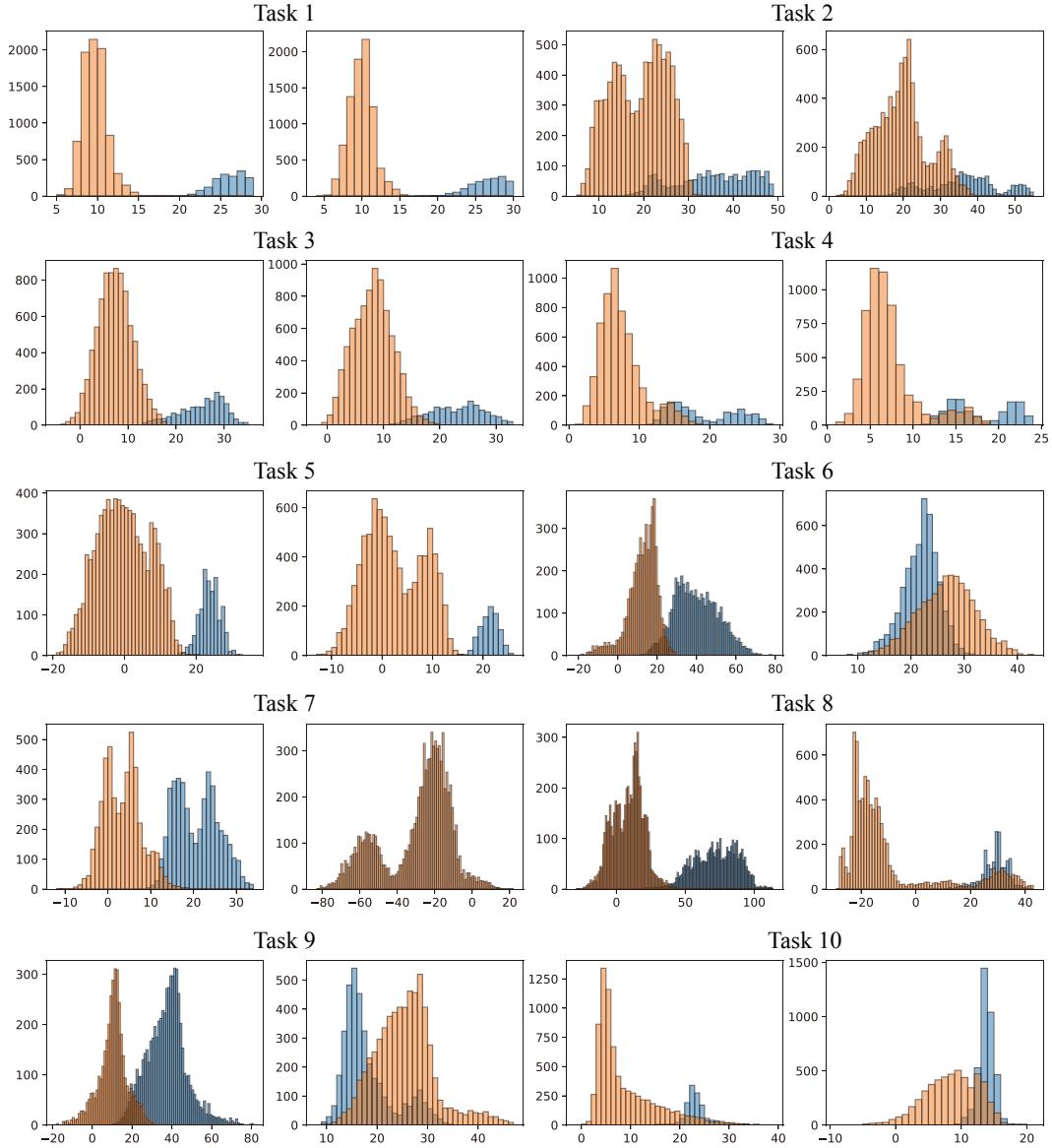


Figure 8: Example histograms of H_i for task 1–10

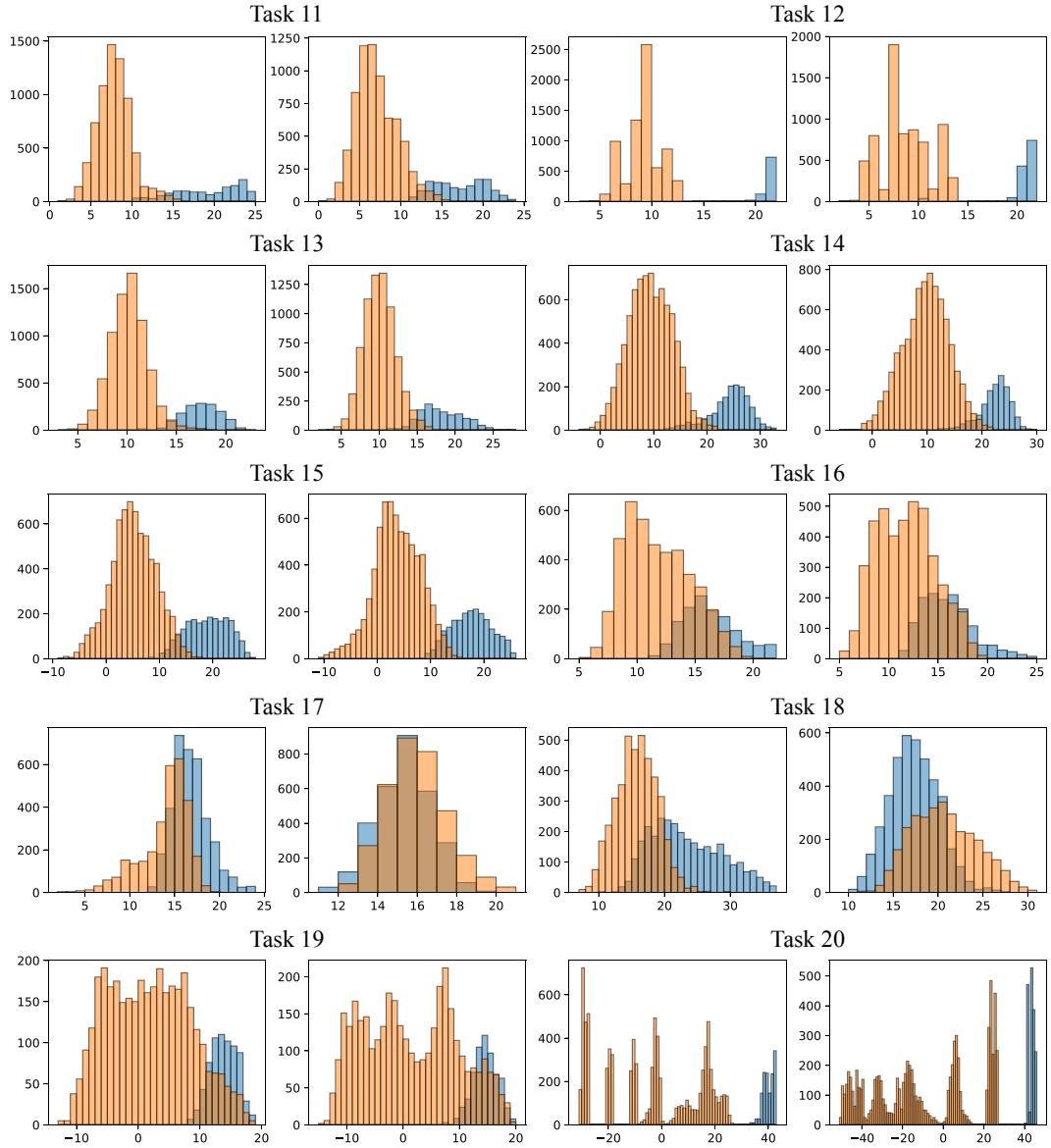


Figure 9: Example histograms of H_i for task 11–20

C MANN Model Description

Table 6: Model Descriptions

Symbol	Description	Domain
I	dimension of input	\mathbb{N}
E	dimension of embedding (internal representation)	\mathbb{N}
L	number of memory element	\mathbb{N}
R	number of read	\mathbb{N}
S	input vectors (sentences)	$\mathbb{R}^{L \times I}$
q	input vector (question)	\mathbb{R}^I
W_{emb_a}	weight of embedding input(address memory)	$\mathbb{R}^{E \times I}$
W_{emb_q}	weight of embedding input(q)	$\mathbb{R}^{E \times I}$
W_{emb_c}	weight of embedding input(content memory)	$\mathbb{R}^{E \times I}$
W_r	weight of read module	$\mathbb{R}^{E \times E}$
W_o	weight of output module	$\mathbb{R}^{I \times E}$
M_a	address memory	$\mathbb{R}^{E \times L}$
M_c	content memory	$\mathbb{R}^{E \times L}$
k_t	t th read key ($1 \leq t \leq R$)	\mathbb{R}^E
a_t	t th attention (read weight)	$\mathbb{R}^{E \times I}$
r_t	t th read vector	\mathbb{R}^E
o_t	t th output vector	\mathbb{R}^I

Memory addressing (content-based):

$$S(u, v) = u \cdot v$$

$$C(M, k)[i] = \frac{\exp\{S(M_i, k)\}}{\sum_j^L \exp\{S(M_j, k)\}}$$

Memory Write:

$$M_a = W_{emb_a} S^T$$

$$M_c = W_{emb_c} S^T$$

Memory Read:

$$k_t = \begin{cases} W_{emb_q} q & \text{if } t = 1 \\ h_{t-1} & \text{otherwise} \end{cases}$$

$$a_t = Address_Memory(k_t) = C(M_a, k_t)$$

$$r_t = Content_Memory(a_t) = M_r w_{r,t}$$

$$r_c_t = Read_Ctrl(k_t) = W_r k_t$$

$$h_t = r_t + r_c_t$$

Output:

$$o_t = softmax(W_o h_t)$$