

Driving Scientific Computations with Make

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<https://gitlab.msu.edu/piecuch-group>

Notation used in this presentation

Shell commands

Commands in the command line are prefixed with \$, e.g.

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$ mkdir my_foobar_dir  
$ vim my_foobar_file
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Placeholders

Placeholders for files or variables will be surrounded by [], e.g.

```
$ cat [A FILE] > [ANOTHER FILE]
```

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$ make [TARGET]
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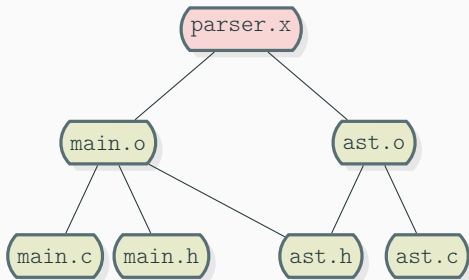


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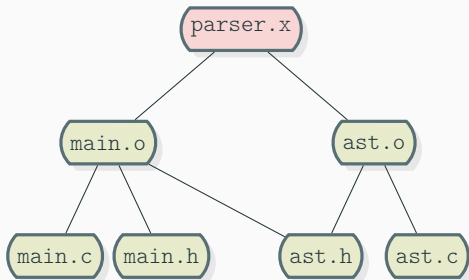


Figure 1: Example file dependency graph

In general, any set of files and rules works!

A Makefile Example

```
# Comments start with # as in bash
# Usually, one begins a file by setting some variables.
# For example:
COMPILER := gcc
LINKER := gcc

# The body of the Makefile consists of a set of rules
# which follow the following syntax:

# [TARGET] ... : [PREREQUISITES] ...
#     [RECIPE]

parser.x: main.o ast.o
    $(LINKER) main.o ast.o

main.o: main.h main.c ast.h
    $(COMPILER) -c main.c

ast.o: ast.h ast.c
    $(COMPILER) -c ast.o
```

Decomposing a Rule Entry

```
[TARGET]: [PREREQUISITES]
```

1

```
[RECIPE]
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- A [TARGET] usually the name of the file that is generated by the [RECIPE]. Can also be a phony target (will discuss later).

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Note

- `[RECIPE]` lines must be prefixed by a tab character
- Multiple `[RECIPE]` lines are allowed, but they are sent to different shells if not terminated by a backslash.

Make Execution

Once a `Makefile` is written, `make` can be executed in a shell, in the same directory as the `Makefile`

```
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One can select a particular `[TARGET]` to execute by passing it to `make`, as so

```
$ make [TARGET]
```

1

Make basic features

Make is loaded with a bunch of functions. For example, one can load paths from the file-system,

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and much more, including conditionals and loops

https://www.gnu.org/software/make/manual/html_node/Functions.html.

Make basic features

`Make` also generates a set of automatic variables that help in writing rules. For example, one can load the name of the target and prerequisites

```
requisites.txt: A couple of words
```

```
    echo $^ > $@
```

1

2

3

```
A couple of words:
```

4

```
$ cat requisites.txt
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where `$^` holds all prerequisites and `$@`, the target.

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where `$^` holds all prerequisites and `$@`, the target.

One can also write rules based on patterns, as so,

```
%.o: %.c
```

```
    gcc -c $< -o $@
```

which allows for writing generic recipes a file type. In this case `$<` holds the name of the first prerequisite.

PHONY targets

Sometimes it is useful to write rules which are not associated with a file. For example,

```
clean:
    rm *.o
```

1
2

Normally, this rule will try to find a file named `clean` in the working directory, and if it exists the rule would not be executed. To let `Make` know this is a dummy rule one can use the `.PHONY` declaration:

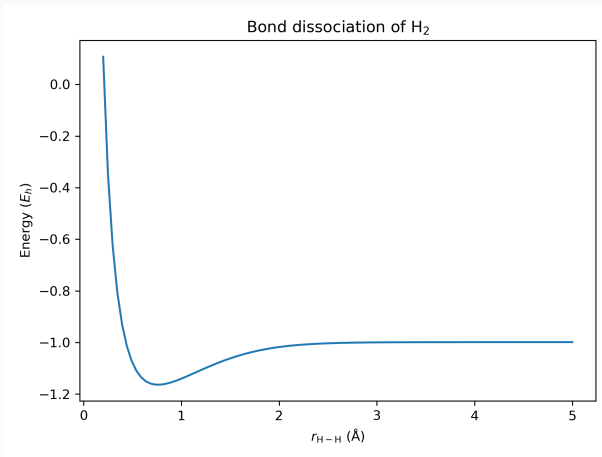
```
.PHONY: clean

clean:
    rm *.o
```

1
2
3
4

An example use in scientific: H₂ dissociation

Let's write a real world example `Makefile`: the potential energy surface of the dissociation of H₂ computed with `Psi4` at the CCSD/cc-pVDZ level.



An example use in scientific: H₂ dissociation

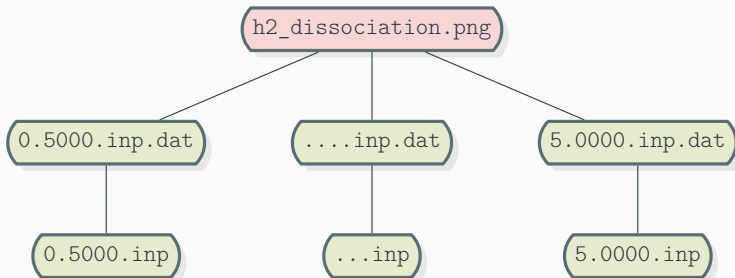
To do this, we will:

1. generate a set of input files from 0.2 Å to 5 Å
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1. `Make` is not so bad! It is just a bunch of dependency rules
2. It can help you drive computations efficiently, without rerunning stuff twice.
3. It is a tool that simplifies many different tasks, not only building software