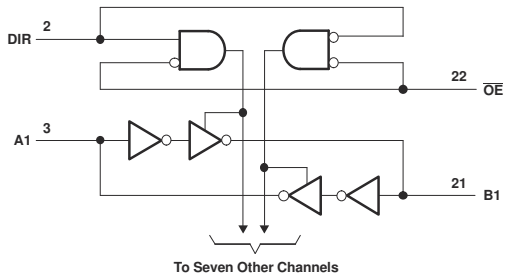
SN74LVC8T245 8-Bit Dual-Supply Bus Transceiver With Configurable Voltage Translation and 3-State Outputs

1 Features

- Control inputs V_{IH}/V_{IL} levels are referenced to V_{CCA} voltage
- V_{CC} isolation feature – if either V_{CC} input is at GND, all are in the high-impedance state
- Fully configurable dual-rail design allows each port to operate over the full 1.65-V to 5.5-V power-supply range
- Latch-up performance exceeds 100 mA per JESD 78, class II
- ESD protection exceeds JESD 22
  - 4000-V Human-Body Model (A114-A)
  - 100-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

2 Applications

- Personal electronic
- Industrial
- Enterprise
- Telecom



Logic Diagram (Positive Logic)

3 Description

The SN74LVC8T245 is an eight bit non-inverting bus transceiver with configurable dual power supply rails that enables bidirectional voltage level translation. The SN74LVC8T245 is optimized to operate with V_{CCA} and V_{CCB} set at 1.65 V to 5.5 V. The A port is designed to track V_{CCA}. V_{CCA} accepts any supply voltage from 1.65 V to 5.5 V. The B port is designed to track V_{CCB}. V_{CCB} accepts any supply voltage from 1.65 V to 5.5 V. This allows for universal low-voltage bidirectional translation between any of the 1.8-V, 2.5-V, 3.3-V, and 5.5-V voltage nodes.

The SN74LVC8T245 is designed for asynchronous communication between two data buses. The logic levels of the direction-control (DIR) input and the output-enable ($\overline{OE}$) input activate either the B-port outputs or the A-port outputs or place both output ports into the high-impedance mode. The device transmits data from the A bus to the B bus when the B-port outputs are activated, and from the B bus to the A bus when the A-port outputs are activated. The input circuitry on both A and B ports is always active and must have a logic HIGH or LOW level applied to prevent excess I_{CC} and I_{CCZ}.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The V_{CC} isolation feature ensures that if either V_{CC} input is at GND, all outputs are in the high-impedance state. To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVC8T245 is designed so that the control pins (DIR and $\overline{OE}$) are supplied by V_{CCA}.

Package Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
SN74LVC8T245	DBV (SSOP, 24)	8.20 mm × 5.30 mm
	DBQ (SSOP, 24)	8.65 mm × 3.90 mm
	PW (TSSOP, 24)	7.80 mm × 4.40 mm
	DGV (TVSOP, 24)	5.00 mm × 4.40 mm
	RHL (VQFN, 24)	5.50 mm × 3.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (November 2014) to Revision C (December 2022) **Page**

- Removed Machine Model specification....1
- Updated the numbering format for tables, figures, and cross-references throughout the document....1
- Updated the *ESD Ratings* section (was called *Handling Ratings*)....4
- Updated thermals in the Thermal Informations section....6
- Increased max switching characterisitics specs for VccB = 5V....8
- Updated the *Overview* section....12
- Added the *Balanced High-Drive CMOS Push-Pull Outputs* and V_{CC} *Isolation* sections....12
- Updated the *Power Supply Recommendations* section....15

Changes from Revision A (June 2005) to Revision B (November 2014) **Page**

- Added the list of Application, Pin Functions table, Handling Rating table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section....1
- Changed Feature From: 200-V Machine Model (A115-A) To: 100-V Machine Model (A115-A)....1

Changes from Revision * (June 2005) to Revision A (August 2005) **Page**

- Changed the device From: Product Preview To: Production....1

5 Pin Configuration and Functions

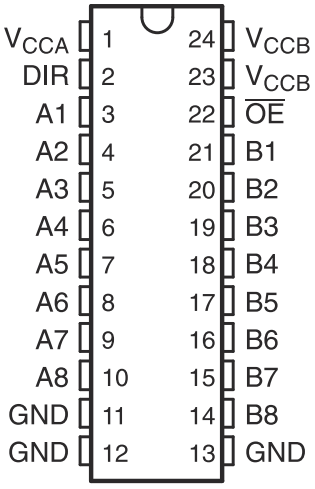


Figure 5-1. DW, NS, DB, DBQ, DGV, or PW Package, 24-Pin SOIC, SO, SSOP, SSOP, TVSOP, or TSSOP (Top View)

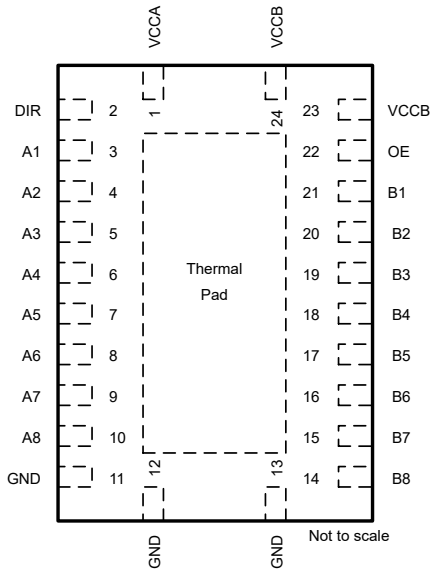


Figure 5-2. RHL Package, 24-Pin VQFN (Top View)

Table 5-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
A1	3	I/O	Input/output A1. Referenced to V_{CCA}.
A2	4	I/O	Input/output A2. Referenced to V_{CCA}.
A3	5	I/O	Input/output A3. Referenced to V_{CCA}.
A4	6	I/O	Input/output A4. Referenced to V_{CCA}.
A5	7	I/O	Input/output A5. Referenced to V_{CCA}.
A6	8	I/O	Input/output A6. Referenced to V_{CCA}.
A7	9	I/O	Input/output A7. Referenced to V_{CCA}.
A8	10	I/O	Input/output A8. Referenced to V_{CCA}.
B1	21	I/O	Input/output B1. Referenced to V_{CCB}.
B2	20	I/O	Input/output B2. Referenced to V_{CCB}.
B3	19	I/O	Input/output B3. Referenced to V_{CCB}.
B4	18	I/O	Input/output B4. Referenced to V_{CCB}.
B5	17	I/O	Input/output B5. Referenced to V_{CCB}.
B6	16	I/O	Input/output B6. Referenced to V_{CCB}.
B7	15	I/O	Input/output B7. Referenced to V_{CCB}.
B8	14	I/O	Input/output B8. Referenced to V_{CCB}.
DIR	2	I	Direction-control signal.
GND	11, 12, 13	G	Ground
$\overline{OE}$	22	I	3-state output-mode enables. Pull $\overline{OE}$ high to place all outputs in 3-state mode. Referenced to V_{CCA}.
V_{CCA}	1	P	A-port supply voltage. 1.65 V ≤ V_{CCA} ≤ 5.5 V
V_{CCB}	23, 24	P	B-port supply voltage. 1.65 V ≤ V_{CCB} ≤ 5.5 V
Thermal Pad[2]		—	

(1) I = input, O = output, P = power
(2) For the RHL package only

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

(1)			MIN	MAX	UNIT
	Supply voltage range, V_{CCA}, V_{CCB}		–0.5	6.5	V
V_I	Input voltage range(2)	I/O ports (A port)	–0.5	6.5	V
		I/O ports (B port)	–0.5	6.5	
		Control inputs	–0.5	6.5	
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)	A port	–0.5	6.5	V
		B port	–0.5	6.5	
V_O	Voltage range applied to any output in the high or low state(2) (3)	A port	–0.5	V_{CCA} + 0.5	V
		B port	–0.5	V_{CCB} + 0.5	
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through each V_{CCA}, V_{CCB}, and GND			±100	mA
T_{stg}	Storage temperature		-65	150	°C
T_J	Junction temperature			150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The output positive-voltage rating may be exceeded up to 6.5 V maximum if the output current rating is observed.

6.2 ESD Ratings

			MIN	MAX	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	–4000	4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	–1000	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

(1) (2) (3) (4)			V_{CCI}	V_{CCO}	MIN	MAX	UNIT
V_{CCA}	Supply voltage				1.65	5.5	V
V_{CCB}					1.65	5.5	
V_{IH}	High-level input voltage	Data inputs(5)	1.65 V to 1.95 V		V_{CCI} × 0.65		V
			2.3 V to 2.7 V		1.7		
			3 V to 3.6 V		2		
			4.5 V to 5.5 V		V_{CCI} × 0.7		
V_{IL}	Low-level input voltage	Data inputs(5)	1.65 V to 1.95 V			V_{CCI} × 0.35	V
			2.3 V to 2.7 V			0.7	
			3 V to 3.6 V			0.8	
			4.5 V to 5.5 V			V_{CCI} × 0.3	
V_{IH}	High-level input voltage	Control inputs (referenced to V_{CCA})(6)	1.65 V to 1.95 V		V_{CCA} × 0.65		V
			2.3 V to 2.7 V		1.7		
			3 V to 3.6 V		2		
			4.5 V to 5.5 V		V_{CCA} × 0.7		
V_{IL}	Low-level input voltage	Control inputs (referenced to V_{CCA})(6)	1.65 V to 1.95 V			V_{CCA} × 0.35	V
			2.3 V to 2.7 V			0.7	
			3 V to 3.6 V			0.8	
			4.5 V to 5.5 V			V_{CCA} × 0.3	
V_I	Input voltage	Control inputs			0	5.5	V
$V_{I/O}$	Input/output voltage	Active state			0	V_{CCO}	V
		3-State			0	5.5	V
I_{OH}	High-level output current			1.65 V to 1.95 V		–4	mA
				2.3 V to 2.7 V		–8	
				3 V to 3.6 V		–24	
				4.5 V to 5.5 V		–32	
I_{OL}	Low-level output current			1.65 V to 1.95 V		4	mA
				2.3 V to 2.7 V		8	
				3 V to 3.6 V		24	
				4.5 V to 5.5 V		32	
$\Delta t/\Delta v$(7)	Input transition rise or fall rate	Data inputs	1.65 V to 1.95 V			20	ns/V
			2.3 V to 2.7 V			20	
			3 V to 3.6 V			10	
			4.5 V to 5.5 V			5	
T_A	Operating free-air temperature				–40	85	°C

(1) V_{CCI} is the V_{CC} associated with the data input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) All unused or driven (floating) data inputs (I/Os) of the device must be held at logic HIGH or LOW (preferably V_{CCI} or GND) to ensure proper device operation and minimize power. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs,* literature number SCBA004.
(4) All unused control inputs must be held at V_{CCA} or GND to ensure proper device operation and minimize power comsumption.
(5) For V_{CCI} values not specified in the data sheet, V_{IH} min = V_{CCI} × 0.7 V, V_{IL} max = V_{CCI} × 0.3 V.
(6) For V_{CCA} values not specified in the data sheet, V_{IH} min = V_{CCA} × 0.7 V, V_{IL} max = V_{CCA} × 0.3 V.
(7) Maximum input transition rate with < 4 channels switching simultaneously.

6.4 Thermal Information DB, DBQ and DGV

THERMAL METRIC[1]		DB	DBQ	DGV	UNIT
		24 PINS	24 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	90.7	81.2	91.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.9	44.8	23.7	
$R_{\theta JB}$	Junction-to-board thermal resistance	49.7	34.5	44.5	
ψ_{JT}	Junction-to-top characterization parameter	18.8	9.5	0.6	
ψ_{JB}	Junction-to-board characterization parameter	49.3	37.2	44.1	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Thermal Information PW and RHL

THERMAL METRIC[1]		PW	RHL	UNIT
		24 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	100.6	48.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	44.7	46.1	
$R_{\theta JB}$	Junction-to-board thermal resistance	55.8	26.1	
ψ_{JT}	Junction-to-top characterization parameter	6.8	4.6	
ψ_{JB}	Junction-to-board characterization parameter	55.4	26.0	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	15.7	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.6 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER(1) (2)		TEST CONDITIONS	V_{CCA}	V_{CCB}	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
V_{OH}		I_{OH} = –100 µA, V_I = V_{IH}	1.65 V to 4.5 V	1.65 V to 4.5 V				V_{CCO} – 0.1			V
		I_{OH} = –4 mA, V_I = V_{IH}	1.65 V	1.65 V				1.2			
		I_{OH} = –8 mA, V_I = V_{IH}	2.3 V	2.3 V				1.9			
		I_{OH} = –24 mA, V_I = V_{IH}	3 V	3 V				2.4			
		I_{OH} = –32 mA, V_I = V_{IH}	4.5 V	4.5 V				3.8			
V_{OL}		I_{OL} = 100 µA, V_I = V_{IL}	1.65 V to 4.5 V	1.65 V to 4.5 V						0.1	V
		I_{OL} = 4 mA, V_I = V_{IL}	1.65 V	1.65 V						0.45	
		I_{OL} = 8 mA, V_I = V_{IL}	2.3 V	2.3 V						0.3	
		I_{OL} = 24 mA, V_I = V_{IL}	3 V	3 V						0.55	
		I_{OL} = 32 mA, V_I = V_{IL}	4.5 V	4.5 V						0.55	
I_I	DIR	V_I = V_{CCA} or GND	1.65 V to 5.5 V	1.65 V to 5.5 V			±1			±2	µA
I_{off}	A or B port	V_I or V_O = 0 to 5.5 V	0 V	0 to 5.5 V			±1			±2	µA
			0 to 5.5 V	0 V			±1			±2	
I_{OZ}	A or B port	V_O = V_{CCO} or GND, $\overline{OE}$ = V_{IH}	1.65 V to 5.5 V	1.65 V to 5.5 V			±1			±2	µA
I_{CCA}		V_I = V_{CCI} or GND, I_O = 0	1.65 V to 5.5 V	1.65 V to 5.5 V						15	µA
			5 V	0 V						15	
			0 V	5 V						–2	
I_{CCB}		V_I = V_{CCI} or GND, I_O = 0	1.65 V to 5.5 V	1.65 V to 5.5 V						15	µA
			5 V	0 V						–2	
			0 V	5 V						15	
I_{CCA} + I_{CCB}		V_I = V_{CCI} or GND, I_O = 0	1.65 V to 5.5 V	1.65 V to 5.5 V						25	µA
ΔI_{CCA}	A port	One A port at V_{CCA} – 0.6 V, DIR at V_{CCA}, B port = open	3 V to 5.5 V	3 V to 5.5 V						50	µA
	DIR	DIR at V_{CCA} – 0.6 V, B port = open, A port at V_{CCA} or GND								50	
ΔI_{CCB}	B port	One B port at V_{CCB} – 0.6 V, DIR at GND, A port = open	3 V to 5.5 V	3 V to 5.5 V						50	µA
C_i	Control inputs	V_I = V_{CCA} or GND	3.3 V	3.3 V		4				5	pF
C_{io}	A or B port	V_O = $V_{CCA/B}$ or GND	3.3 V	3.3 V		8.5				10	pF

(1) V_{CCO} is the V_{CC} associated with the output port.
(2) V_{CCI} is the V_{CC} associated with the input port.

6.7 Switching Characteristics, V_{CCA} = 1.8 V ± 0.15 V

over recommended operating free-air temperature range, V_{CCA} = 1.8 V ± 0.15 V (unless otherwise noted) (see Figure 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	1.7	21.9	1.3	9.2	1	7.4	0.8	7.1	ns
t_{PHL}											
t_{PLH}	B	A	0.9	23.8	0.8	23.6	0.7	23.4	0.7	23.4	ns
t_{PHL}											
t_{PHZ}	$\overline{OE}$	A	1.5	29.6	1.5	29.4	1.5	29.3	1.4	29.2	ns
t_{PLZ}											
t_{PHZ}	$\overline{OE}$	B	2.4	32.2	1.9	13.1	1.7	12	1.3	10.3	ns
t_{PLZ}											
t_{PZH}	$\overline{OE}$	A	0.4	24	0.4	23.8	0.4	23.7	0.4	23.7	ns
t_{PZL}											
t_{PZH}	$\overline{OE}$	B	1.8	32	1.5	16	1.2	12.6	0.9	12	ns
t_{PZL}											

6.8 Switching Characteristics, V_{CCA} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range, V_{CCA} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	1.5	21.4	1.2	9	0.8	6.2	0.6	4.8	ns
t_{PHL}											
t_{PLH}	B	A	1.2	9.3	1	9.1	1	8.9	0.9	8.8	ns
t_{PHL}											
t_{PHZ}	$\overline{OE}$	A	1.4	9	1.4	9	1.4	9	1.4	9	ns
t_{PLZ}											
t_{PHZ}	$\overline{OE}$	B	2.3	29.6	1.8	11	1.7	9.3	0.9	6.9	ns
t_{PLZ}											
t_{PZH}	$\overline{OE}$	A	1	10.9	1	10.9	1	10.9	1	10.9	ns
t_{PZL}											
t_{PZH}	$\overline{OE}$	B	1.7	28.2	1.5	12.9	1.2	9.4	1	7.5	ns
t_{PZL}											

6.9 Switching Characteristics, V_{CCA} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V_{CCA} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	1.5	21.2	1.1	8.8	0.8	6.3	0.5	4.4	ns
t_{PHL}											
t_{PLH}	B	A	0.8	7.2	0.8	6.2	0.7	6.1	0.6	6	ns
t_{PHL}											
t_{PHZ}	$\overline{OE}$	A	1.6	8.2	1.6	8.2	1.6	8.2	1.6	8.2	ns
t_{PLZ}											
t_{PHZ}	$\overline{OE}$	B	2.1	29	1.7	10.3	1.5	8.6	0.8	6.3	ns
t_{PLZ}											
t_{PZH}	$\overline{OE}$	A	0.8	8.1	0.8	8.1	0.8	8.1	0.8	8.1	ns
t_{PZL}											
t_{PZH}	$\overline{OE}$	B	1.8	27.7	1.4	12.4	1.1	8.8	0.9	6.8	ns
t_{PZL}											

6.10 Switching Characteristics, V_{CCA} = 5 V ± 0.5 V

over recommended operating free-air temperature range, V_{CCA} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	1.5	21.4	1	8.8	0.7	6	0.4	4.2	ns
t_{PHL}											
t_{PLH}	B	A	0.7	7	0.4	4.8	0.3	4.5	0.3	4.3	ns
t_{PHL}											
t_{PHZ}	$\overline{OE}$	A	0.3	5.4	0.3	5.4	0.3	5.4	0.3	5.4	ns
t_{PLZ}											
t_{PHZ}	$\overline{OE}$	B	2	28.7	1.6	9.7	1.4	8	0.7	5.7	ns
t_{PLZ}											
t_{PZH}	$\overline{OE}$	A	0.7	6.4	0.7	6.4	0.7	6.4	0.7	6.4	ns
t_{PZL}											
t_{PZH}	$\overline{OE}$	B	1.5	27.6	1.3	11.4	1	8.8	0.9	6.6	ns
t_{PZL}											

6.11 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CCA} = V_{CCB} = 1.8 V	V_{CCA} = V_{CCB} = 2.5 V	V_{CCA} = V_{CCB} = 3.3 V	V_{CCA} = V_{CCB} = 5 V	UNIT
			TYP	TYP	TYP	TYP	
C_{pdA} (1)	A-port input, B-port output	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns	2	2	2	3	pF
	B-port input, A-port output		12	13	13	16	
C_{pdB} (1)	A-port input, B-port output		13	13	14	16	
	B-port input, A-port output		2	2	2	3	

(1) Power dissipation capacitance per transceiver

6.12 Typical Characteristics

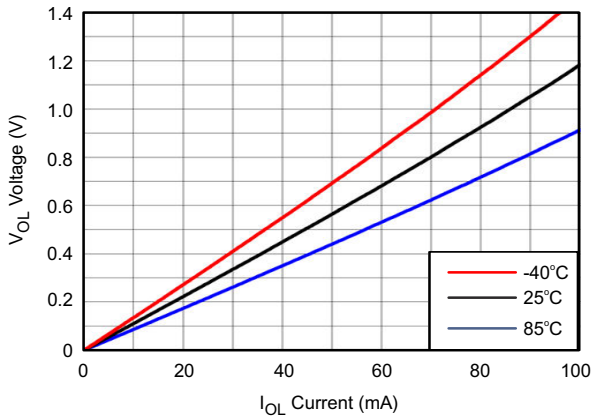


Figure 6-1. Voltage vs Current

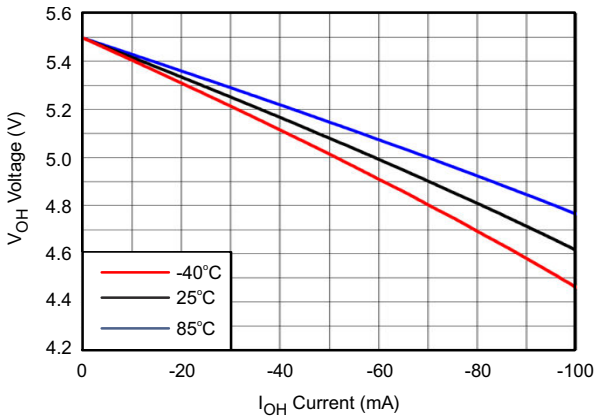
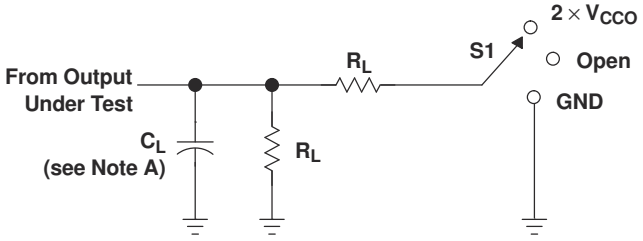


Figure 6-2. Voltage vs Current

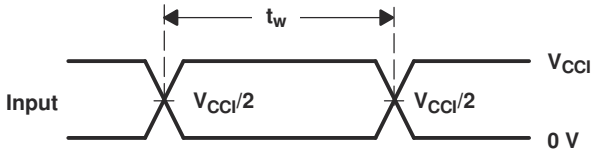
7 Parameter Measurement Information



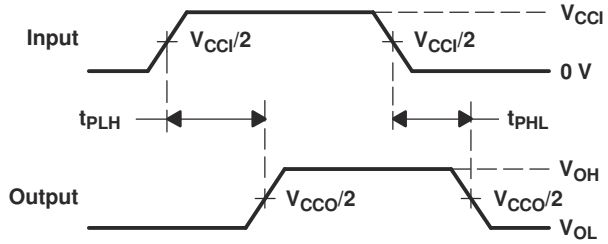
LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CCO}$
t_{PHZ}/t_{PZH}	GND

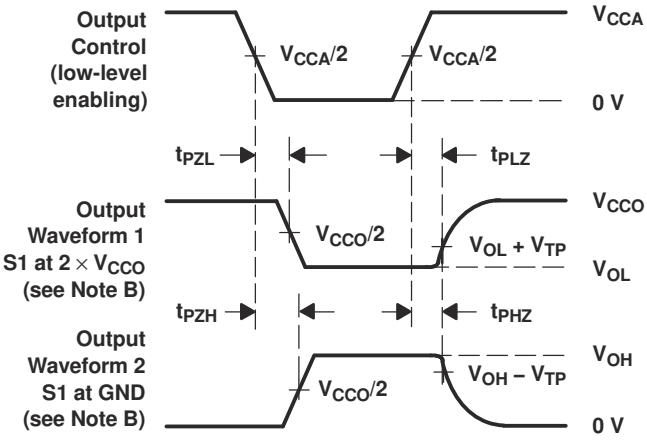
V_{CCO}	C_L	R_L	V_{TP}
1.8 V ± 0.15 V	15 pF	2 kΩ	0.15 V
2.5 V ± 0.2 V	15 pF	2 kΩ	0.15 V
3.3 V ± 0.3 V	15 pF	2 kΩ	0.3 V
5 V ± 0.5 V	15 pF	2 kΩ	0.3 V



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, dv/dt ≥ 1 V/ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. V_{CCI} is the V_{CC} associated with the input port.
I. V_{CCO} is the V_{CC} associated with the output port.
J. All parameters and waveforms are not applicable to all devices.

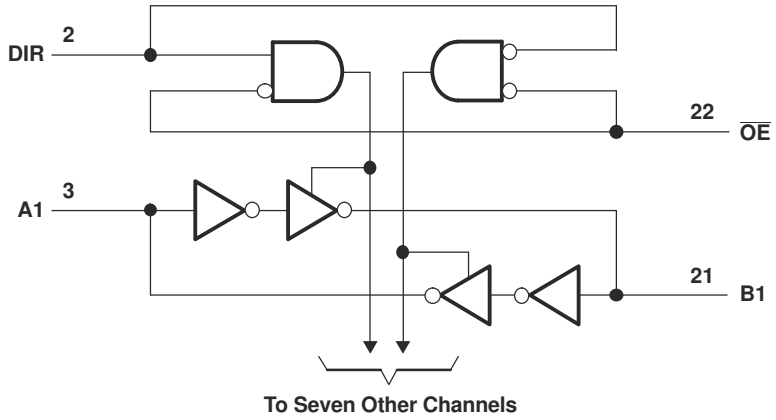
Figure 7-1. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN74LVC8T245 is an eight bit non-inverting bus transceiver with configurable dual power supply rails that enables bidirectional voltage level translation. Pin Ax and direction control pin are support by V_{CCA} and pin Bx is support by V_{CCB}. The A port is able to accept I/O voltages ranging from 1.65 V to 5.5 V, while the B port can accept I/O voltages from 1.65 V to 5.5 V. The high on DIR allows data transmission from A to B and a low on DIR allows data transmission from B to A. For voltage level translation below 1.65 V, see TI AXC products.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.65-V to 5.5-V Power-Supply Range

Both V_{CCA} and V_{CCB} can be supplied at any voltage between 1.65 V and 5.5 V making the device suitable for translating between any of the voltage nodes (1.8 V, 2.5 V, 3.3 V, and 5 V).

8.3.2 I_{off} Supports Partial-Power-Down Mode Operation

I_{off} prevents backflow current by disabling I/O output circuits when device is in partial-power-down mode.The inputs and outputs for this device enter a high-impedance state when the device is powered down, inhibiting current backflow into the device. The maximum leakage into or out of any input or output pin on the device is specified by I_{off} in the Electrical Characteristics.

8.3.3 Balanced High-Drive CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The high drive capability of this device creates fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. Two outputs can be connected together for 2X stronger output drive strength. The electrical and thermal limits defined in the Absolute Maximum Ratings must be followed at all times.

8.3.4 V_{cc} Isolation

The I/O's of both ports will enter a high-impedance state when either of the supplies are at GND, while the other supply is still connected to the device. The maximum leakage into or out of any input or output pin on the device is specified by I_{off} in the *Electrical Characteristics*.

8.4 Device Functional Modes

The SN74LVC8T245 is voltage level translator that can operate from 1.65 V to 5.5 V (V_{CCA} and V_{CCB}). The signal translation between 1.65 V and 5.5 V requires direction control and output enable control. When $\overline{OE}$ is low and DIR is high, data transmission is from A to B. When $\overline{OE}$ is low and DIR is low, data transmission is from B to A. When $\overline{OE}$ is high, both output ports will be high-impedance. For voltage level translation below 1.65V, see TI AXC products.

Table 8-1. Function Table
(Each 8-Bit Section)

CONTROL INPUTS(1)		OUTPUT CIRCUITS		OPERATION
$\overline{OE}$	DIR	A PORT	B PORT	
L	L	Enabled	Hi-Z	B data to A bus
L	H	Hi-Z	Enabled	A data to B bus
H	X	Hi-Z	Hi-Z	Isolation

(1) Input circuits of the data I/Os are always active.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The SN74LVC8T245 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The maximum output current can be up to 32 mA when device is powered by 5 V. It is recommended to tie all unused I/Os to GND. The device should not have any floating I/Os when changing translation direction.

9.2 Typical Application

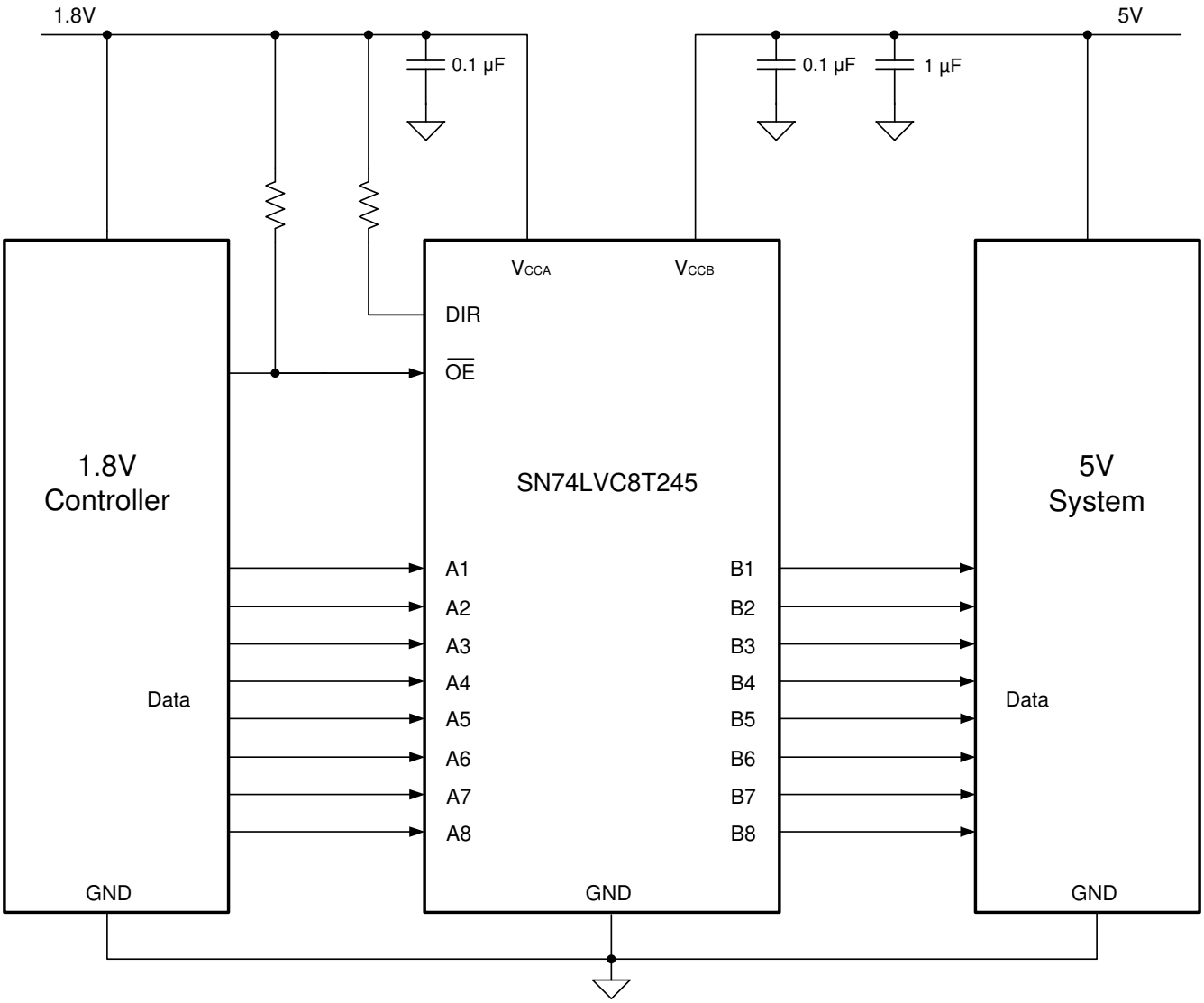


Figure 9-1. Typical Application Circuit

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 9-1.

Table 9-1. Design Parameters

PARAMETERS	VALUES
Input voltage range	1.65 V to 5.5 V
Output voltage	1.65 V to 5.5 V

9.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the SN74LVC8T245 device to determine the input voltage range. For a valid logic high, the value must exceed the V_{IH} of the input port. For a valid logic low, the value must be less than the V_{IL} of the input port.
- Output voltage range
  - Use the supply voltage of the device that the SN74LVC8T245 device is driving to determine the output voltage range.

9.2.3 Application Curve

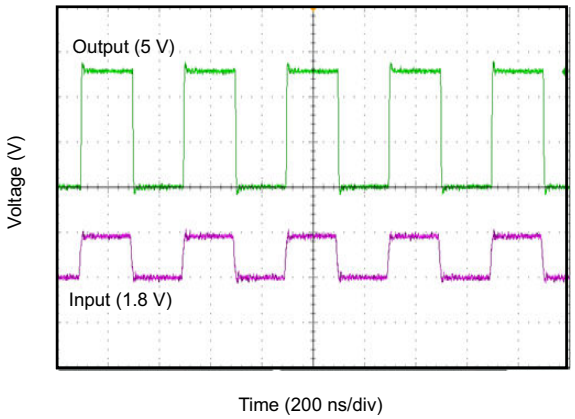


Figure 9-2. Translation Up (1.8 V to 5 V) at 2.5 MHz

10 Power Supply Recommendations

The SN74LVC8T245 device uses two separate configurable power-supply rails, V_{CCA} and V_{CCB}. V_{CCA} accepts any supply voltage from 1.65 V to 5.5 V and V_{CCB} accepts any supply voltage from 1.65 V to 5.5 V. The A port and B port are designed to track V_{CCA} and V_{CCB} respectively allowing for low-voltage bidirectional translation between any of the 1.8-V, 2.5 -V, 3.3-V and 5-V voltage nodes. The recommendation is to first power-up the input supply rail to help avoid internal floating while the output supply rail ramps up. However, both power-supply rails can be ramped up simultaneously.

11 Layout

11.1 Layout Guidelines

To ensure reliability of the device, following common printed-circuit board layout guidelines is recommended.

- Bypass capacitors should be used on power supplies.
- Short trace lengths should be used to avoid excessive loading.
- Placing pads on the signal paths for loading capacitors or pullup resistors helps adjust rise and fall times of signals depending on the system requirements.

11.2 Layout Example

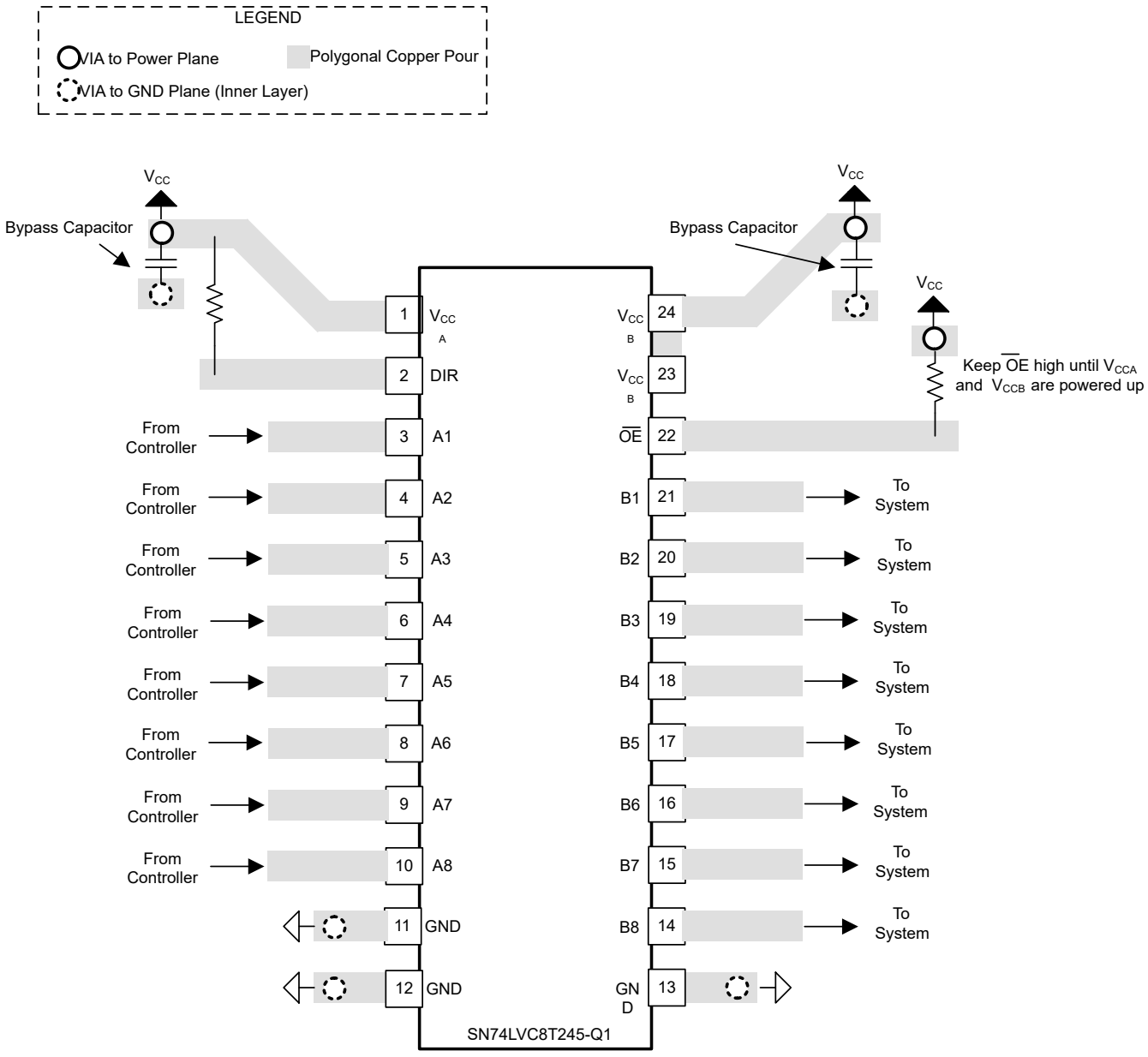


Figure 11-1. SN74LVC8T245 Layout

12 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
74LVC8T245DBQRG4	Active	Production	SSOP (DBQ) | 24	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVC8T245
74LVC8T245RHLRG4	Active	Production	VQFN (RHL) | 24	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	NH245
SN74LVC8T245DBQR	Active	Production	SSOP (DBQ) | 24	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVC8T245
SN74LVC8T245DBQR.B	Active	Production	SSOP (DBQ) | 24	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVC8T245
SN74LVC8T245DBR	Active	Production	SSOP (DB) | 24	2000 | LARGE T&R	Yes	NIPDAU | NIPDAU	Level-1-260C-UNLIM	-40 to 85	NH245
SN74LVC8T245DBR.A	Active	Production	SSOP (DB) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NH245
SN74LVC8T245DBRG4	Active	Production	SSOP (DB) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NH245
SN74LVC8T245DGVR	Active	Production	TVSOP (DGV) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NH245
SN74LVC8T245DGVR.B	Active	Production	TVSOP (DGV) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NH245
SN74LVC8T245DGVRG4	Active	Production	TVSOP (DGV) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NH245
SN74LVC8T245DWR	Active	Production	SOIC (DW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC8T245
SN74LVC8T245DWR.B	Active	Production	SOIC (DW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC8T245
SN74LVC8T245DWRG4	Active	Production	SOIC (DW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC8T245
SN74LVC8T245NSR	Active	Production	SOP (NS) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC8T245
SN74LVC8T245NSR.B	Active	Production	SOP (NS) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC8T245
SN74LVC8T245PW	Active	Production	TSSOP (PW) | 24	60 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NH245
SN74LVC8T245PW.A	Active	Production	TSSOP (PW) | 24	60 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NH245
SN74LVC8T245PW.B	Active	Production	TSSOP (PW) | 24	60 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NH245
SN74LVC8T245PWG4	Active	Production	TSSOP (PW) | 24	60 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NH245
SN74LVC8T245PWR	Active	Production	TSSOP (PW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NH245
SN74LVC8T245PWR.A	Active	Production	TSSOP (PW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NH245
SN74LVC8T245PWRE4	Active	Production	TSSOP (PW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NH245
SN74LVC8T245PWRG4	Active	Production	TSSOP (PW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NH245
SN74LVC8T245RHLR	Active	Production	VQFN (RHL) | 24	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	NH245
SN74LVC8T245RHLR.A	Active	Production	VQFN (RHL) | 24	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	NH245
SN74LVC8T245RHLR.B	Active	Production	VQFN (RHL) | 24	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	NH245

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF SN74LVC8T245 :

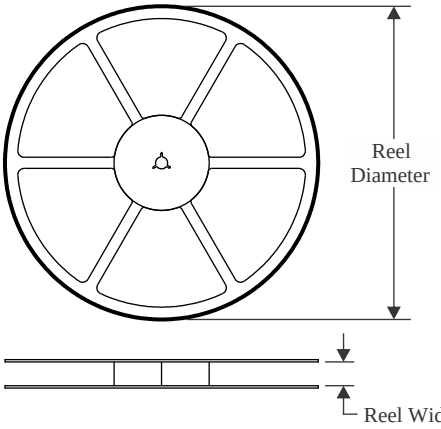
- Automotive : SN74LVC8T245-Q1
- Enhanced Product : SN74LVC8T245-EP

NOTE: Qualified Version Definitions:

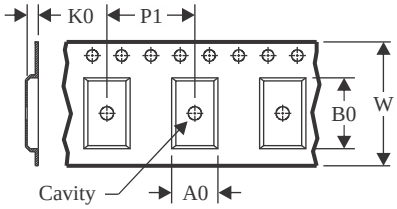
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

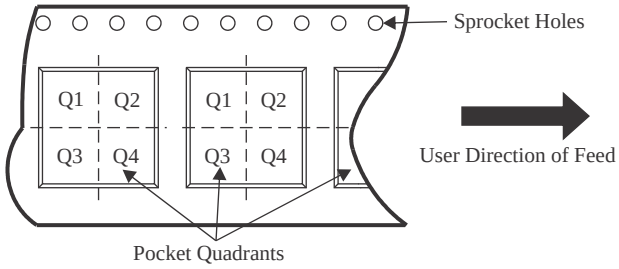


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

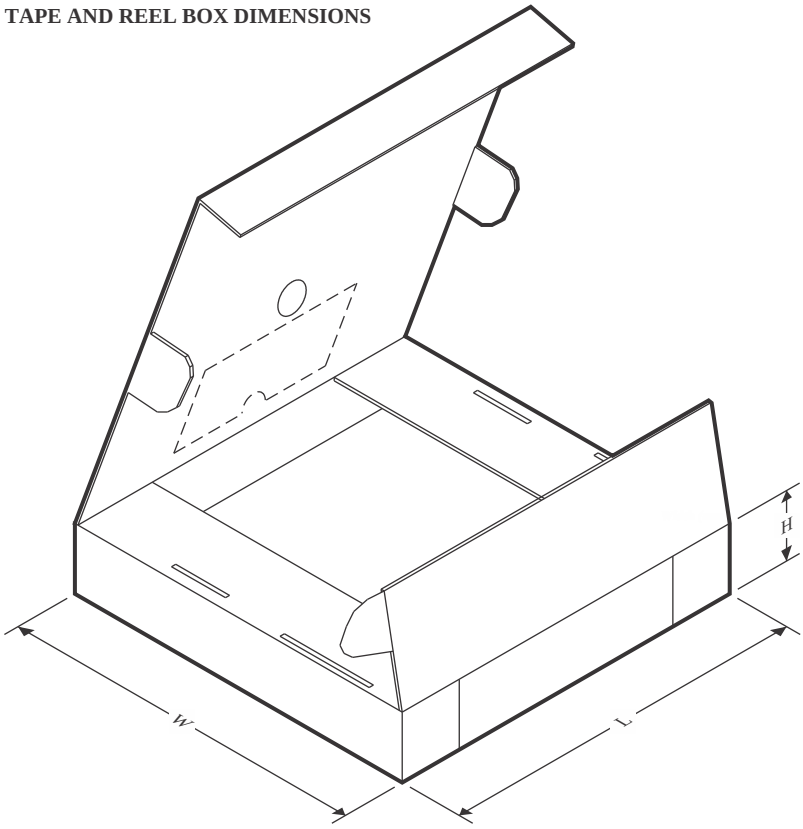
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC8T245DBQR	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC8T245DBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
SN74LVC8T245DBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
SN74LVC8T245DGVR	TVSOP	DGV	24	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC8T245DWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74LVC8T245RHLR	VQFN	RHL	24	1000	180.0	12.4	3.8	5.8	1.2	8.0	12.0	Q1

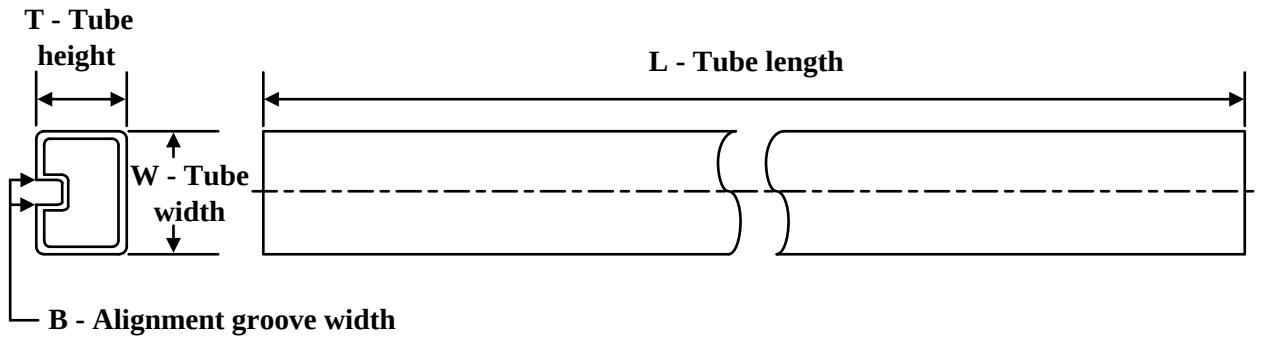
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC8T245DBQR	SSOP	DBQ	24	2500	353.0	353.0	32.0
SN74LVC8T245DBR	SSOP	DB	24	2000	353.0	353.0	32.0
SN74LVC8T245DBR	SSOP	DB	24	2000	353.0	353.0	32.0
SN74LVC8T245DGVR	TVSOP	DGV	24	2000	353.0	353.0	32.0
SN74LVC8T245DWR	SOIC	DW	24	2000	350.0	350.0	43.0
SN74LVC8T245RHLR	VQFN	RHL	24	1000	213.0	191.0	35.0

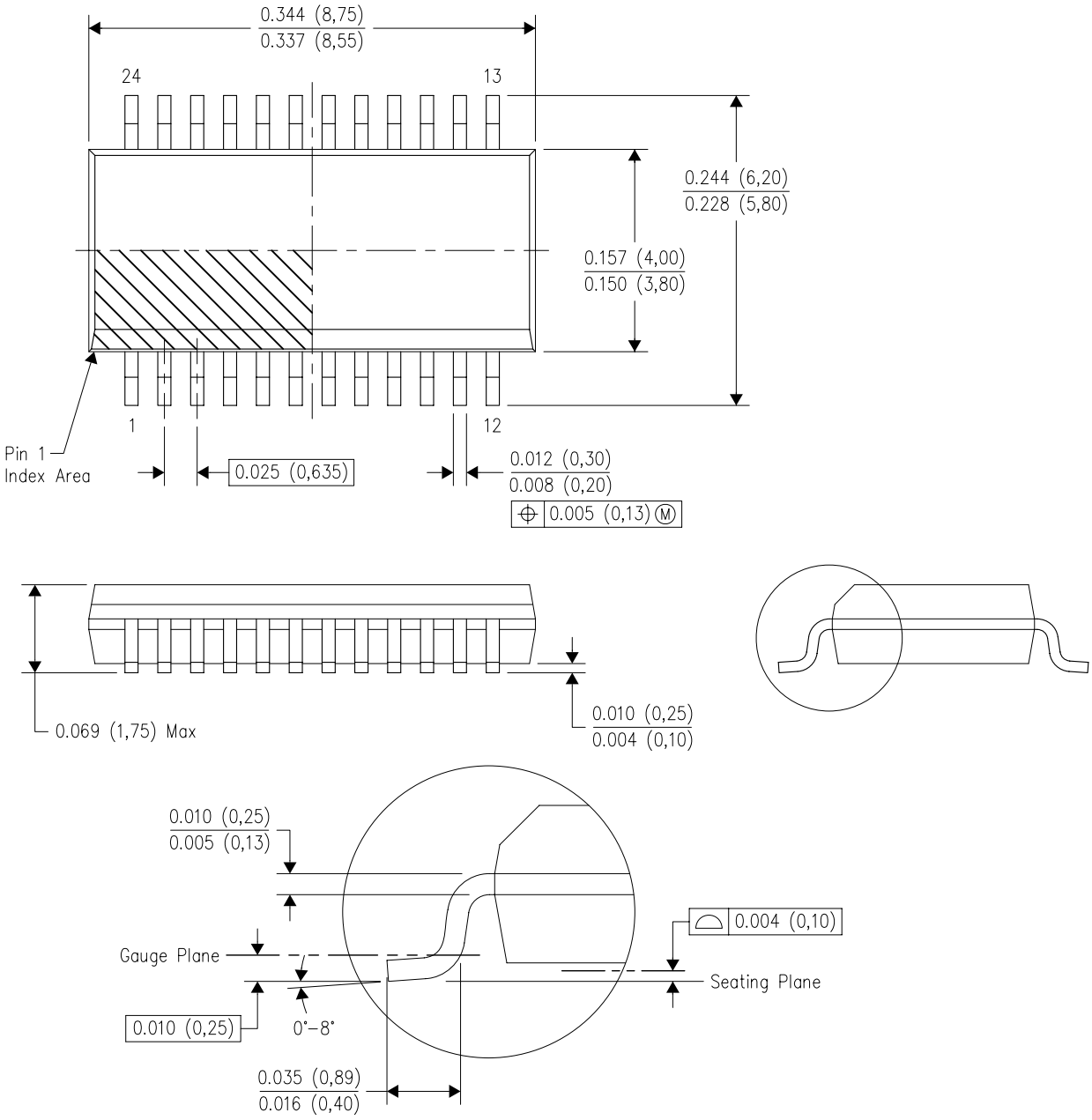
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74LVC8T245PW	PW	TSSOP	24	60	530	10.2	3600	3.5
SN74LVC8T245PW	PW	TSSOP	24	60	530	10.2	3600	3.5
SN74LVC8T245PW.A	PW	TSSOP	24	60	530	10.2	3600	3.5
SN74LVC8T245PW.A	PW	TSSOP	24	60	530	10.2	3600	3.5
SN74LVC8T245PW.B	PW	TSSOP	24	60	530	10.2	3600	3.5
SN74LVC8T245PW.B	PW	TSSOP	24	60	530	10.2	3600	3.5
SN74LVC8T245PWG4	PW	TSSOP	24	60	530	10.2	3600	3.5
SN74LVC8T245PWG4	PW	TSSOP	24	60	530	10.2	3600	3.5

DBQ (R–PDSO–G24) PLASTIC SMALL–OUTLINE PACKAGE



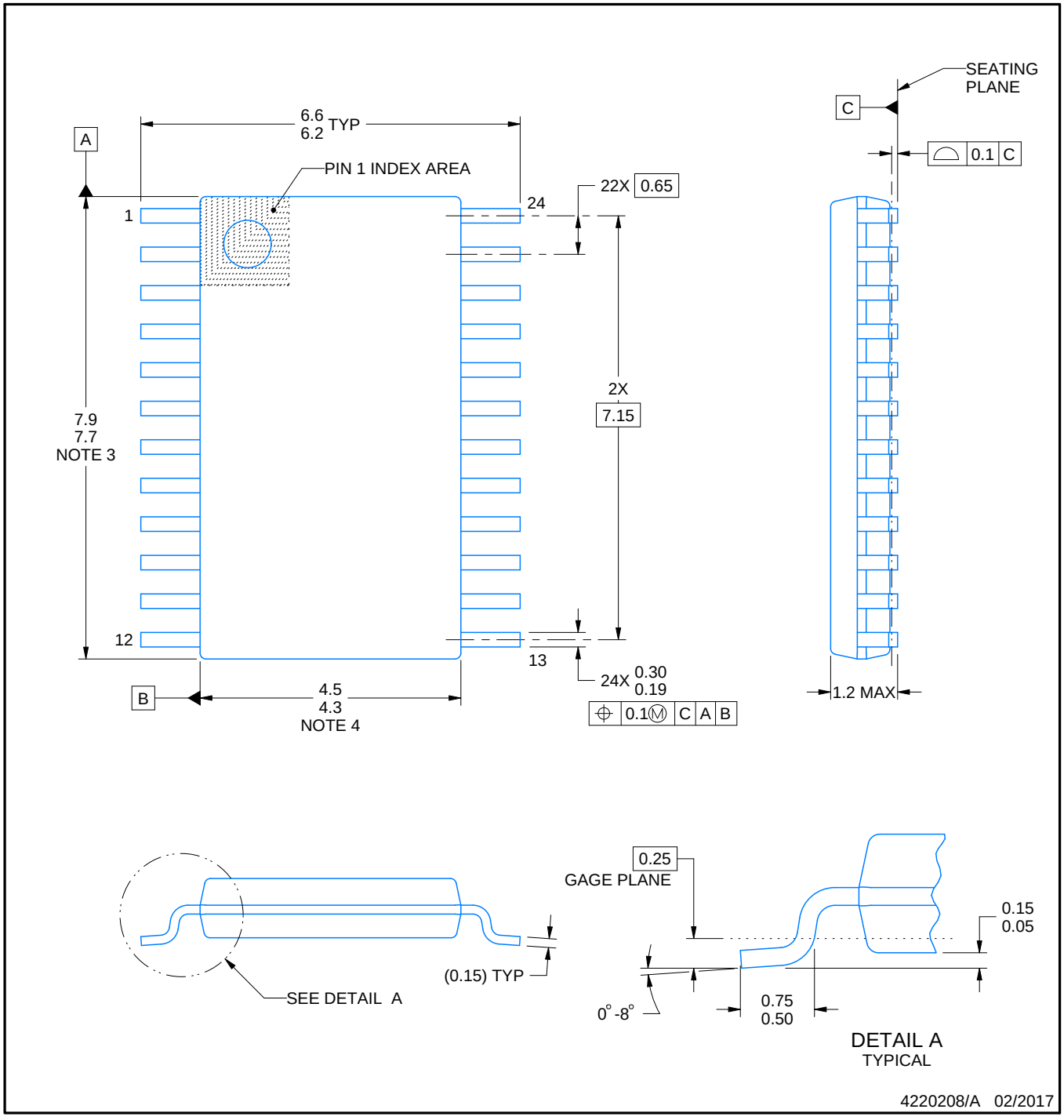
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
D. Falls within JEDEC MO–137 variation AE.

PACKAGE OUTLINE

PW0024A

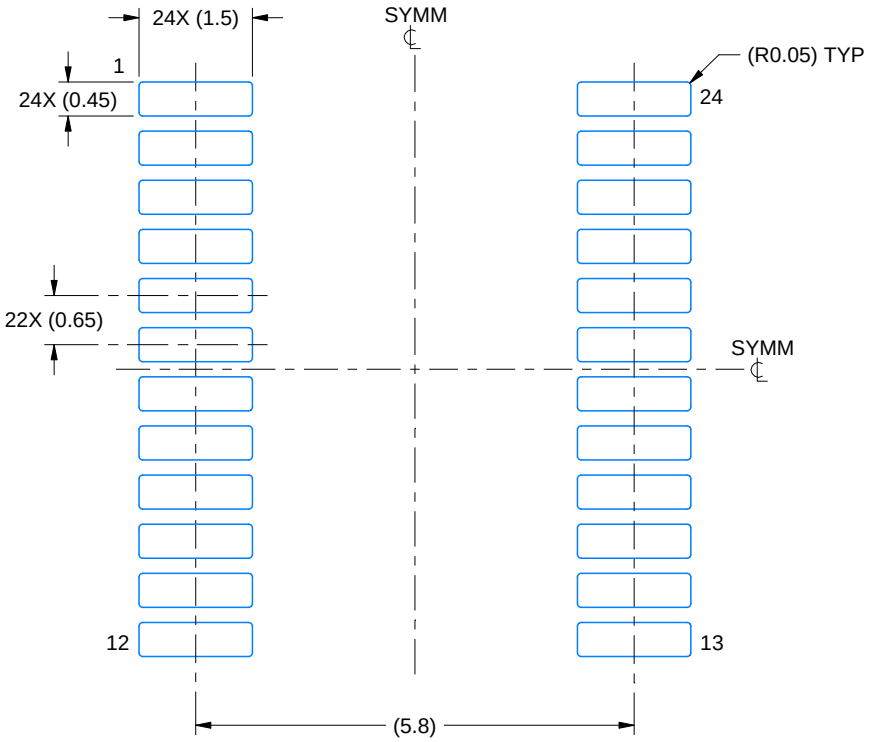
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

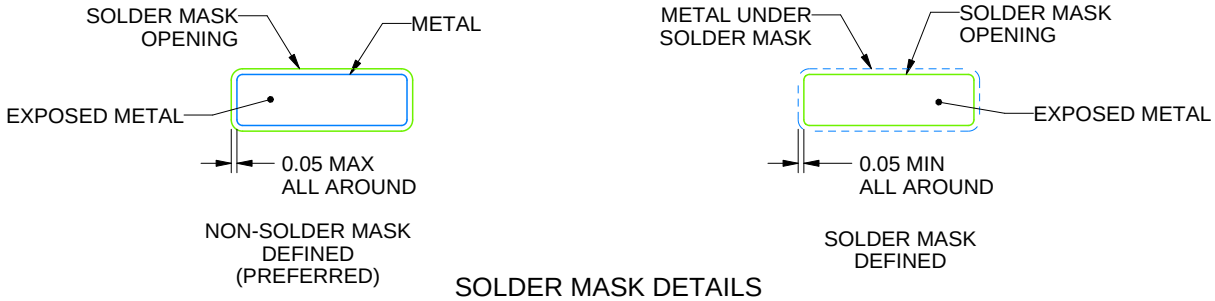


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

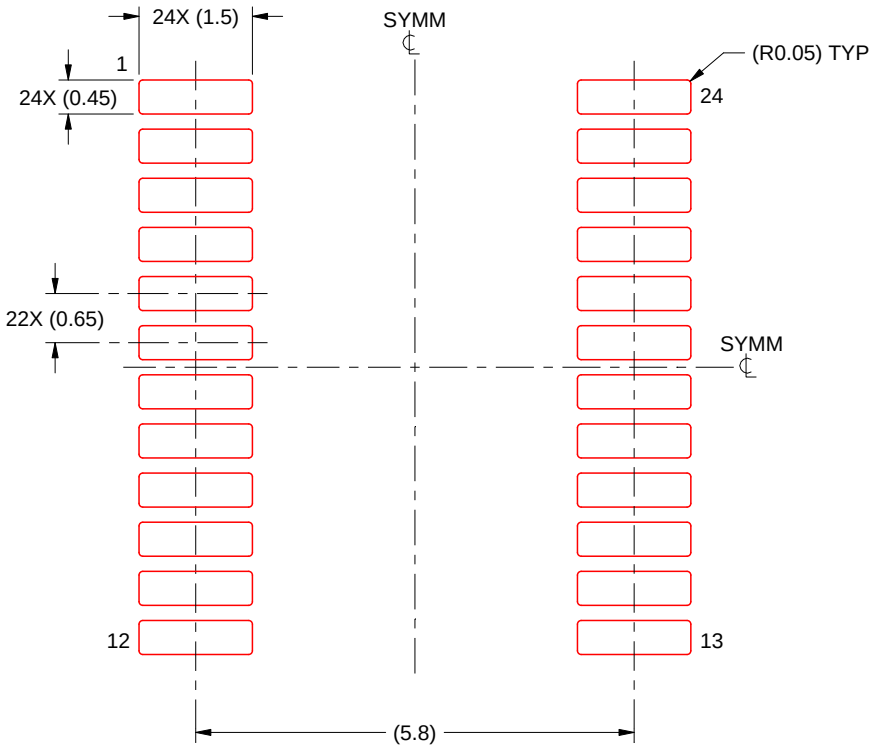


SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

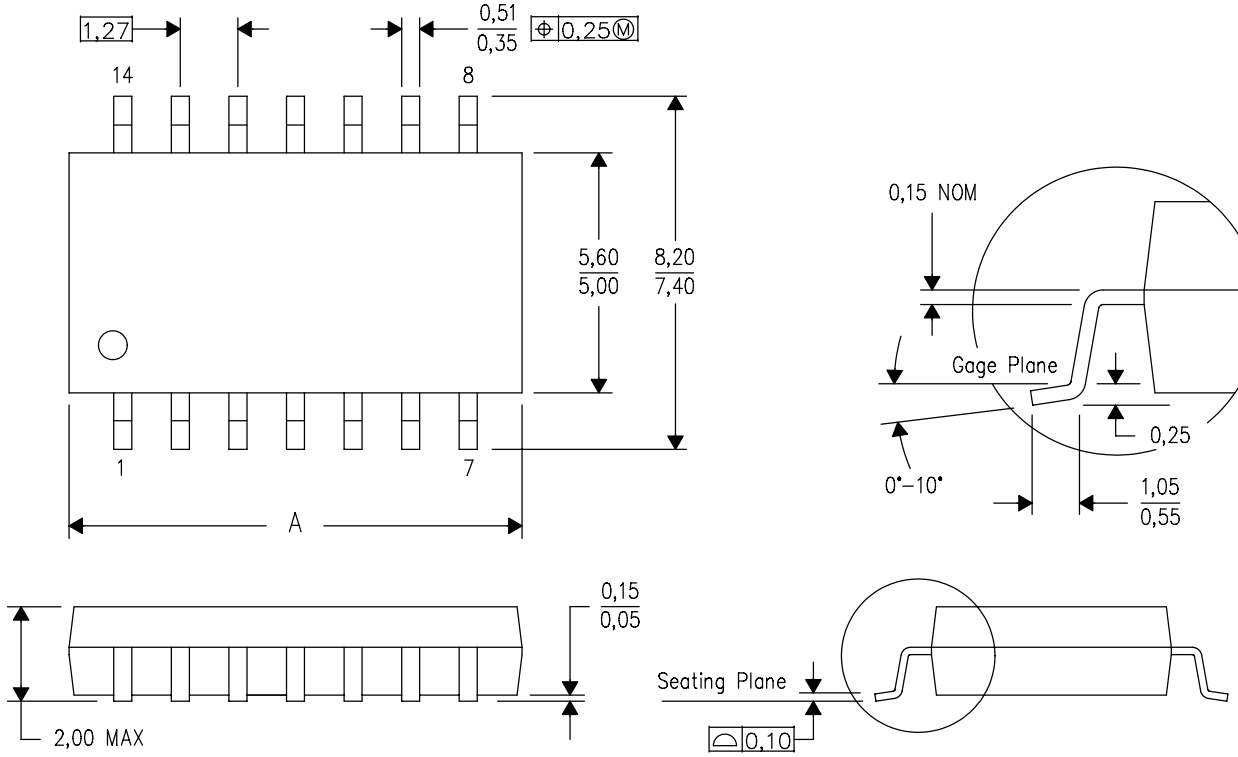
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN

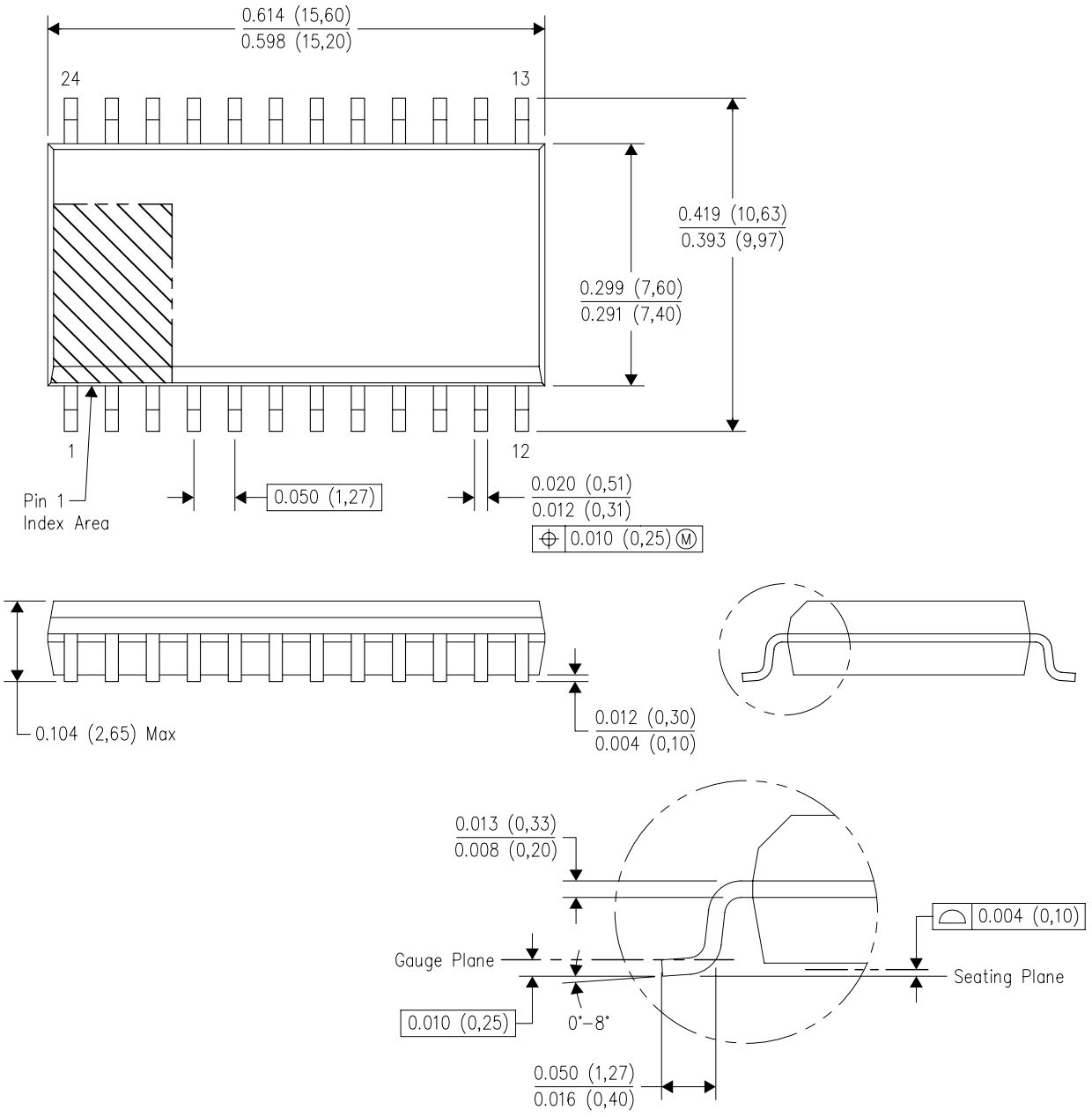


DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE



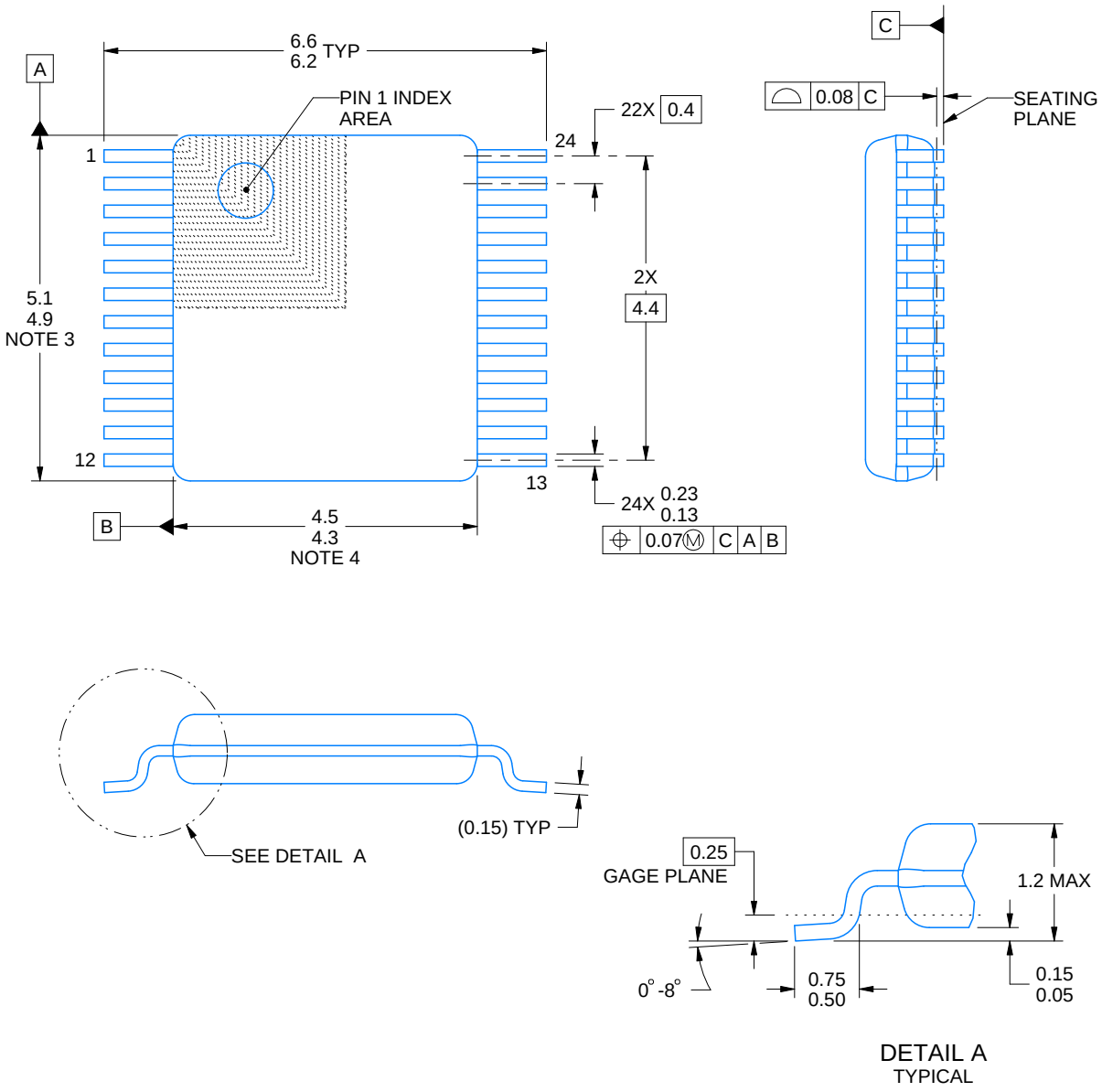
NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

PACKAGE OUTLINE

DGV0024A

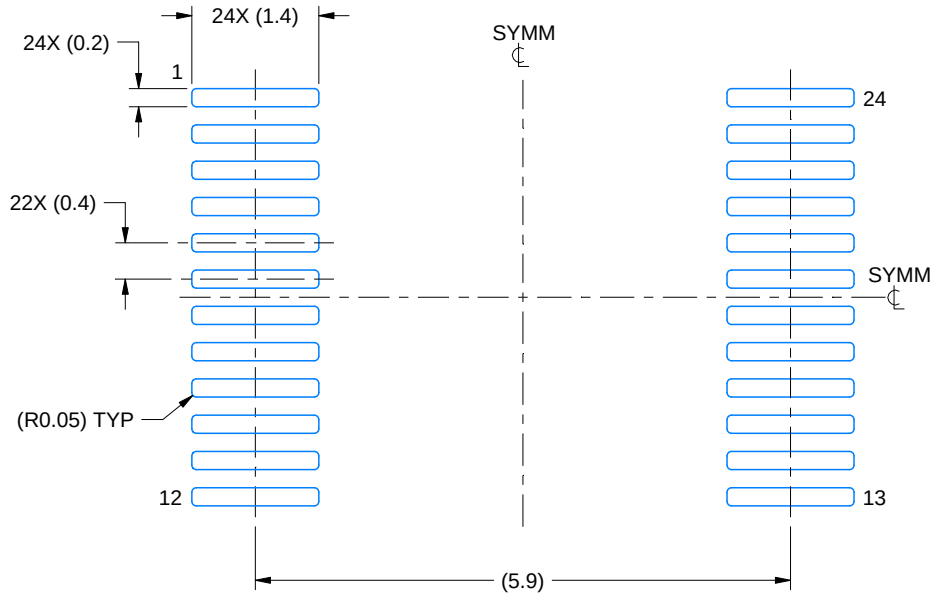
TVSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

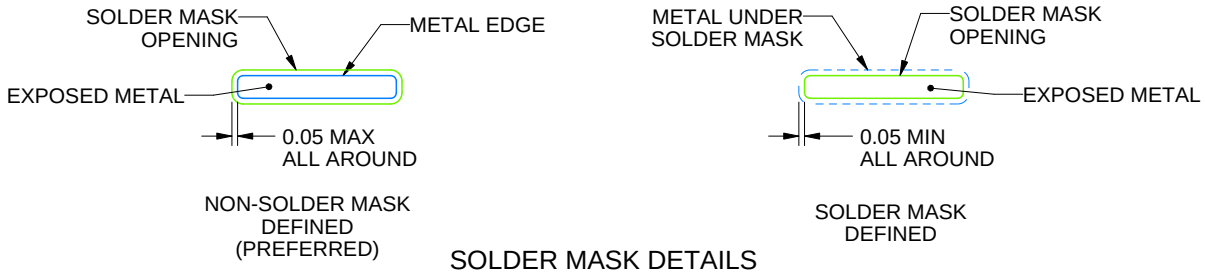


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X

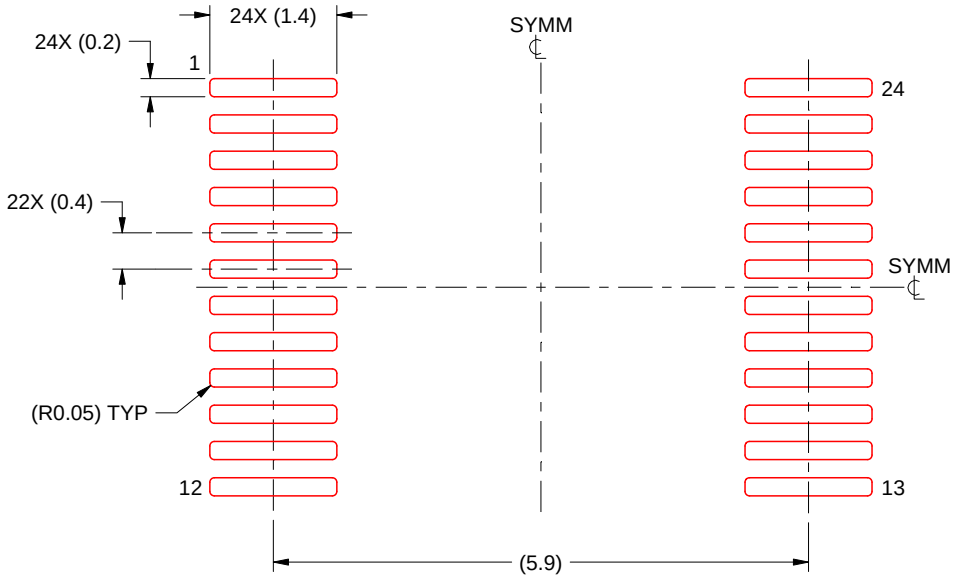


SOLDER MASK DETAILS

4229221/A 12/2022

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 12X

4229221/A 12/2022

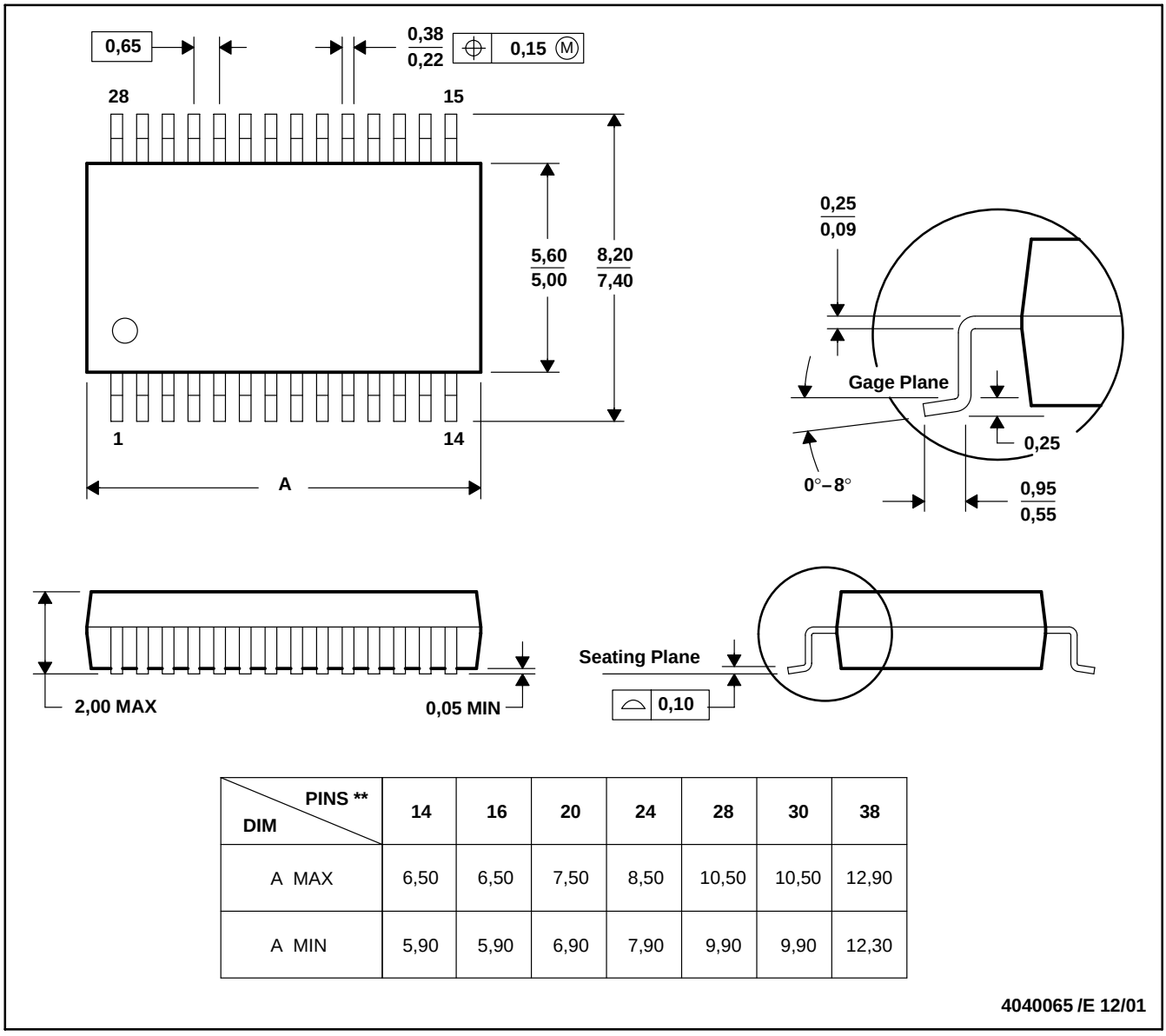
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

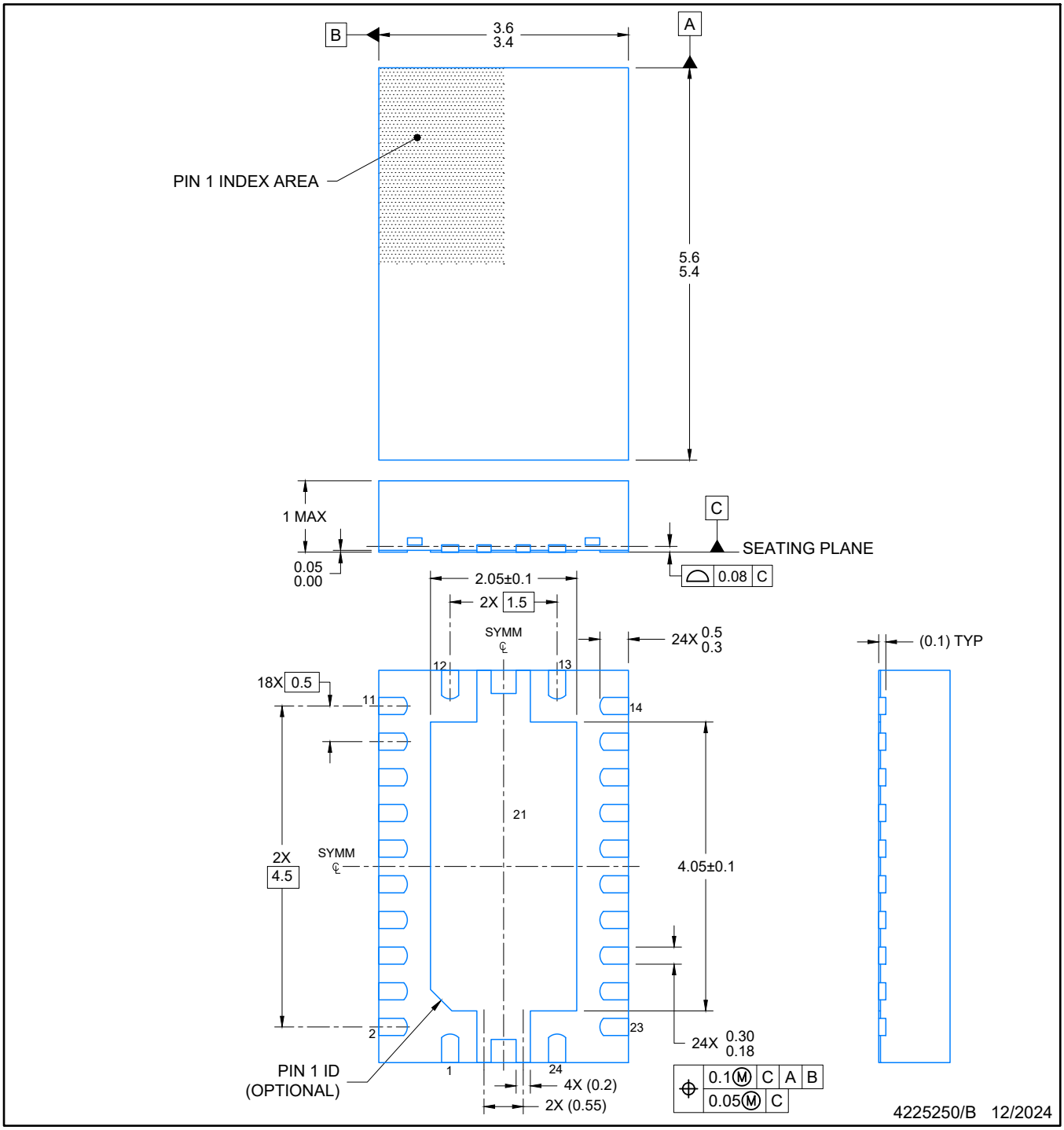
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

PACKAGE OUTLINE

RHL0024A

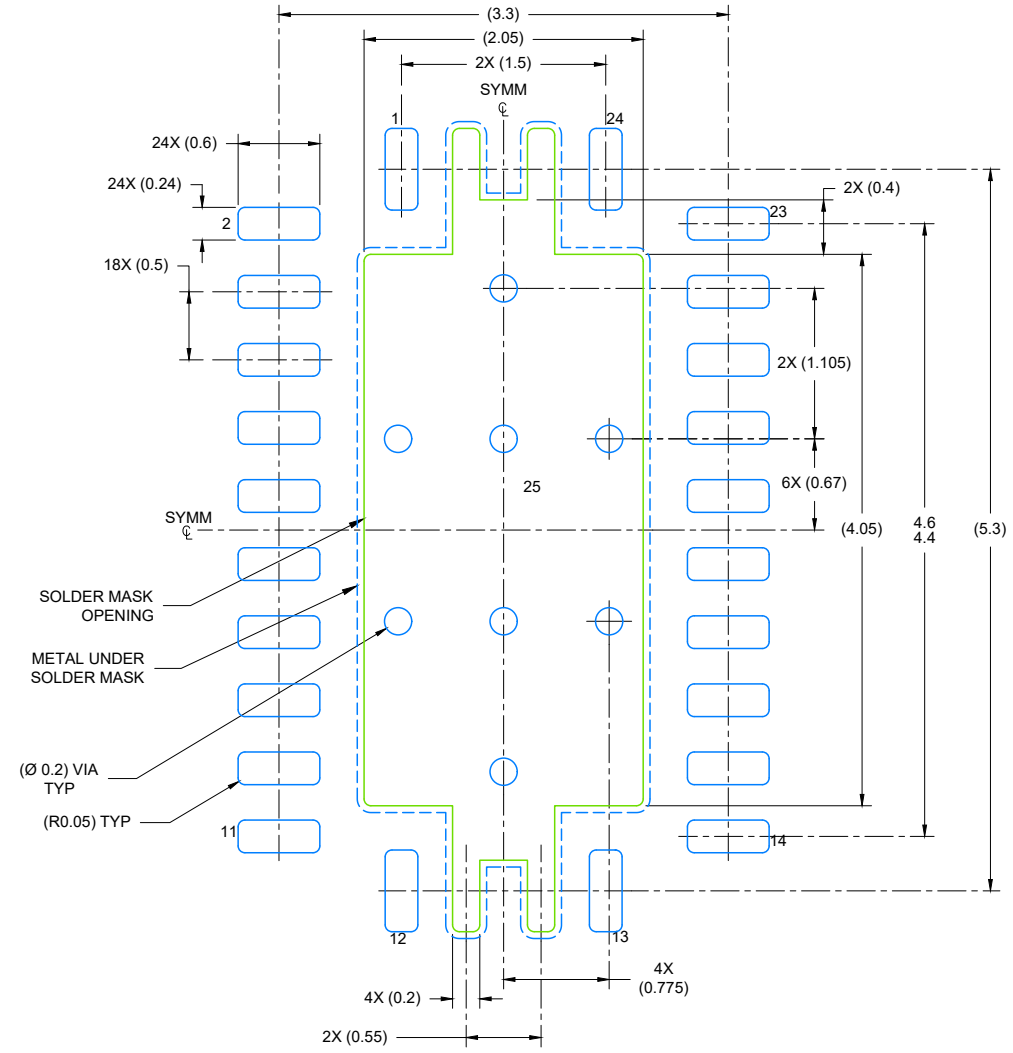
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD

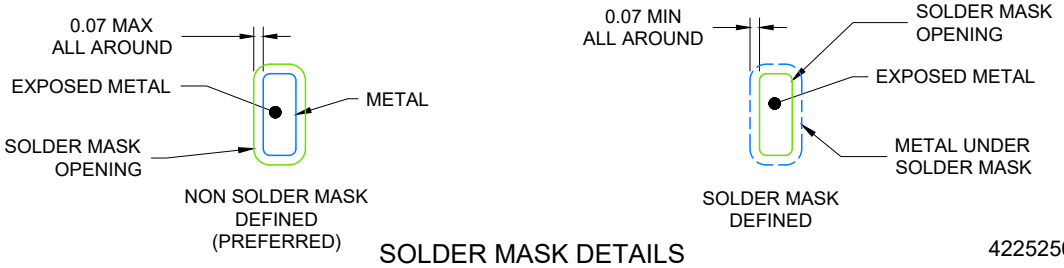


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 18X

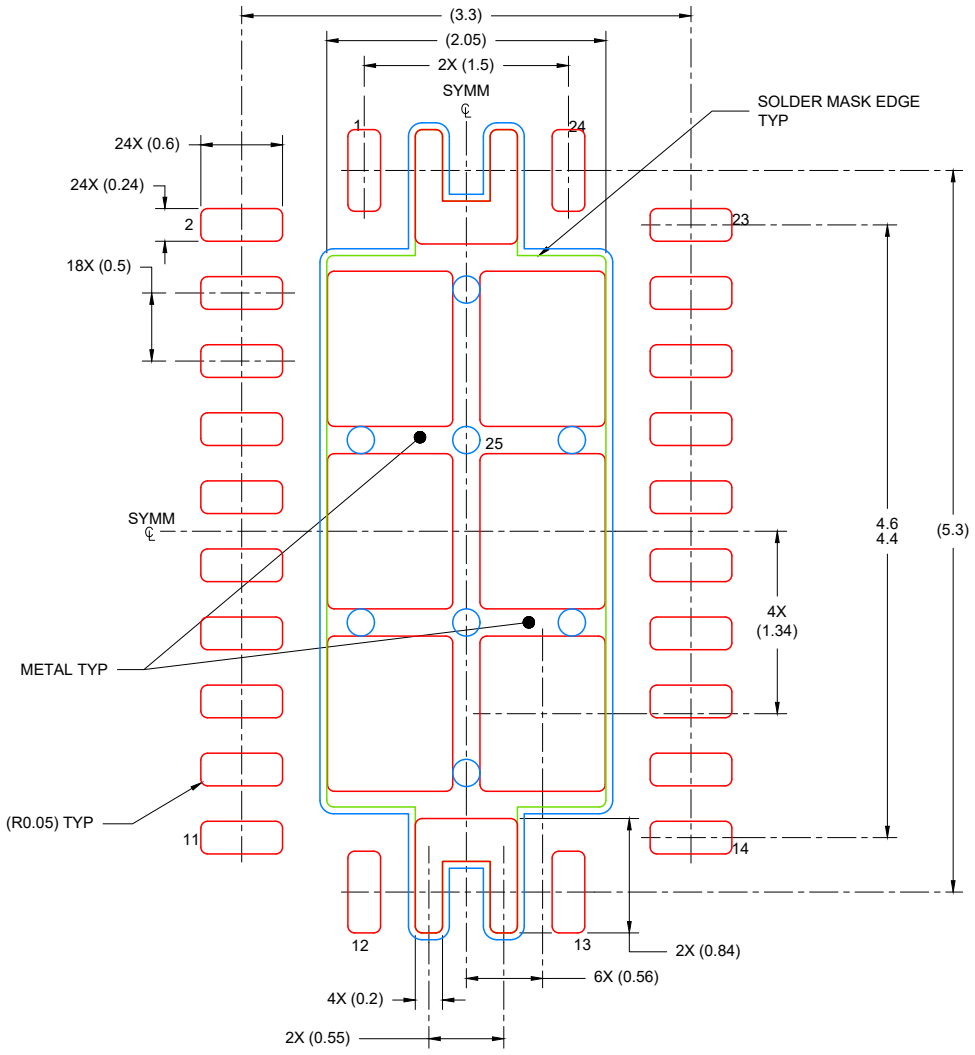


SOLDER MASK DETAILS

4225250/B 12/2024

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED COVERAGE BY AREA
SCALE: 18X

4225250/B 12/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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