Exercício 12:

- Escrever um programa para alternar o estado dos LEDs vermelho e verde da placa MSP-EXP430G2 a cada 500.000 ciclos de *clock*.

- Utilizar o *Timer1_A* para a temporização.

MSP430G2553.h :

```
#define DCO0        (0x20)  /* DCO Select Bit 0 */
#define DCO1        (0x40)  /* DCO Select Bit 1 */
#define DCO2        (0x80)  /* DCO Select Bit 2 */

#define RSEL0       (0x01)  /* Range Select Bit 0 */
#define RSEL1       (0x02)  /* Range Select Bit 1 */
#define RSEL2       (0x04)  /* Range Select Bit 2 */
#define RSEL3       (0x08)  /* Range Select Bit 3 */
```

DCOCTL ← DCO0

BCSCTL1 ← RSEL2 + RSEL1 + RSEL0

DCOCTL	0	0	1	0	0	0	0	0
BCSCTL1	0	0	0	0	0	1	1	1

DCOCTL ← DCO0
BCSCTL1 ← RSEL2 + RSEL1 + RSEL0

DCOCTL ← DCO1 + DCO0
BCSCTL1 ← RSEL3 + RSEL1 + RSEL0

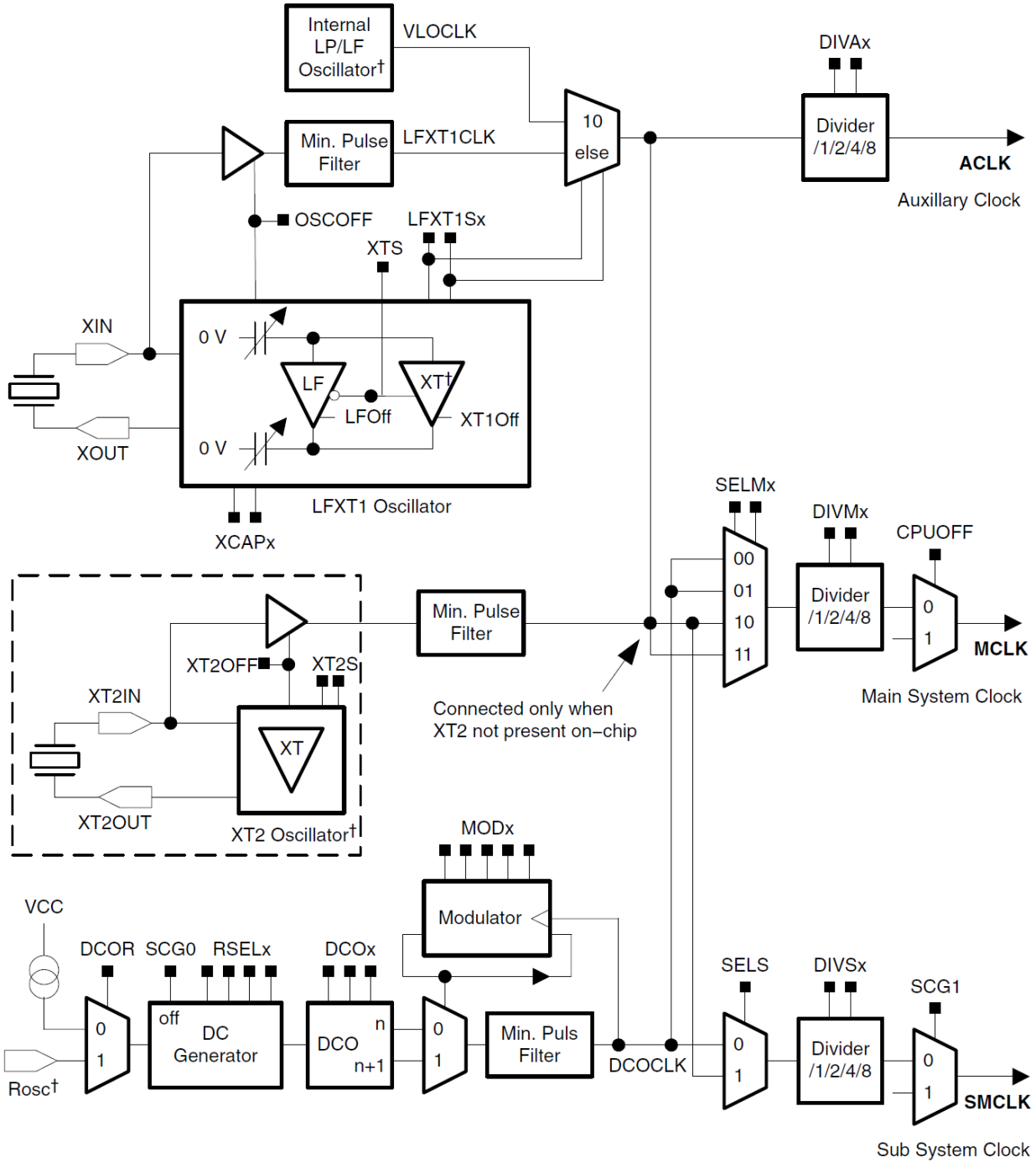
DCOCTL	0	1	1	0	0	0	0	0
BCSCTL1	0	0	0	0	1	0	1	1

DCOCTL ← DCO2
BCSCTL1 ← RSEL3 + RSEL2 + RSEL0

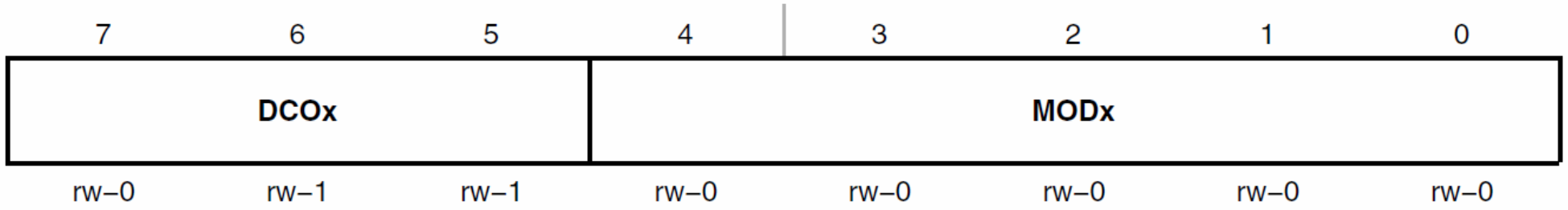
DCOCTL	1	0	0	0	0	0	0	0
BCSCTL1	0	0	0	0	1	1	0	1

DCOCTL ← DCO2
BCSCTL1 ← RSEL3+RSEL2+RSEL1+RSEL0

DCOCTL	1	0	0	0	0	0	0	0
BCSCTL1	0	0	0	0	1	1	1	1

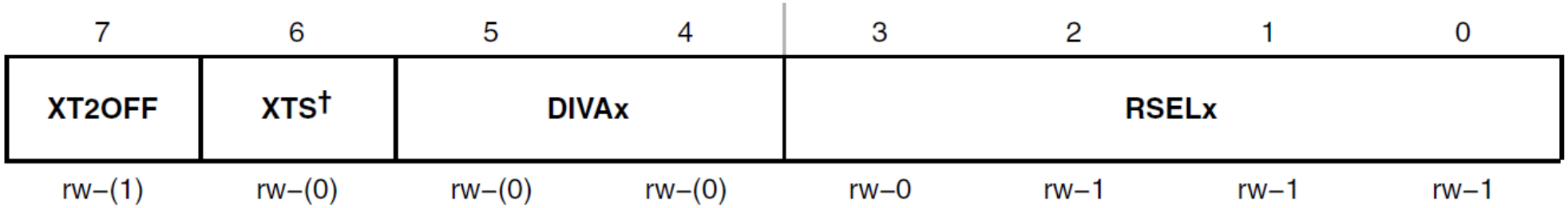

Internal LP/LF Oscillator†
VLOCLK
Min. Pulse Filter
LFXT1CLK
10
else
DIVAx
Divider /1/2/4/8
ACLK
Auxillary Clock
OSCOFF
LFXT1Sx
XTS
XIN
XOUT
0 V
0 V
LF
XT†
LFOff
XT1Off
LFXT1 Oscillator
XCAPx
SELMx
DIVMx
CPUOFF
00
01
10
11
Divider /1/2/4/8
0
1
MCLK
Main System Clock
Min. Pulse Filter
XT2OFF
XT2S
XT2IN
XT
XT2OUT
XT2 Oscillator†
Connected only when XT2 not present on–chip
MODx
Modulator
VCC
DCOR
SCG0
RSELx
DCOx
off
DC Generator
DCO
n
n+1
Rosc†
Min. Puls Filter
DCOCLK
SELS
DIVSx
SCG1
Divider /1/2/4/8
SMCLK
Sub System Clock

DCOCTL, DCO Control Register



DCOx	Bits 7-5	DCO frequency select. These bits select which of the eight discrete DCO frequencies within the range defined by the RSELx setting is selected.
MODx	Bits 4-0	Modulator selection. These bits define how often the f_{DCO+1} frequency is used within a period of 32 DCOCLK cycles. During the remaining clock cycles (32–MOD) the f_{DCO} frequency is used. Not useable when DCOx=7.

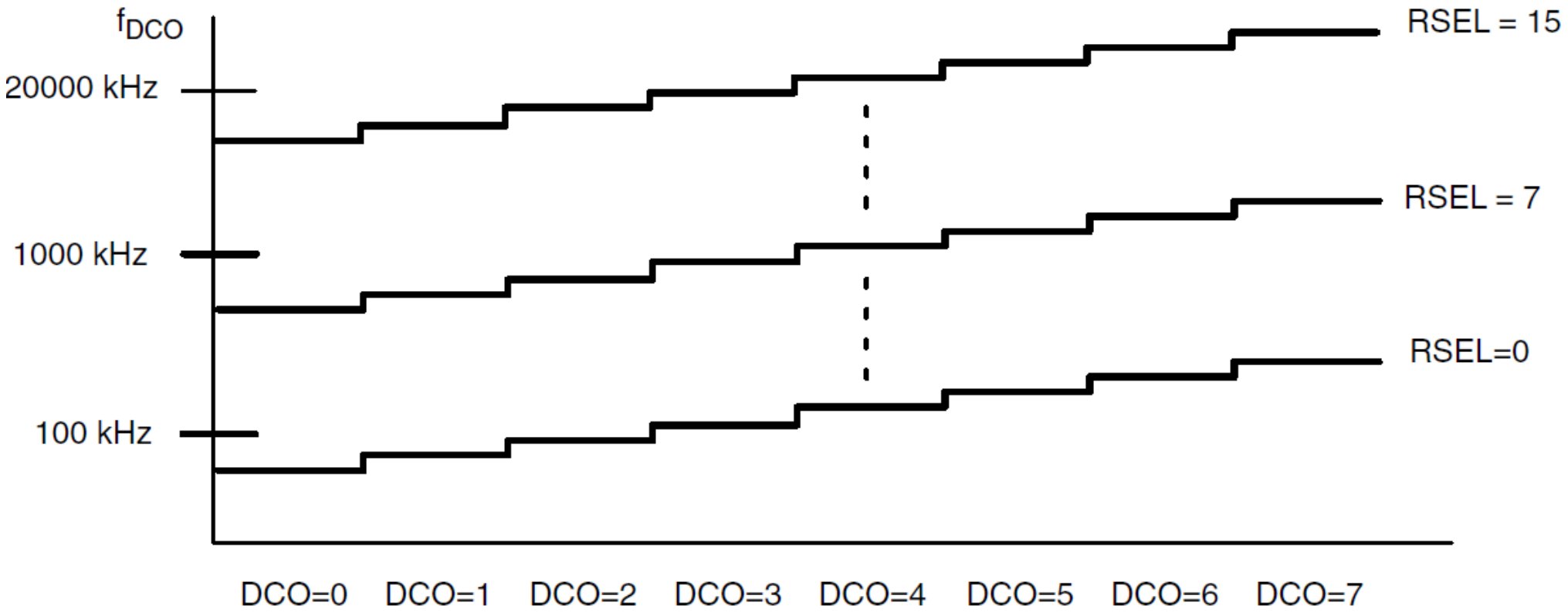
BCSCTL1, Basic Clock System Control Register 1

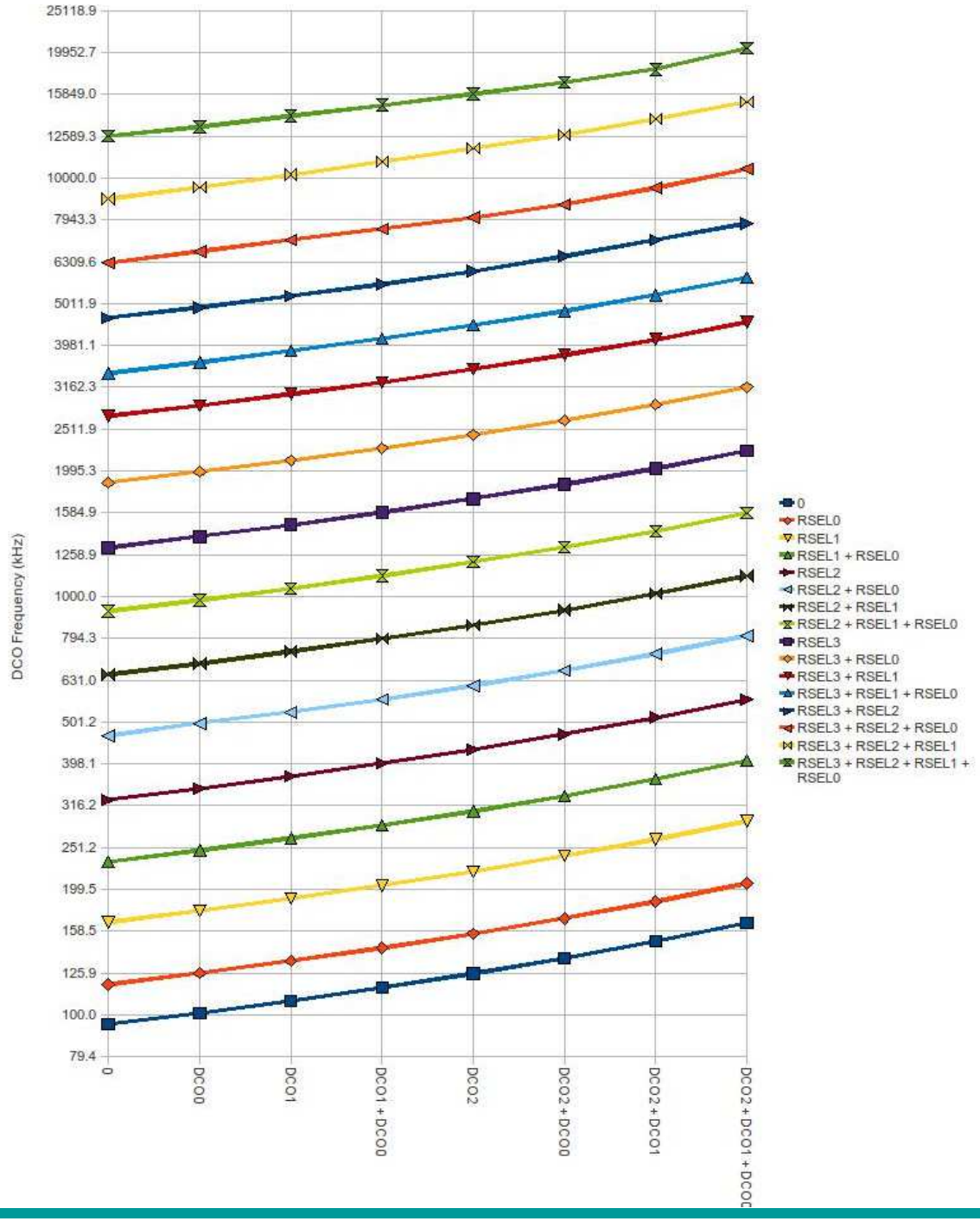


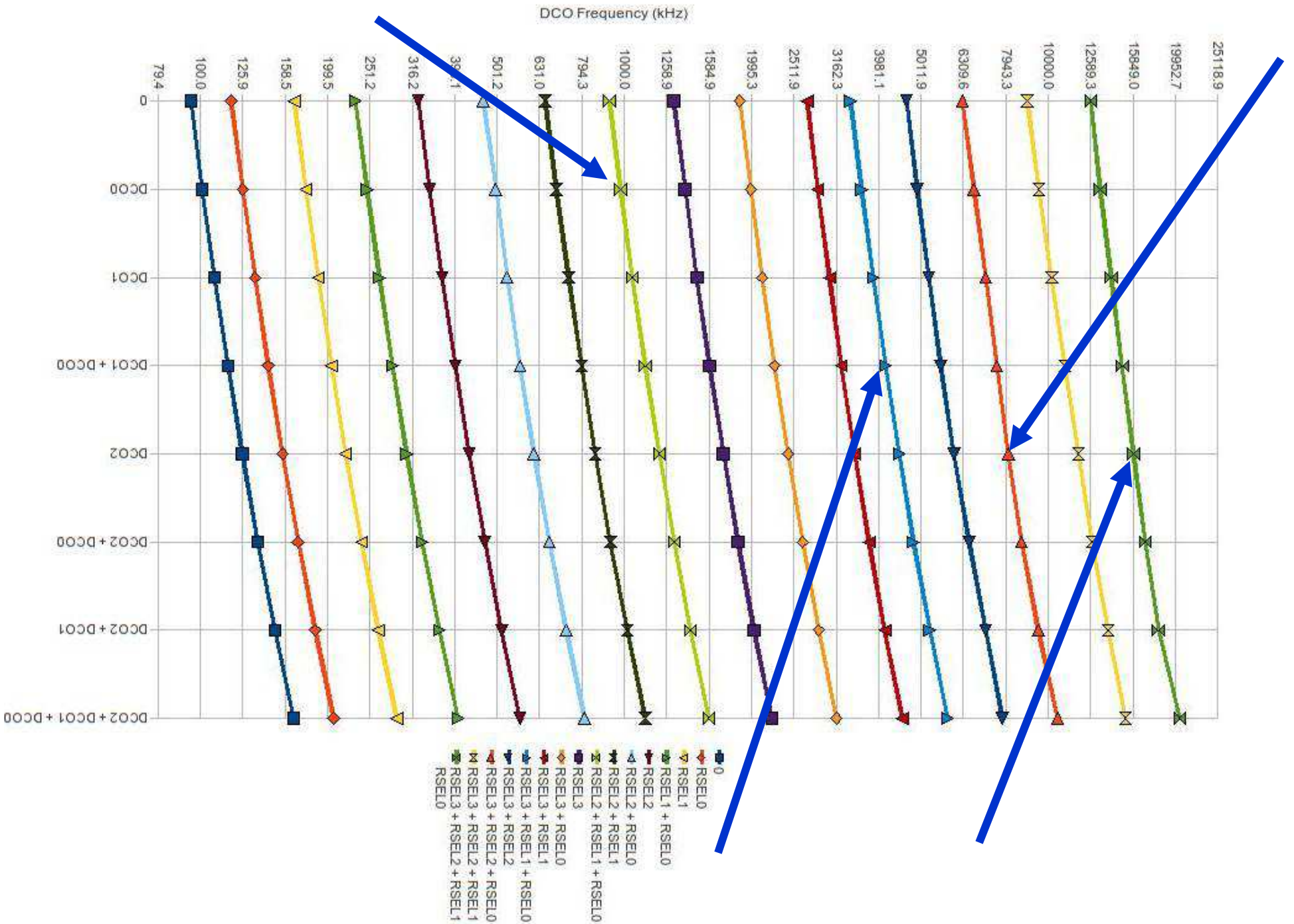
† XTS = 1 is not supported in MSP430x20xx devices.

XT2OFF	Bit 7	XT2 off. This bit turns off the XT2 oscillator 0 XT2 is on 1 XT2 is off if it is not used for MCLK or SMCLK.
XTS	Bit 6	LFXT1 mode select. 0 Low frequency mode 1 High frequency mode
DIVAx	Bits 5-4	Divider for ACLK 00 /1 01 /2 10 /4 11 /8
RSELx	Bits 3-0	Range Select. Sixteen different frequency ranges are available. The lowest frequency range is selected by setting RSELx=0. RSEL3 is ignored when DCOR = 1.

. *Typical DCOx Range and RSELx Steps*




25118.9
19952.7
15849.0
12589.3
10000.0
7943.3
6309.6
5011.9
3981.1
3162.3
2511.9
1995.3
1584.9
1258.9
1000.0
794.3
631.0
501.2
398.1
316.2
251.2
199.5
158.5
125.9
100.0
79.4
DCO Frequency (kHz)
0
DCO0
DCO1
DCO1 + DCO0
DCO2
DCO2 + DCO0
DCO2 + DCO1
DCO2 + DCO1 + DCO0
0
RSEL0
RSEL1
RSEL1 + RSEL0
RSEL2
RSEL2 + RSEL0
RSEL2 + RSEL1
RSEL2 + RSEL1 + RSEL0
RSEL3
RSEL3 + RSEL0
RSEL3 + RSEL1
RSEL3 + RSEL1 + RSEL0
RSEL3 + RSEL2
RSEL3 + RSEL2 + RSEL0
RSEL3 + RSEL2 + RSEL1
RSEL3 + RSEL2 + RSEL1 + RSEL0


DCO Frequency (kHz)
79.4
100.0
125.9
158.5
199.5
251.2
316.2
501.2
631.0
794.3
1000.0
1258.9
1584.9
1995.3
2511.9
3162.3
3981.1
5011.9
6309.6
7943.3
10000.0
12589.3
15849.0
19952.7
25118.9
0
DCO0
DCO1
DCO1 + DCO0
DCO2
DCO2 + DCO0
DCO2 + DCO1
DCO2 + DCO1 + DCO0
RSEL3 + RSEL2 + RSEL1 + RSEL0
RSEL3 + RSEL2 + RSEL1
RSEL3 + RSEL2 + RSEL0
RSEL3 + RSEL2
RSEL3 + RSEL1 + RSEL0
RSEL3 + RSEL1
RSEL3 + RSEL0
RSEL3
RSEL2 + RSEL1 + RSEL0
RSEL2 + RSEL1
RSEL2 + RSEL0
RSEL2
RSEL1 + RSEL0
RSEL1
RSEL0
0

	0	DCO0	DCO1	DCO1 + DCO0	DCO2	DCO2 + DCO0	DCO2 + DCO1	DCO2 + DCO1 + DCO0
0	94.9	101.0	108.1	116.2	125.6	136.7	149.9	166.0
RSEL0	118.1	125.8	134.5	144.6	156.4	170.1	186.6	206.5
RSEL1	166.6	177.4	189.7	203.8	220.2	239.6	262.7	290.7
RSEL1 + RSEL0	232.1	247.2	264.3	283.9	306.8	333.8	365.8	404.8
RSEL2	326.5	347.7	371.7	399.3	431.1	468.8	513.5	567.8
RSEL2 + RSEL0	465.0	497.8	528.8	567.6	612.8	665.5	728.9	805.8
RSEL2 + RSEL1	650.1	691.5	738.5	792.4	855.1	927.5	1015.1	1121.4
RSEL2 + RSEL1 + RSEL0	921.6	980.2	1046.1	1121.1	1209.3	1310.3	1433.0	1581.1
RSEL3	1308.5	1390.7	1483.5	1588.5	1712.0	1852.8	2023.4	2229.9
RSEL3 + RSEL0	1871.1	1986.2	2116.6	2263.4	2436.6	2634.8	2874.5	3165.0
RSEL3 + RSEL1	2698.8	2861.8	3046.5	3252.6	3497.6	3776.8	4114.9	4529.0
RSEL3 + RSEL1 + RSEL0	3413.7	3623.8	3862.5	4129.0	4446.5	4812.9	5255.0	5786.7
RSEL3 + RSEL2	4629.0	4910.4	5229.8	5579.2	5994.8	6501.5	7121.3	7796.6
RSEL3 + RSEL2 + RSEL0	6281.3	6678.6	7118.2	7564.9	8056.5	8640.2	9469.0	10522.0
RSEL3 + RSEL2 + RSEL1	8917.6	9499.4	10187.0	10928.9	11788.0	12680.8	13824.4	15197.5
RSEL3 + RSEL2 + RSEL1 + RSEL0	12584.2	13266.5	14093.8	14939.9	15895.6	16915.7	18199.7	20405.3

```
#define CALDCO_16MHZ_    (0x10F8u)  /* DCOCTL  Calibration Data for 16MHz */
#define CALBC1_16MHZ_    (0x10F9u)  /* BCSCTL1 Calibration Data for 16MHz */
#define CALDCO_12MHZ_    (0x10FAu)  /* DCOCTL  Calibration Data for 12MHz*/
#define CALBC1_12MHZ_    (0x10FBu)  /* BCSCTL1 Calibration Data for 12MHz */
#define CALDCO_8MHZ_     (0x10FCu)  /* DCOCTL  Calibration Data for 8MHz */
#define CALBC1_8MHZ_     (0x10FDu)  /* BCSCTL1 Calibration Data for 8MHz */
#define CALDCO_1MHZ_     (0x10FEu)  /* DCOCTL  Calibration Data for 1MHz */
#define CALBC1_1MHZ_     (0x10FFu)  /* BCSCTL1 Calibration Data for 1MHz */
```

BCSCTL1 ← CALBC1_*x*MHZ;

DCOCTL ← CALDCO_*x*MHZ;