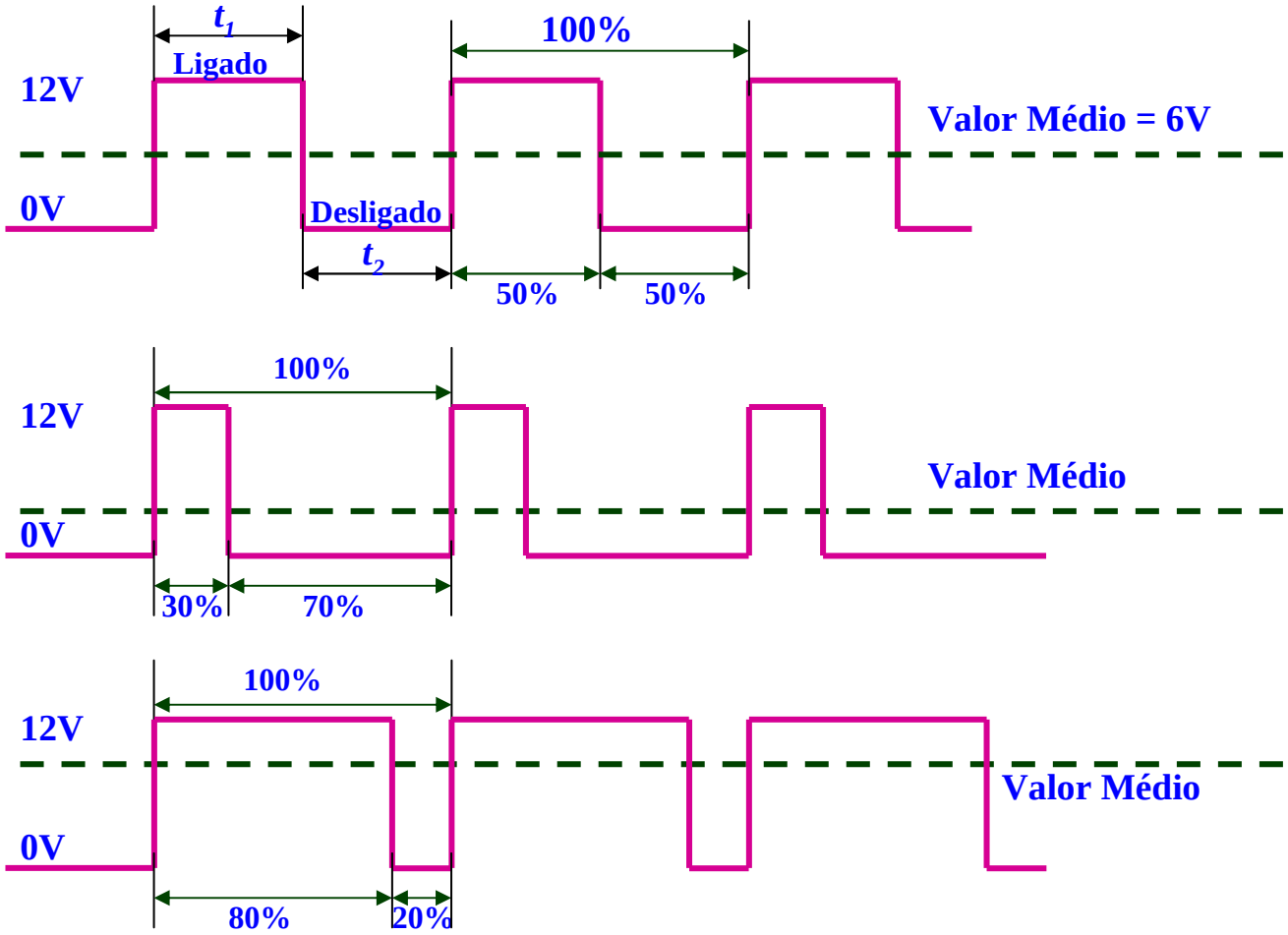
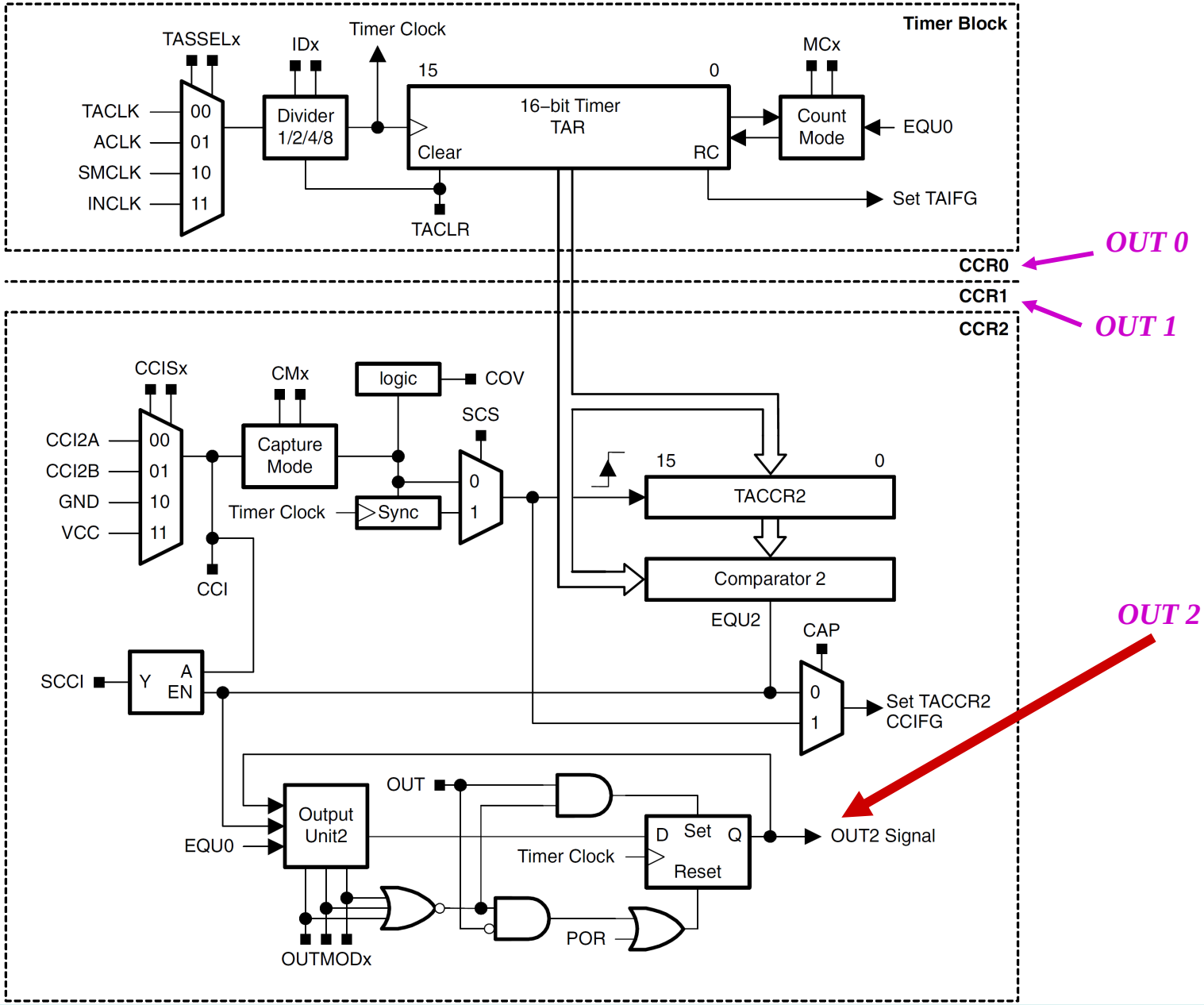
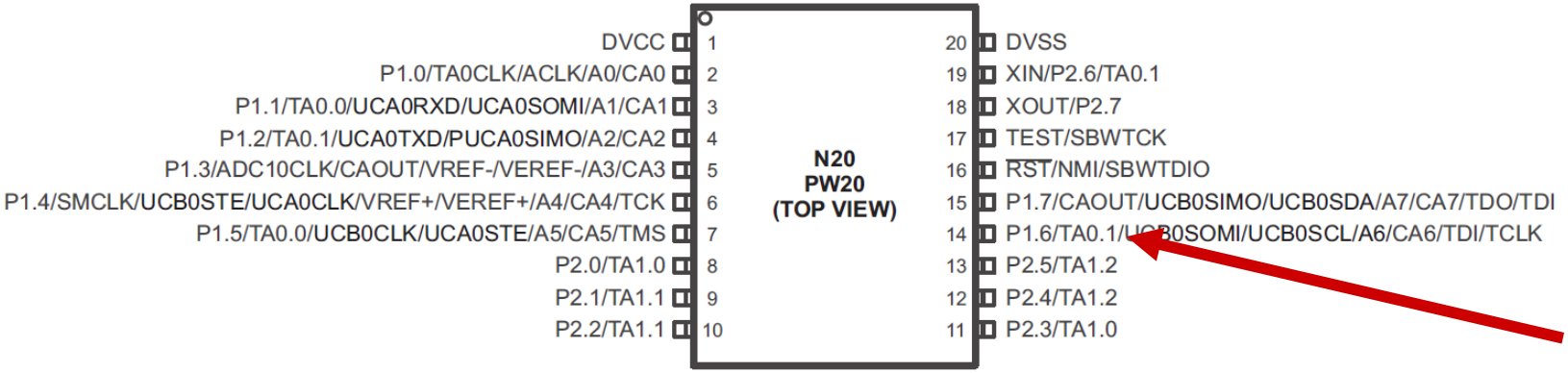
Exercício: Escrever um programa para controlar a luminosidade do LED Verde da placa (*P1.6*) através de PWM.

- **Utilizar o *Conversor AD* para variar a luminosidade**
- **Utilizar o *Timer0_A* para gerar o PWM**

PWM: Pulse Width Modulation




Timer Block
TASSELx
IDx
Timer Clock
MCx
15
0
TACLK
ACLK
SMCLK
INCLK
00
01
10
11
Divider 1/2/4/8
16–bit Timer TAR
Clear
RC
Count Mode
EQU0
Set TAIFG
TACLR
CCR0
CCR1
CCR2
OUT 0
OUT 1
CCISx
CMx
logic
COV
SCS
CCI2A
CCI2B
GND
VCC
Capture Mode
Timer Clock
Sync
TACCR2
Comparator 2
EQU2
CCI
SCCI
Y
A
EN
CAP
Set TACCR2 CCIFG
OUT 2
OUT
Output Unit2
EQU0
D
Set
Q
Reset
Timer Clock
OUT2 Signal
POR
OUTMODx



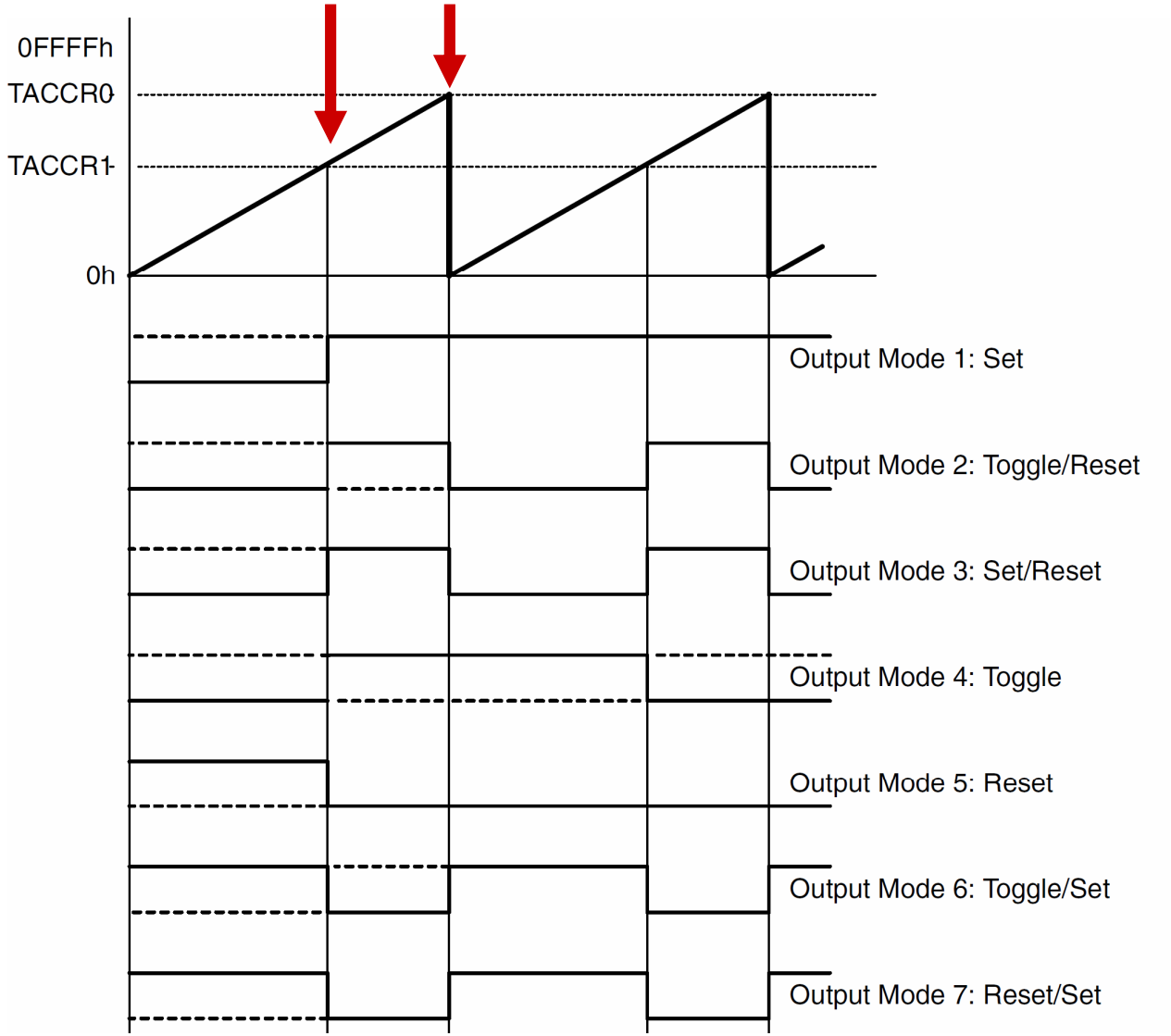
TERMINAL				I/O	DESCRIPTION
NAME	NO.				
	PW20, N20	PW28	RHB32		
P1.6/	14	22	21	I/O	General-purpose digital I/O pin
TA0.1/					Timer0_A, compare: Out1 output
A6/					ADC10 analog input A6(1)
CA6/					Comparator_A+, CA6 input
UCB0SOMI/					USCI_B0 slave out/master in SPI mode,
UCB0SCL/					USCI_B0 SCL I2C clock in I2C mode
TDI/TCLK					JTAG test data input or test clock input during programming and test

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS / SIGNALS[1]					
			P1DIR.x	P1SEL.x	P1SEL2.x	ADC10AE.x INCH.x=1[2]	JTAG Mode	CAPD.y
P1.6/	6	P1.x (I/O)	I: 0; O: 1	0	0	0	0	0
TA0.1/		TA0.1	1	1	0	0	0	0
UCB0SOMI/		UCB0SOMI	from USCI	1	1	0	0	0
UCB0SCL/		UCB0SCL	from USCI	1	1	0	0	0
A6[2]/		A6	X	X	X	1 (y = 6)	0	0
CA6		CA6	X	X	X	0	0	1 (y = 6)
TDI/TCLK/		TDI/TCLK	X	X	X	0	1	0
Pin Osc		Capacitive sensing	X	0	1	0	0	0

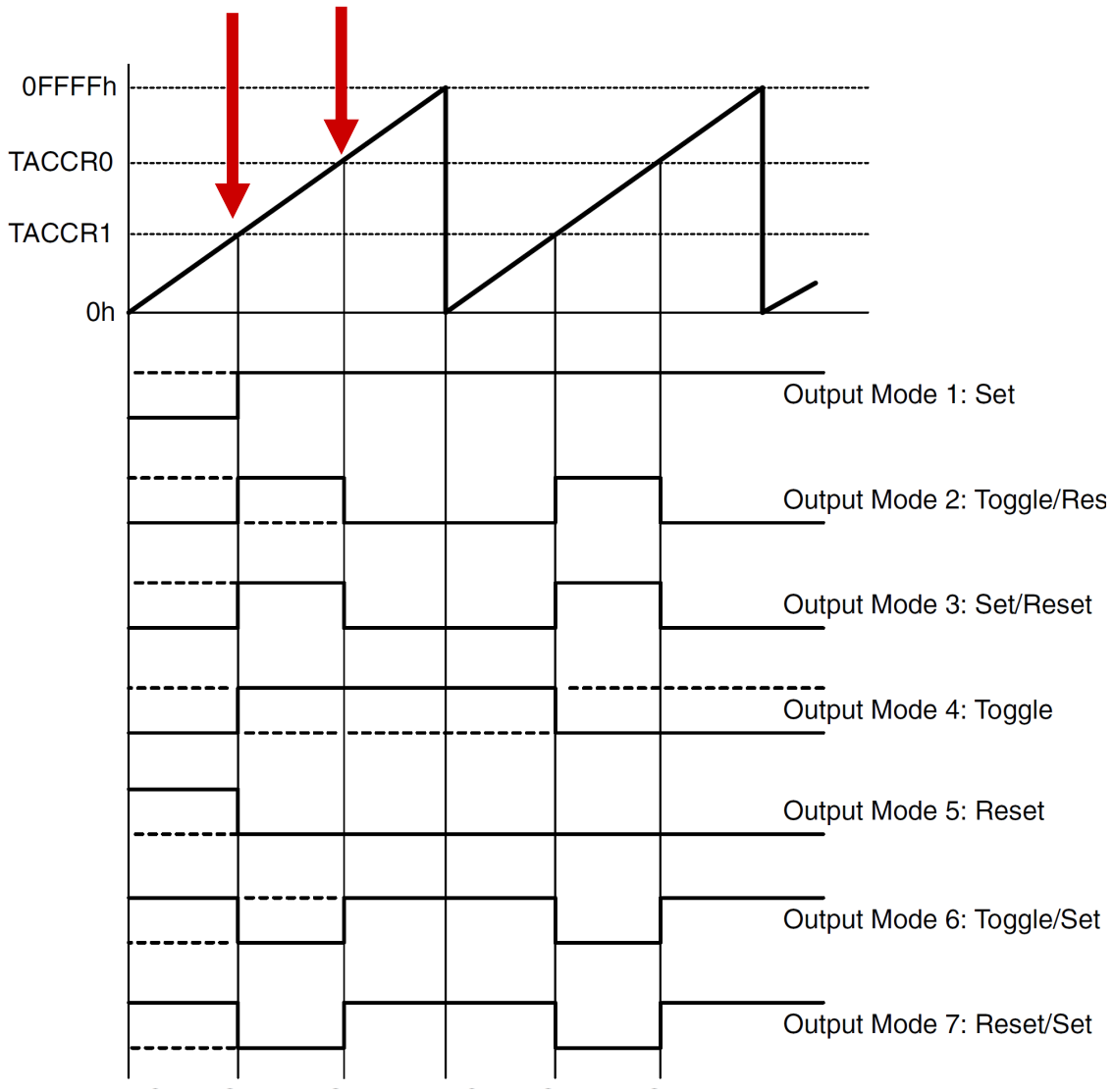
Table 12–2. Output Modes

OUTMODx	Mode	Description
000	Output	The output signal OUTx is defined by the OUTx bit. The OUTx signal updates immediately when OUTx is updated.
001	Set	The output is set when the timer *counts* to the TACCRx value. It remains set until a reset of the timer, or until another output mode is selected and affects the output.
010	Toggle/Reset	The output is toggled when the timer *counts* to the TACCRx value. It is reset when the timer *counts* to the TACCR0 value.
011	Set/Reset	The output is set when the timer *counts* to the TACCRx value. It is reset when the timer *counts* to the TACCR0 value.
100	Toggle	The output is toggled when the timer *counts* to the TACCRx value. The output period is double the timer period.
101	Reset	The output is reset when the timer *counts* to the TACCRx value. It remains reset until another output mode is selected and affects the output.
110	Toggle/Set	The output is toggled when the timer *counts* to the TACCRx value. It is set when the timer *counts* to the TACCR0 value.
111	Reset/Set	The output is reset when the timer *counts* to the TACCRx value. It is set when the timer *counts* to the TACCR0 value.

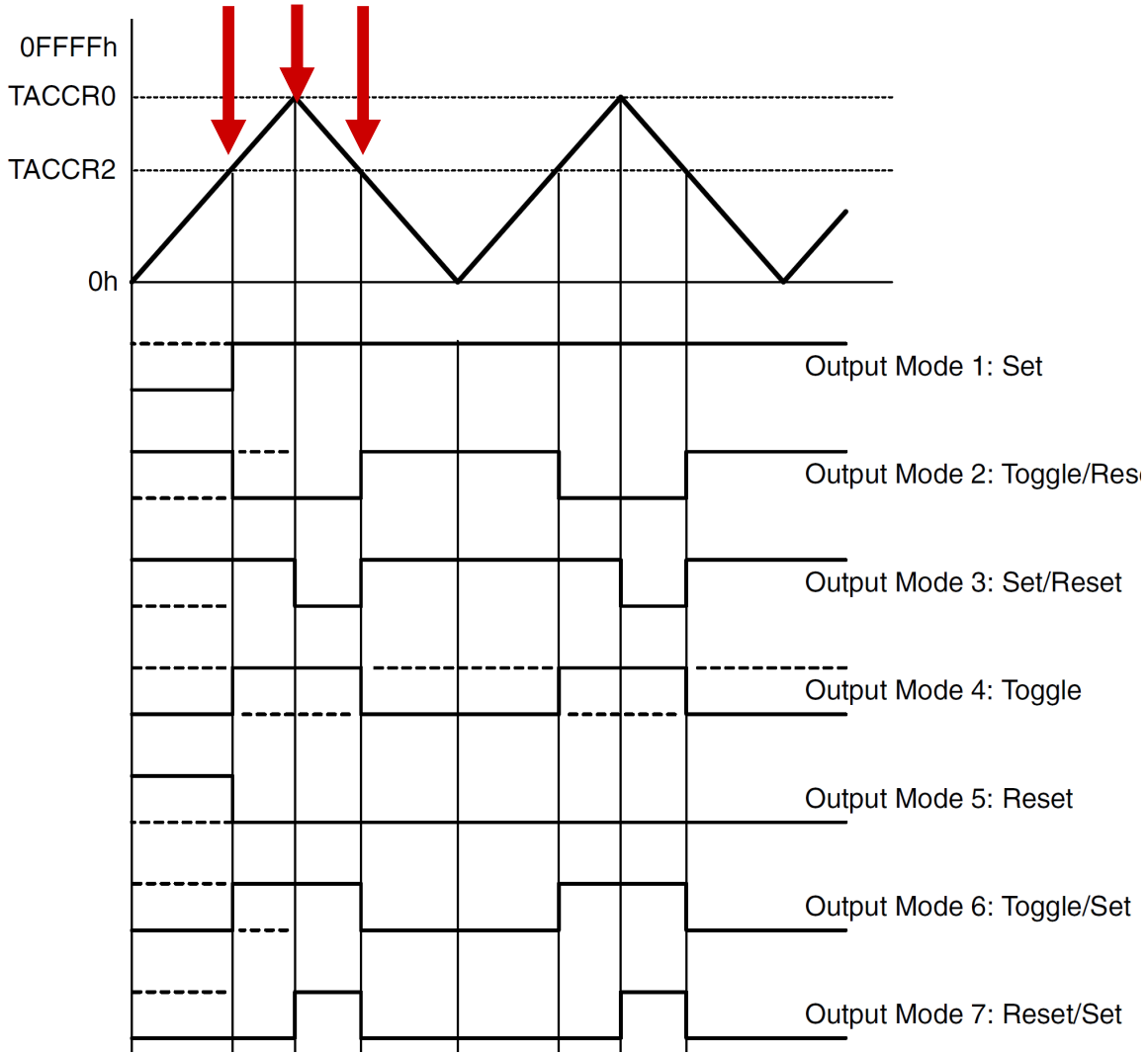
Geração de *PWM* através do *Timer0_A* – *UP Mode*



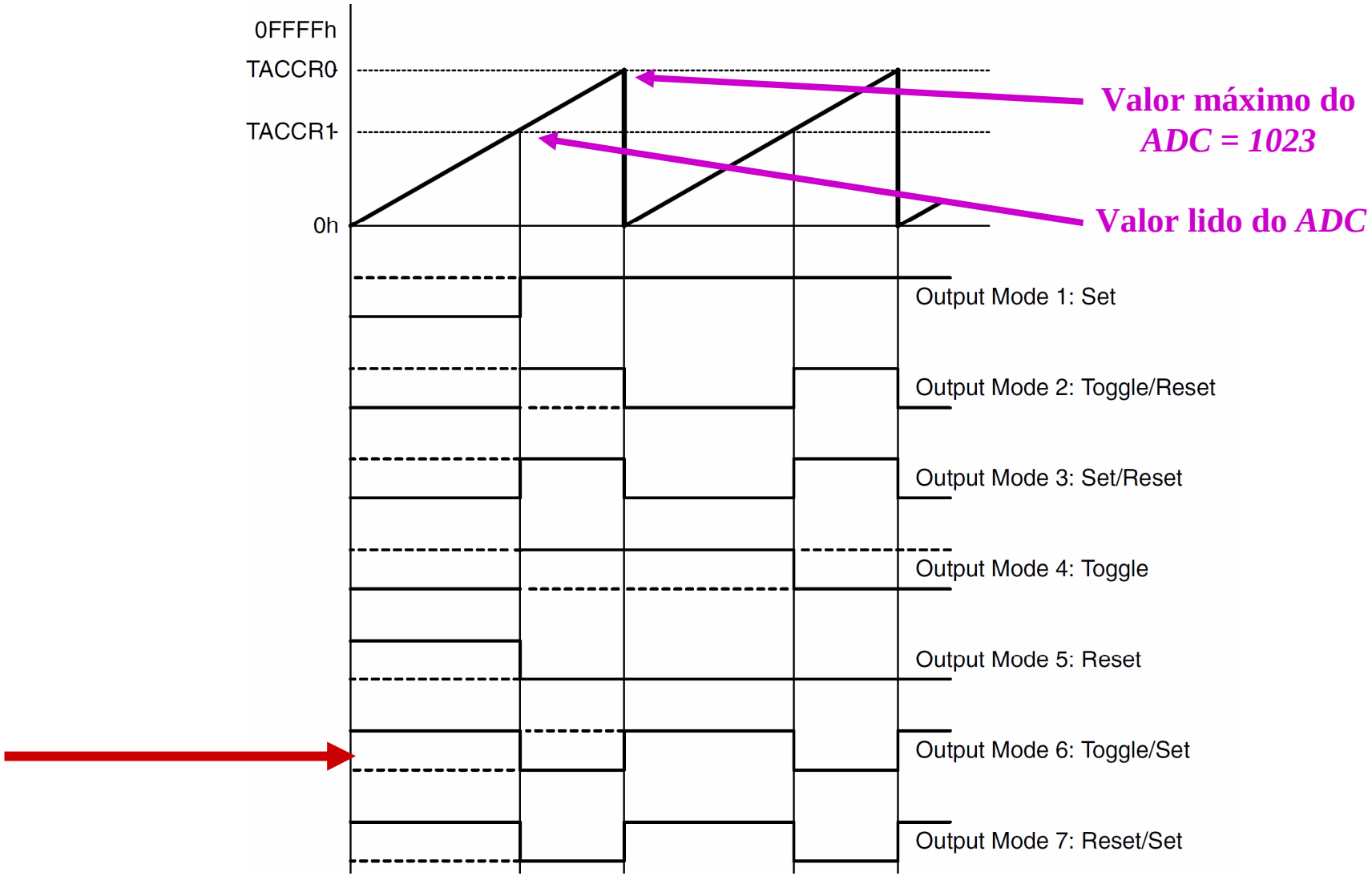
Geração do *PWM* através do *Timer0_A* – *Continuos Mode*



Geração do *PWM* através do *Timer0_A* – *UP/Down Mode*



Geração de *PWM* através do *Timer0_A* – *UP Mode*



TACTL, Timer_A Control Register

TA0CTL

15	14	13	12	11	10	9	8
Unused						TASSELx	
rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)

7	6	5	4	3	2	1	0
IDx		MCx		Unused	TACLR	TAIE	TAIFG
rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	w–(0)	rw–(0)	rw–(0)

Unused Bits 15-10 Unused

TASSELx Bits 9-8 Timer_A clock source select
- 00 TACLK
- 01 ACLK
- 10 SMCLK
- 11 INCLK

IDx Bits 7-6 Input divider. These bits select the divider for the input clock.
- 00 /1
- 01 /2
- 10 /4
- 11 /8

MCx Bits 5-4 Mode control. Setting MCx = 00h when Timer_A is not in use conserves power.
- 00 Stop mode: the timer is halted.
- 01 Up mode: the timer counts up to TACCR0.
- 10 Continuous mode: the timer counts up to 0FFFFh.
- 11 Up/down mode: the timer counts up to TACCR0 then down to 0000h.

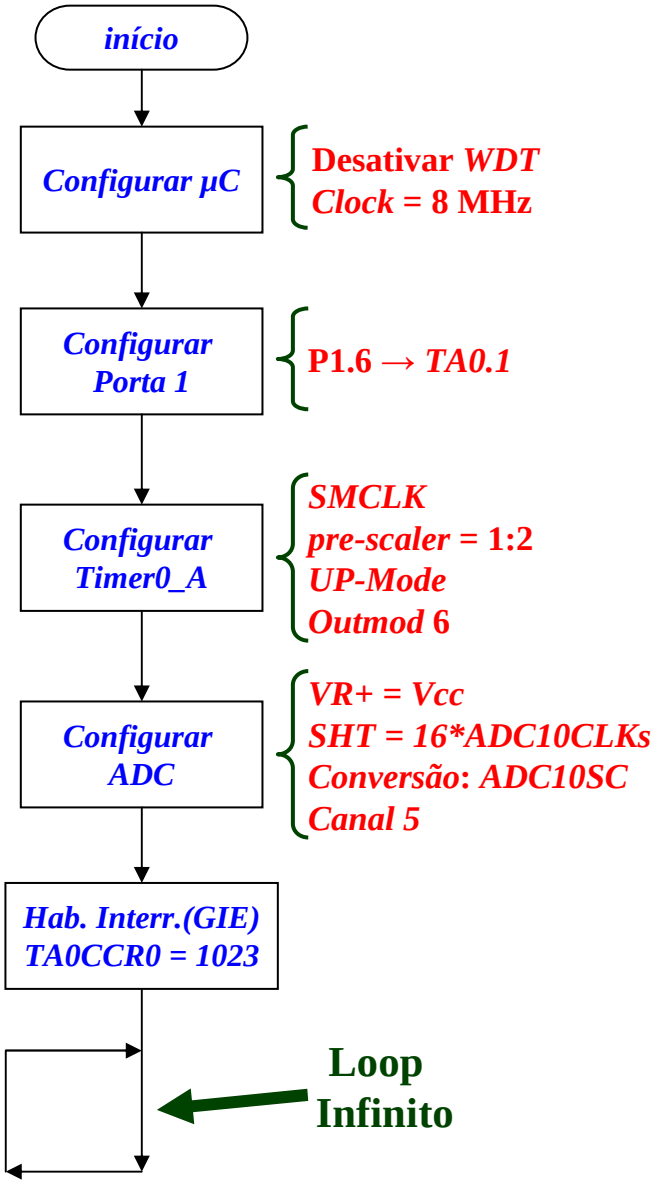
TACCTLx, Capture/Compare Control Register *TA0CCTL1*

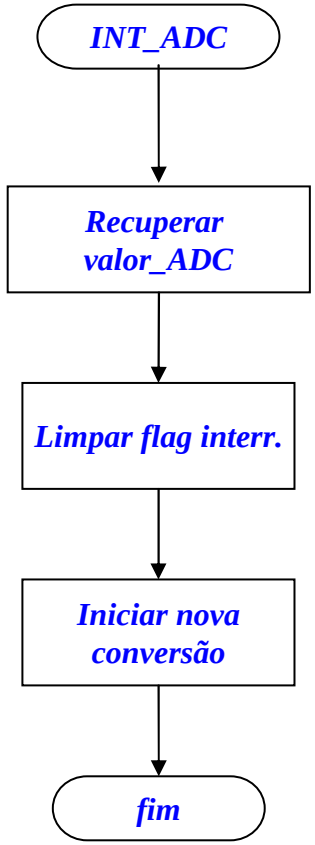
15	14	13	12	11	10	9	8
CMx		CCISx		SCS	SCCI	Unused	CAP
rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	r	r0	rw–(0)

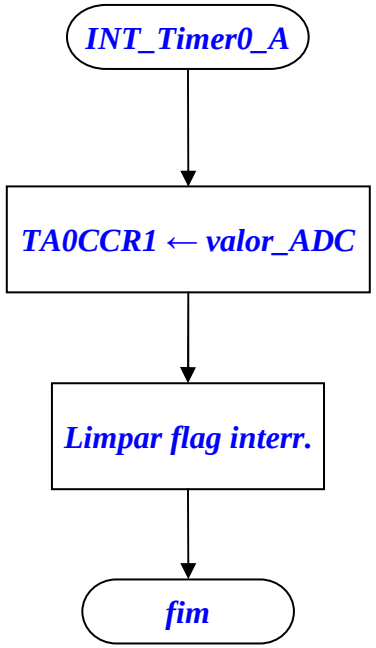
7	6	5	4	3	2	1	0
OUTMODx			CCIE	CCI	OUT	COV	CCIFG
rw–(0)	rw–(0)	rw–(0)	rw–(0)	r	rw–(0)	rw–(0)	rw–(0)

OUTMODx Bits 7-5 Output mode. Modes 2, 3, 6, and 7 are not useful for TACCR0 because EQUx = EQU0.

000 OUT bit value
001 Set
010 Toggle/reset
011 Set/reset
100 Toggle
101 Reset
110 Toggle/set
111 Reset/set


início
Configurar µC
Desativar WDT
Clock = 8 MHz
Configurar Porta 1
P1.6 → TA0.1
Configurar Timer0_A
SMCLK
pre-scaler = 1:2
UP-Mode
Outmod 6
Configurar ADC
VR+ = Vcc
SHT = 16*ADC10CLKs
Conversão: ADC10SC
Canal 5
Hab. Interr.(GIE)
TA0CCR0 = 1023
Loop Infinito


INT_ADC
Recuperar valor_ADC
Limpar flag interr.
Iniciar nova conversão
fim


INT_Timer0_A
TA0CCR1 ← valor_ADC
Limpar flag interr.
fim