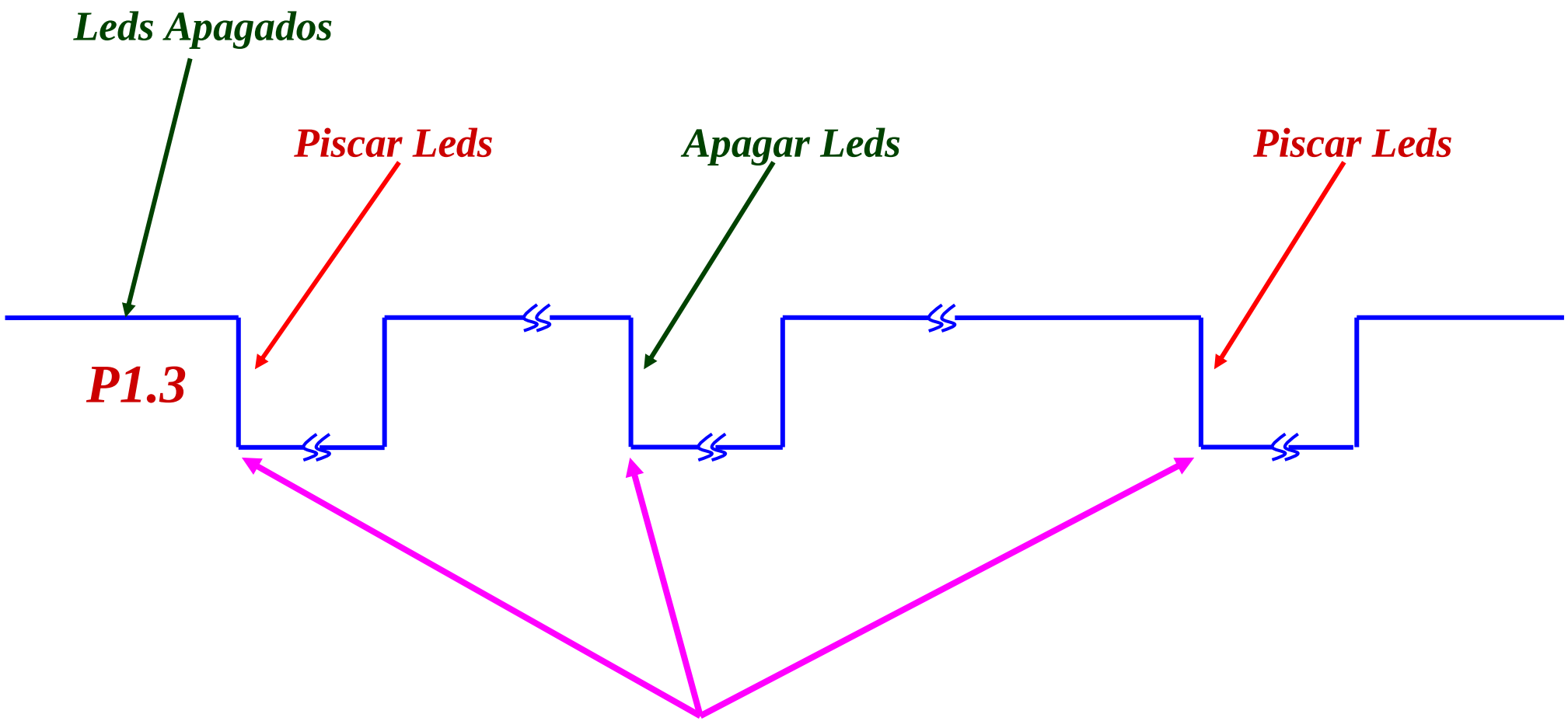
Exercício 10:

- Escrever um programa para alternar o estado dos LEDs vermelho e verde da placa MSP-EXP430G2 a cada 250ms.
- Utilizar a sub-rotina de temporização (*delay*)

- Inicialmente os LEDs deverão estar apagados;

- Sempre que a interrupção do pino *P1.3* (*Botão S2*) for ativada, o estado dos LEDs deverá alternar entre apagado e piscante;

- Configurar a interrupção do pino *P1.3* para a borda negativa.



Interrupção do pino *P1.3* ativada borda negativa.

Vetores de Interrupções do MSP430G2553

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-Up External Reset Watchdog Timer+ Flash key violation PC out-of-range(1)	PORIFG RSTIFG WDTIFG KEYV(2)	Reset	0FFFEh	31, highest
NMI Oscillator fault Flash memory access violation	NMIIFG OFIFG ACCVIFG(2)(3)	(non)-maskable (non)-maskable (non)-maskable	0FFFCh	30
Timer1_A3	TA1CCR0 CCIFG(4)	maskable	0FFFAh	29
Timer1_A3	TA1CCR2 TA1CCR1 CCIFG, TAIFG(2)(4)	maskable	0FFF8h	28
Comparator_A+	CAIFG(4)	maskable	0FFF6h	27
Watchdog Timer+	WDTIFG	maskable	0FFF4h	26
Timer0_A3	TA0CCR0 CCIFG(4)	maskable	0FFF2h	25
Timer0_A3	TA0CCR2 TA0CCR1 CCIFG, TAIFG (5)(4)	maskable	0FFF0h	24
USCI_A0/USCI_B0 receive USCI_B0 I2C status	UCA0RXIFG, UCB0RXIFG(2)(5)	maskable	0FFEEh	23
USCI_A0/USCI_B0 transmit USCI_B0 I2C receive/transmit	UCA0TXIFG, UCB0TXIFG(2)(6)	maskable	0FFECh	22
ADC10 (MSP430G2x53 only)	ADC10IFG(4)	maskable	0FFEAh	21
			0FFE8h	20
I/O Port P2 (up to eight flags)	P2IFG.0 to P2IFG.7(2)(4)	maskable	0FFE6h	19
I/O Port P1 (up to eight flags)	P1IFG.0 to P1IFG.7(2)(4)	maskable	0FFE4h	18

Interrupções das portas P1 e P2

Each pin in ports P1 and P2 have interrupt capability, configured with the PxIFG, PxIE, and PxIES registers. All P1 pins source a single interrupt vector, and all P2 pins source a different single interrupt vector. The PxIFG register can be tested to determine the source of a P1 or P2 interrupt.

Port	Register	Short Form	Address	Register Type	Initial State
P1	Input	P1IN	020h	Read only	–
	Output	P1OUT	021h	Read/write	Unchanged
	Direction	P1DIR	022h	Read/write	Reset with PUC
	Interrupt Flag	P1IFG	023h	Read/write	Reset with PUC
	Interrupt Edge Select	P1IES	024h	Read/write	Unchanged
	Interrupt Enable	P1IE	025h	Read/write	Reset with PUC
	Port Select	P1SEL	026h	Read/write	Reset with PUC
	Port Select 2	P1SEL2	041h	Read/write	Reset with PUC
	Resistor Enable	P1REN	027h	Read/write	Reset with PUC

Interrupt Enable P1IE, P2IE

Each PxIE bit enables the associated PxIFG interrupt flag.

Bit = 0: The interrupt is disabled.

Bit = 1: The interrupt is enabled.

P1IE	*x*	*x*	*x*	*x*	1	*x*	*x*	*x*
	7	6	5	4	3	2	1	0

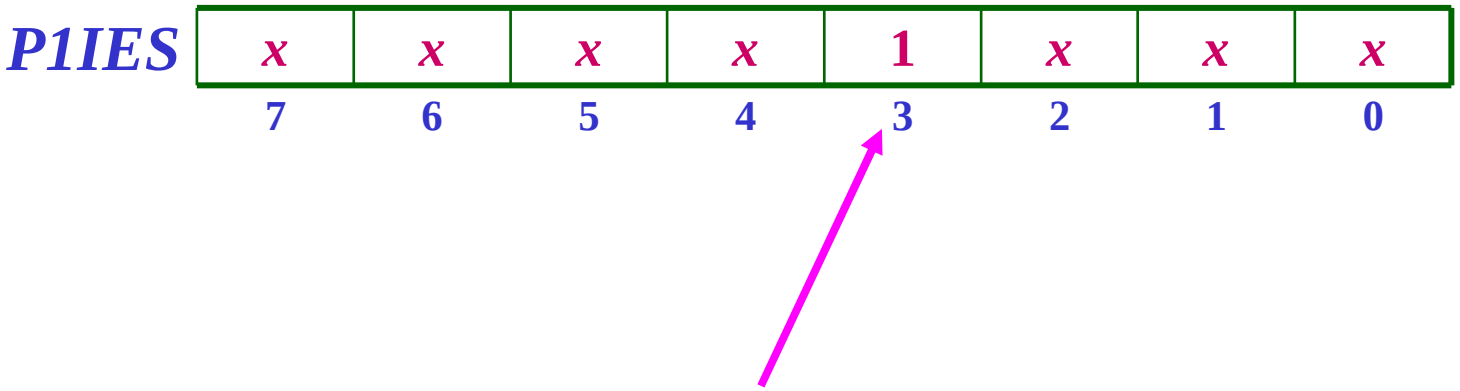
Interrupção do Pino *P1.3* habilitada

Interrupt Edge Select Registers P1IES, P2IES

Each PxIES bit selects the interrupt edge for the corresponding I/O pin.

Bit = 0: The PxIFGx flag is set with a low-to-high transition

Bit = 1: The PxIFGx flag is set with a high-to-low transition



Interrupção do pino *P1.3* ativada na borda de descida

Interrupt Flag Registers P1IFG, P2IFG

Each PxIFGx bit is the interrupt flag for its corresponding I/O pin and is set when the selected input signal edge occurs at the pin. All PxIFGx interrupt flags request an interrupt when their corresponding PxIE bit and the GIE bit are set. Each PxIFG flag must be reset with software. Software can also set each PxIFG flag, providing a way to generate a software initiated interrupt.

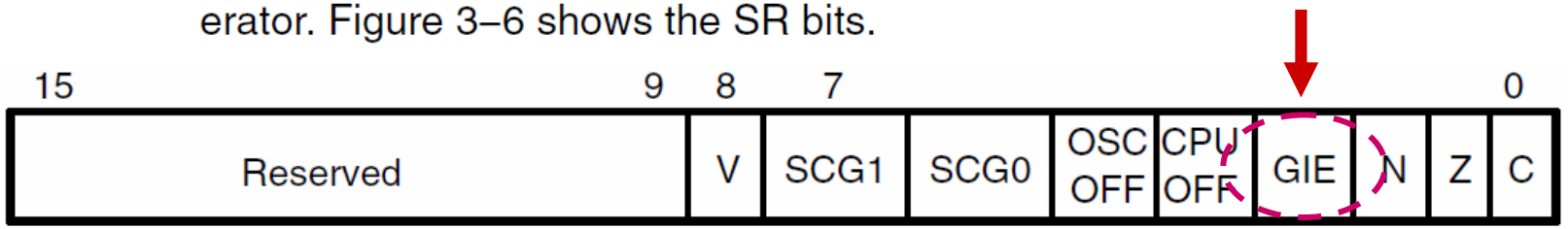
Bit = 0: No interrupt is pending

Bit = 1: An interrupt is pending

Only transitions, not static levels, cause interrupts. If any PxIFGx flag becomes set during a Px interrupt service routine, or is set after the `RETI` instruction of a Px interrupt service routine is executed, the set PxIFGx flag generates another interrupt. This ensures that each transition is acknowledged.

Status Register (SR)

The status register (SR/R2), used as a source or destination register, can be used in the register mode only addressed with word instructions. The remaining combinations of addressing modes are used to support the constant generator. Figure 3–6 shows the SR bits.



GIE General interrupt enable. This bit, when set, enables maskable interrupts. When reset, all maskable interrupts are disabled.

N Negative bit. This bit is set when the result of a byte or word operation is negative and cleared when the result is not negative.

- Word operation: N is set to the value of bit 15 of the result
- Byte operation: N is set to the value of bit 7 of the result

Z Zero bit. This bit is set when the result of a byte or word operation is 0 and cleared when the result is not 0.

C Carry bit. This bit is set when the result of a byte or word operation produced a carry and cleared when no carry occurred.

MSP430G2553.h

```
/************************************************************
 STATUS REGISTER BITS
************************************************************/
#define C                       (0x0001u)
#define Z                       (0x0002u)
#define N                       (0x0004u)
#define V                       (0x0100u)
#define GIE                     (0x0008u)
#define CPUOFF                  (0x0010u)
#define OSCOFF                  (0x0020u)
#define SCG0                    (0x0040u)
#define SCG1                    (0x0080u)
```

Habilitação das interrupções:

```
bis.w   #GIE,
SR
```

eint - Enable General Interrupts

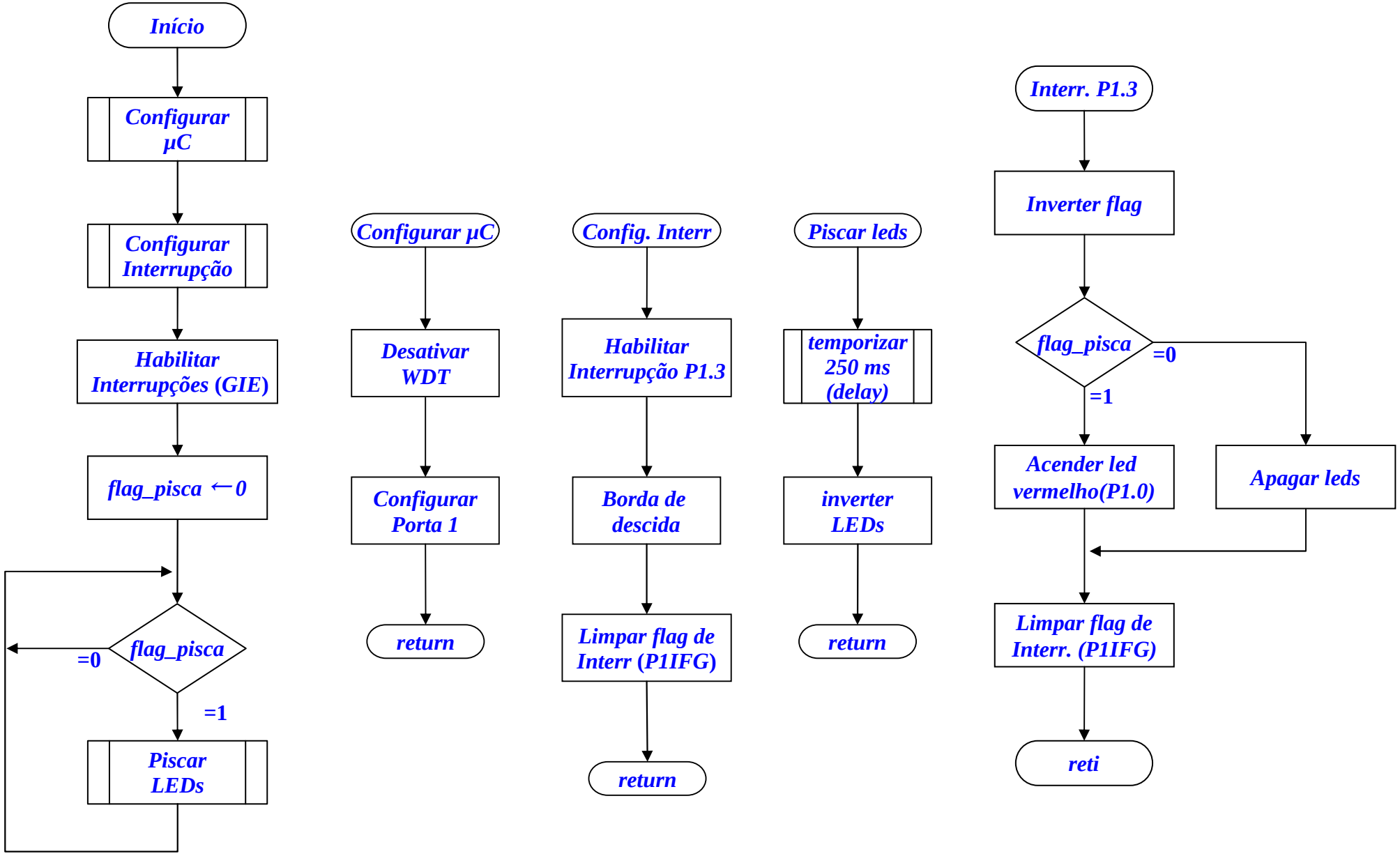
Vetor de Interrupção (Porta 1):

I/O Port P2 (up to eight flags)	P2IFG.0 to P2IFG.7 (2)(4)	maskable	0FFE6h	19
I/O Port P1 (up to eight flags)	P1IFG.0 to P1IFG.7 (2)(4)	maskable	0FFE4h	18

```
ORG    0xFFE4    (ASEG   0xFFE4)
DC16   interrupcao_P1
```

Rotina de Interrupção:

```
interrupcao_P1:
        . . .
        . . .
        . . .
        bic.b   #BIT3, &P1IFG    ; Limpar flag de interrupção
        reti
```


Início
Configurar µC
Configurar Interrupção
Habilitar Interrupções (GIE)
flag_pisca ← 0
flag_pisca
=0
=1
Piscar LEDs
Configurar µC
Desativar WDT
Configurar Porta 1
return
Config. Interr
Habilitar Interrupção P1.3
Borda de descida
Limpar flag de Interr (P1IFG)
return
Piscar leds
temporizar 250 ms (delay)
inverter LEDs
return
Interr. P1.3
Inverter flag
flag_pisca
=0
=1
Acender led vermelho(P1.0)
Apagar leds
Limpar flag de Interr. (P1IFG)
reti