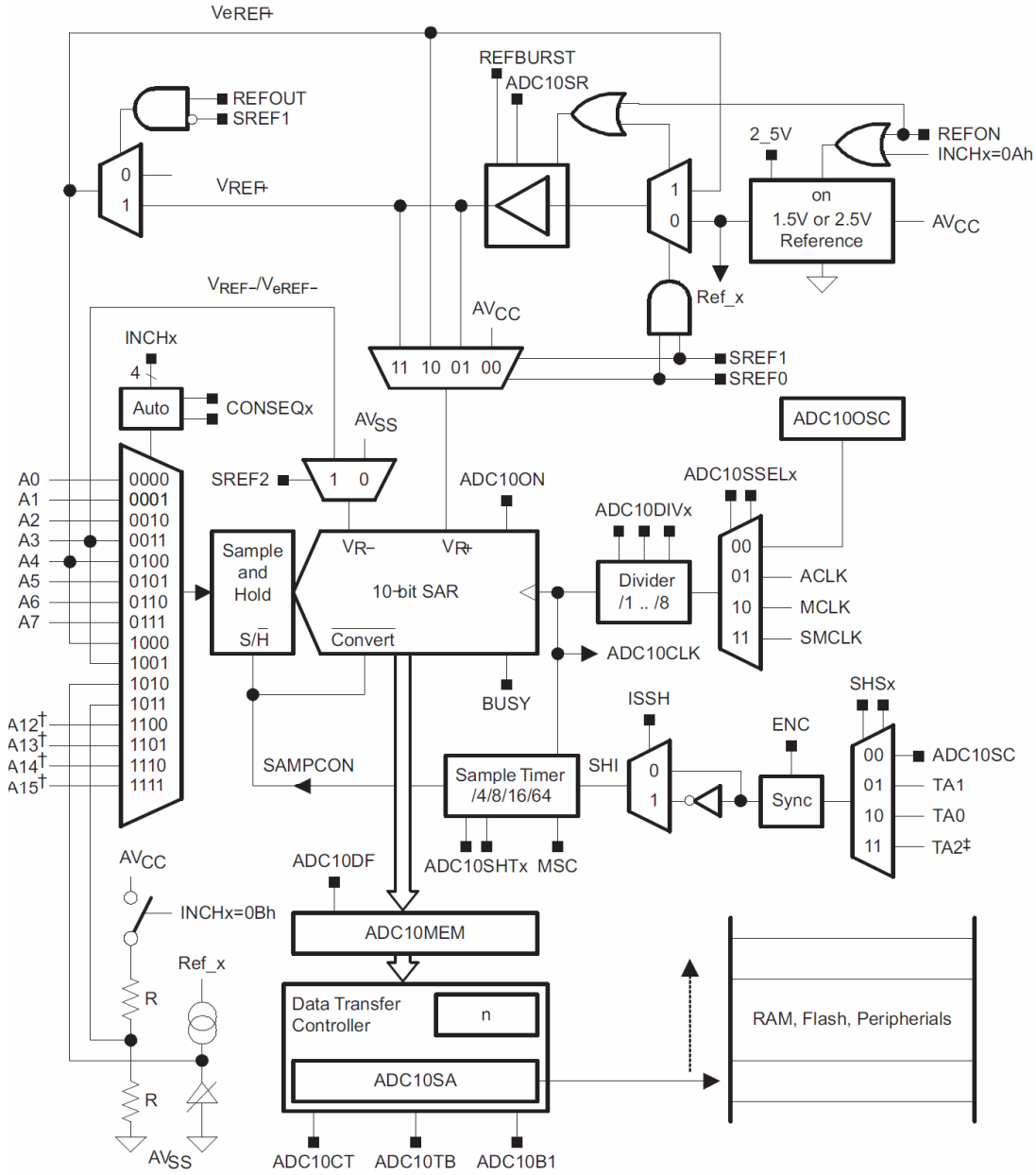
Ler o canal 5 do Conversor AD (*P1.5/A5*), com referência *AVcc*

valor *ADC* < *0x00FF*:	Apagar leds
0x00FF ≤ valor *ADC* < *0x01FF*:	Acender led Verde
0x01FF ≤ valor *ADC* < *0x02FF*:	Acender led Vermelho
0x02FF ≤ valor *ADC* :	Acender ambos os leds

Configurar o DCO para 8MHz


VeREF+
REFBURST
ADC10SR
REFOUT
SREF1
VREF+
2_5V
REFON
INCHx=0Ah
on
1.5V or 2.5V
Reference
AVCC
VREF-/VeREF-
Ref_x
INCHx
4
AVCC
11 10 01 00
SREF1
SREF0
Auto
CONSEQx
AVSS
ADC10OSC
A0
A1
A2
A3
A4
A5
A6
A7
SREF2
1 0
ADC10ON
ADC10SSELx
ADC10DIVx
0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
1010
1011
1100
1101
1110
1111
Sample
and
Hold
S/H
VR-
VR+
10-bit SAR
Convert
Divider
/1 .. /8
00
01
10
11
ACLK
MCLK
SMCLK
ADC10CLK
BUSY
ISSH
SHSx
ENC
A12†
A13†
A14†
A15†
SAMPCON
Sample Timer
/4/8/16/64
SHI
Sync
ADC10SC
TA1
TA0
TA2‡
AVCC
ADC10DF
INCHx=0Bh
ADC10SHTx
MSC
ADC10MEM
Ref_x
R
Data Transfer
Controller
n
RAM, Flash, Peripherials
ADC10SA
R
AVSS
ADC10CT
ADC10TB
ADC10B1

22.3.1 ADC10CTL0, ADC10 Control Register 0

15	14	13	12	11	10	9	8
SREFx			ADC10SHTx		ADC10SR	REFOUT	REFBURST
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)
7	6	5	4	3	2	1	0
MSC	REF2_5V	REFON	ADC10ON	ADC10IE	ADC10IFG	ENC	ADC10SC
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)

Can be modified only when ENC = 0

SREFx Bits 15-13 Select reference

000	$V_{R+} = V_{CC}$ and $V_{R-} = V_{SS}$
001	$V_{R+} = V_{REF+}$ and $V_{R-} = V_{SS}$
010	$V_{R+} = Ve_{REF+}$ and $V_{R-} = V_{SS}$
011	V_{R+} = Buffered Ve_{REF+} and $V_{R-} = V_{SS}$
100	$V_{R+} = V_{CC}$ and $V_{R-} = V_{REF-}/ V_{eREF-}$
101	$V_{R+} = V_{REF+}$ and $V_{R-} = V_{REF-}/ V_{eREF-}$
110	$V_{R+} = Ve_{REF+}$ and $V_{R-} = V_{REF-}/ V_{eREF-}$
111	V_{R+} = Buffered Ve_{REF+} and $V_{R-} = V_{REF-}/ V_{eREF-}$

ADC10SHTx Bits 12-11 ADC10 sample-and-hold time

00	4 × ADC10CLKs
01	8 × ADC10CLKs
10	16 × ADC10CLKs
11	64 × ADC10CLKs

22.3.1 ADC10CTL0, ADC10 Control Register 0

15	14	13	12	11	10	9	8
SREFx			ADC10SHTx		ADC10SR	REFOUT	REFBURST
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)
7	6	5	4	3	2	1	0
MSC	REF2_5V	REFON	ADC10ON	ADC10IE	ADC10IFG	ENC	ADC10SC
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)

Can be modified only when ENC = 0

ADC10SR Bit 10 ADC10 sampling rate. This bit selects the reference buffer drive capability for the maximum sampling rate. Setting ADC10SR reduces the current consumption of the reference buffer.

- 0 Reference buffer supports up to ~200 ksps
- 1 Reference buffer supports up to ~50 ksps

REFOUT Bit 9 Reference output

- 0 Reference output off
- 1 Reference output on

REFBURST Bit 8 Reference burst.

- 0 Reference buffer on continuously
- 1 Reference buffer on only during sample-and-conversion

MSC Bit 7 Multiple sample and conversion. Valid only for sequence or repeated modes.

- 0 The sampling requires a rising edge of the SHI signal to trigger each sample-and-conversion.
- 1 The first rising edge of the SHI signal triggers the sampling timer, but further sample-and-conversions are performed automatically as soon as the prior conversion is completed

22.3.1 ADC10CTL0, ADC10 Control Register 0

15	14	13	12	11	10	9	8
SREFx			ADC10SHTx		ADC10SR	REFOUT	REFBURST
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)
7	6	5	4	3	2	1	0
MSC	REF2_5V	REFON	ADC10ON	ADC10IE	ADC10IFG	ENC	ADC10SC
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)

Can be modified only when ENC = 0

REF2_5V Bit 6 Reference-generator voltage. REFON must also be set.
- 0 1.5 V
- 1 2.5 V

REFON Bit 5 Reference generator on
- 0 Reference off
- 1 Reference on

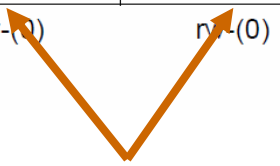
ADC10ON Bit 4 ADC10 on
- 0 ADC10 off
- 1 ADC10 on

ADC10IE Bit 3 ADC10 interrupt enable
- 0 Interrupt disabled
- 1 Interrupt enabled

22.3.1 ADC10CTL0, ADC10 Control Register 0

15	14	13	12	11	10	9	8
SREFx			**ADC10SHTx**		**ADC10SR**	**REFOUT**	**REFBURST**
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)
7	6	5	4	3	2	1	0
MSC	**REF2_5V**	**REFON**	**ADC10ON**	**ADC10IE**	**ADC10IFG**	**ENC**	**ADC10SC**
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)

Can be modified only when ENC = 0



ADC10IFG Bit 2 ADC10 interrupt flag. This bit is set if ADC10MEM is loaded with a conversion result. It is automatically reset when the interrupt request is accepted, or it may be reset by software. When using the DTC this flag is set when a block of transfers is completed.

0 No interrupt pending

1 Interrupt pending

ENC Bit 1 Enable conversion

0 ADC10 disabled

1 ADC10 enabled

ADC10SC Bit 0 Start conversion. Software-controlled sample-and-conversion start. ADC10SC and ENC may be set together with one instruction. ADC10SC is reset automatically.

0 No sample-and-conversion start

1 Start sample-and-conversion

22.3.2 ADC10CTL1, ADC10 Control Register 1

15	14	13	12	11	10	9	8
INCHx				SHSx		ADC10DF	ISSH
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)
7	6	5	4	3	2	1	0
ADC10DIVx			ADC10SSELx		CONSEQx		ADC10BUSY
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	r-0

Can be modified only when ENC = 0

INCHx Bits 15-12 Input channel select. These bits select the channel for a single-conversion or the highest channel for a sequence of conversions.

0000	A0
0001	A1
0010	A2
0011	A3
0100	A4
0101	A5
0110	A6
0111	A7
1000	V_{eREF+}
1001	V_{REF-}/V_{eREF-}
1010	Temperature sensor
1011	$(V_{CC} - V_{SS}) / 2$
1100	$(V_{CC} - V_{SS}) / 2$, A12 on MSP430x22xx devices
1101	$(V_{CC} - V_{SS}) / 2$, A13 on MSP430x22xx devices
1110	$(V_{CC} - V_{SS}) / 2$, A14 on MSP430x22xx devices
1111	$(V_{CC} - V_{SS}) / 2$, A15 on MSP430x22xx devices

22.3.2 ADC10CTL1, ADC10 Control Register 1

15	14	13	12	11	10	9	8
INCHx				SHSx		ADC10DF	ISSH
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)
7	6	5	4	3	2	1	0
ADC10DIVx			ADC10SSELx		CONSEQx		ADC10BUSY
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	r-0

Can be modified only when ENC = 0

SHSx Bits 11-10 Sample-and-hold source select

- 00 ADC10SC bit
- 01 Timer_A.OUT1
- 10 Timer_A.OUT0
- 11 Timer_A.OUT2 (Timer_A.OUT1 on MSP430x20x2 devices)

ADC10DF Bit 9 ADC10 data format

- 0 Straight binary
- 1 2s complement

ISSH Bit 8 Invert signal sample-and-hold

- 0 The sample-input signal is not inverted.
- 1 The sample-input signal is inverted.

22.3.2 ADC10CTL1, ADC10 Control Register 1

15	14	13	12	11	10	9	8
INCHx				SHSx		ADC10DF	ISSH
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)
7	6	5	4	3	2	1	0
ADC10DIVx			ADC10SSELx		CONSEQx		ADC10BUSY
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	r-0

Can be modified only when ENC = 0

ADC10DIVx Bits 7-5 ADC10 clock divider

000	/1
001	/2
010	/3
011	/4
100	/5
101	/6
110	/7
111	/8

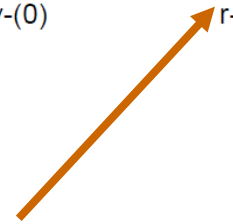
ADC10SSELx Bits 4-3 ADC10 clock source select

00	ADC10OSC
01	ACLK
10	MCLK
11	SMCLK

22.3.2 ADC10CTL1, ADC10 Control Register 1

15	14	13	12	11	10	9	8
INCHx				SHSx		ADC10DF	ISSH
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)
7	6	5	4	3	2	1	0
ADC10DIVx			ADC10SSELx		CONSEQx		ADC10BUSY
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	r-0

Can be modified only when ENC = 0



CONSEQx	Bits 2-1	Conversion sequence mode select	
		00	Single-channel-single-conversion
		01	Sequence-of-channels
		10	Repeat-single-channel
		11	Repeat-sequence-of-channels
ADC10BUSY	Bit 0	ADC10 busy. This bit indicates an active sample or conversion operation	
		0	No operation is active.
		1	A sequence, sample, or conversion is active.

22.3.3 ADC10AE0, Analog (Input) Enable Control Register 0

7	6	5	4	3	2	1	0
ADC10AE0x							
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)

ADC10AE0x	Bits 7-0	ADC10 analog enable. These bits enable the corresponding pin for analog input. BIT0 corresponds to A0, BIT1 corresponds to A1, etc. 0 Analog input disabled 1 Analog input enabled

Canal 5: *00100000*

22.3.5 ADC10MEM, Conversion-Memory Register, Binary Format

15	14	13	12	11	10	9	8
0	0	0	0	0	0	Conversion Results	
r0	r0	r0	r0	r0	r0	r	r

7	6	5	4	3	2	1	0
Conversion Results							
r	r	r	r	r	r	r	r

Conversion Results	Bits 15-0	The 10-bit conversion results are right justified, straight-binary format. Bit 9 is the MSB. Bits 15-10 are always 0.

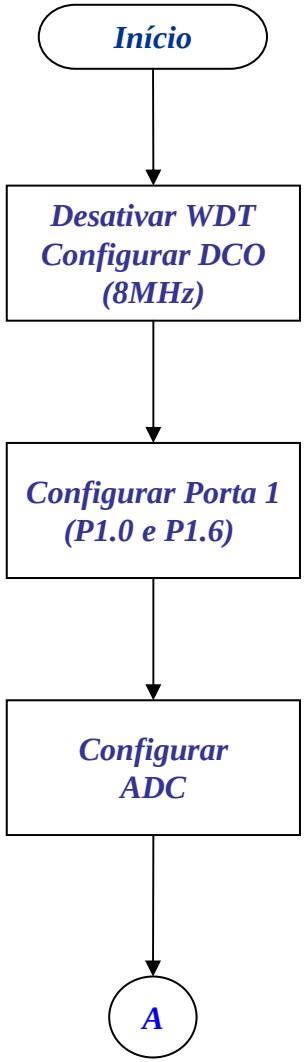
22.3.6 ADC10MEM, Conversion-Memory Register, 2s Complement Format

15	14	13	12	11	10	9	8
Conversion Results							
r	r	r	r	r	r	r	r

7	6	5	4	3	2	1	0
Conversion Results		0	0	0	0	0	0
r	r	r0	r0	r0	r0	r0	r0

Conversion Results	Bits 15-0	The 10-bit conversion results are left-justified, 2s complement format. Bit 15 is the MSB. Bits 5-0 are always 0.

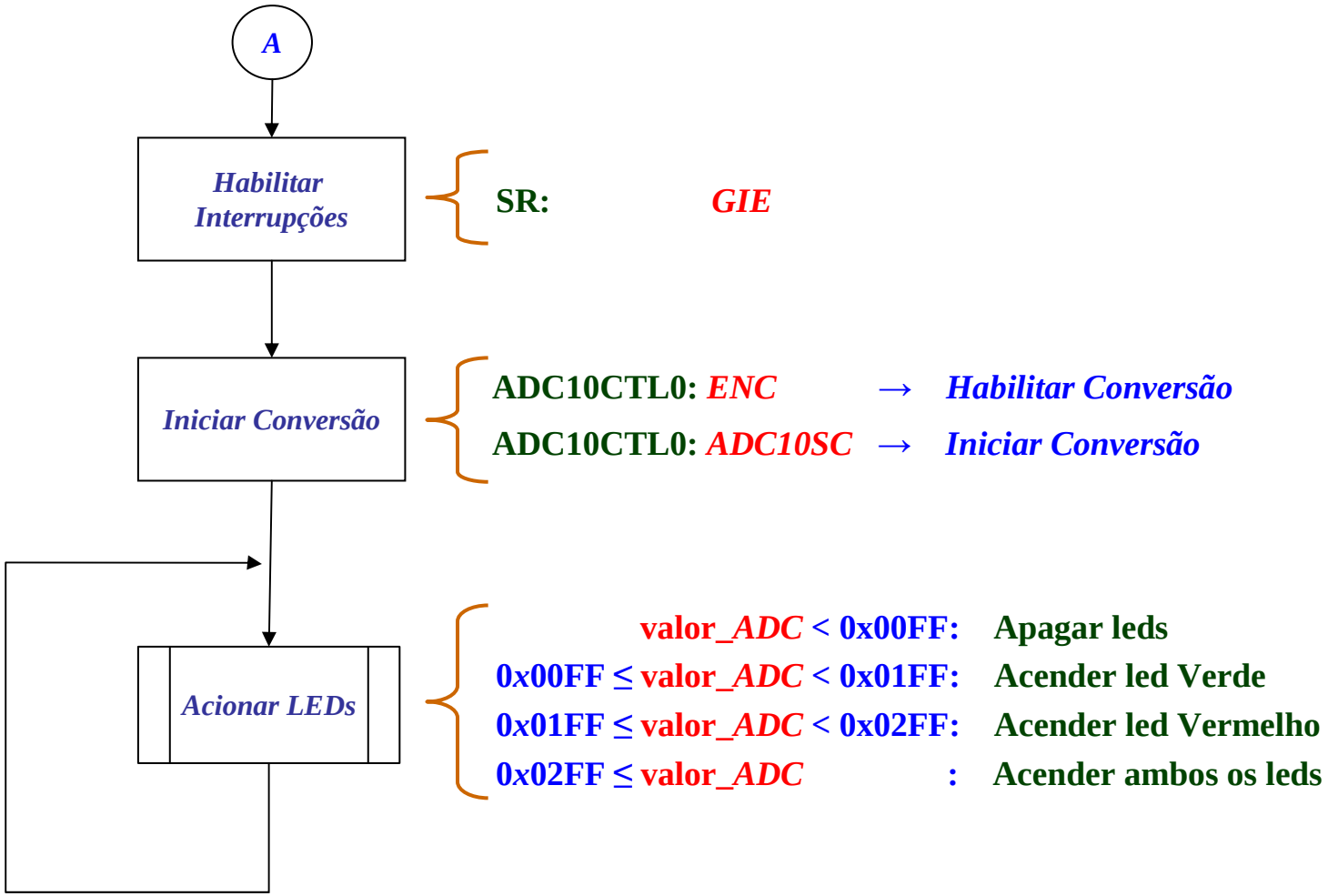
C: Exercício 21.a



WDTCTL: *WDTHOLD*
DCOCTL: *CALDCO_8MHz*
BCSCTL1: *CALBC1_8MHz*

ADC10CTL0: *SREFx* → *Ref.*: VR+ = Vcc, VR- = Vss
ADC10CTL0: *ADC10SHTx* → *Sample and Hold Time*: (16*ADC10CLKs)
ADC10CTL0: *MSC* → *Início da conversão (não automática)*
ADC10CTL0: *ADC10ON* → *ADC on*
ADC10CTL0: *ADC10IE* → *Habilita Interrupção do ADC*
ADC10CTL1: *INCHx* → *Entrada através do Canal 5 (A5)*
ADC10AE0: → *Habilita P1.5 hab. para entrada analógica*

C: Exercício 21.a



C: Exercício 21.a