Si3200 Power Offload Circuit

Introduction

This application note presents a method of offloading power dissipation from the Si3200 linefeed device and onto either an external linear regulator or an external resistor.

A design method to select the optimal voltage drop across the external power offload circuit based upon system requirements is also presented. Once the optimal external circuit voltage drop has been determined, the selection of the Zener diode in Figure 1 or the $R_{offload}$ resistors in Figure 2 is straightforward.

The solutions presented are intended for applications in which a single battery supply is available, and it is desirable to derive a lower battery voltage from this single supply to minimize power dissipation on shorter loops.

In this document, the system-supplied higher magnitude voltage is referred to as VBHI, and the derived lower magnitude voltage is referred to as VBLO. Figure 1 shows the linear regulator power offload circuit while Figure 2 shows the external resistor power offload circuit.

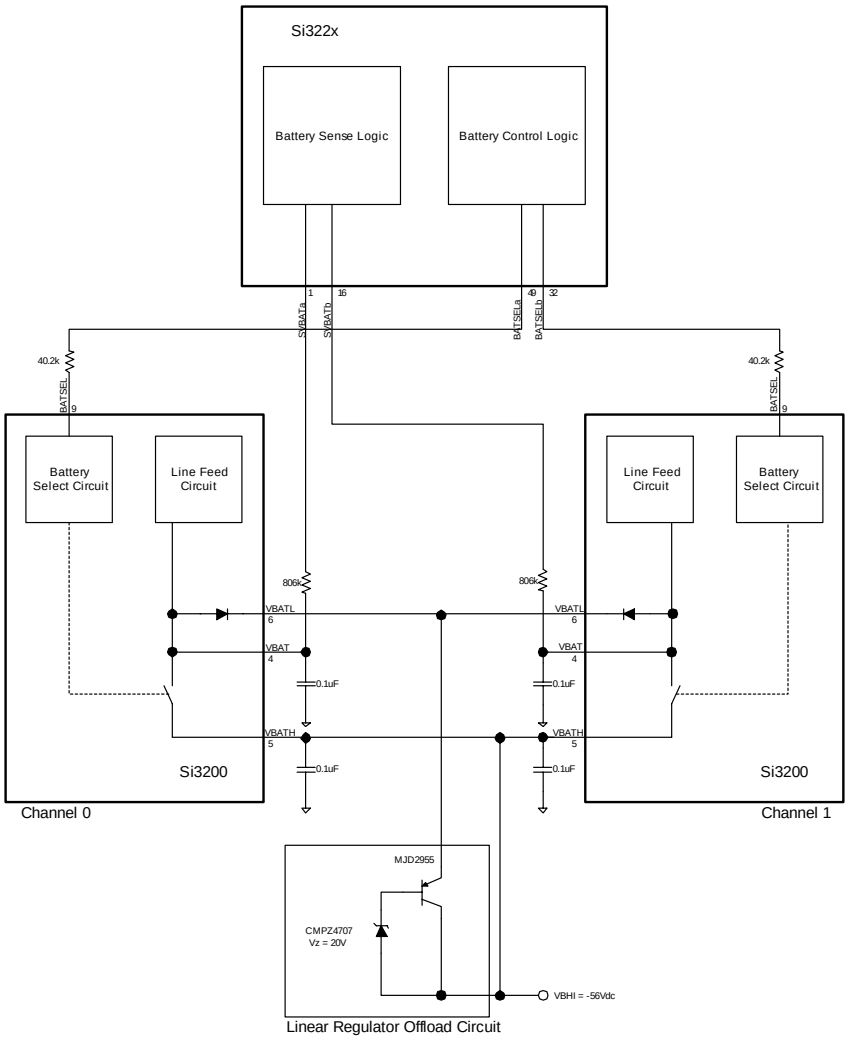

Figure 1. Linear Regulator Power Offload Circuit

Design Method

The following sections present a design method for the linear regulator and resistor power offload circuits.

System Requirements

Table 1 enumerates the system requirements that must be known to proceed with the power offload circuit design. The values for each of these parameters stem from the specific customer application and its unique requirements.

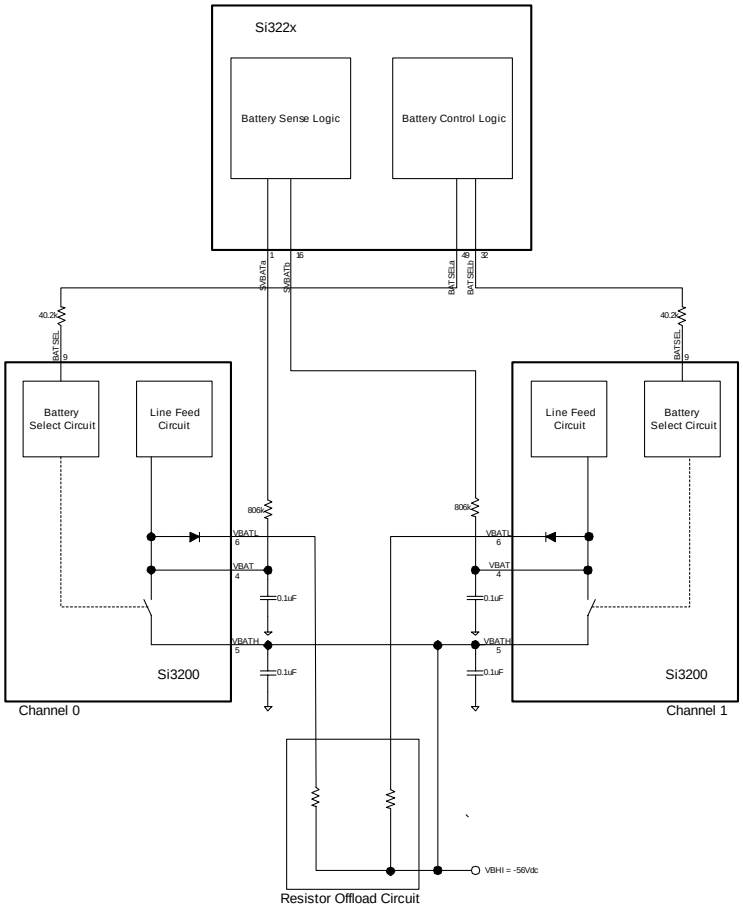

Figure 2. External Resistor Power Offload Circuit

Table 1. System Requirements

Parameter	Symbol	Units
Maximum Ambient Temperature	$T_{a\ (max)}$	°C
Loop Current (ILIM)	I_{lim}	mA
Bias Current (SBIAS)	I_{bias}	mA
Telephone dc Resistance (typ.)	R_{ph}	Ω
Maximum Loop Length	$L_{w\ (max)}$	feet/meters
Wire dc Resistance per unit length	R_w	Ω/foot or Ω/meter
Battery Supply Voltage	VBHI	Volts
Overhead Voltages (V_{CM} + V_{OV})	V_{oh}	Volts

Maximum Si3200 Power Dissipation

The maximum power dissipation for the Si3200 linefeed device is established from its specified maximum junction temperature ($T_{j(max)}$) and junction-to-ambient thermal impedance (θ_{ja}) along with the customer-supplied expected maximum ambient temperature ($T_{a(max)}$).

$$P_{d(max)} = \frac{T_{j(max)} - T_{a(max)}}{\theta_{ja}}$$

Equation 1.Maximum Power Dissipation

Table 2 provides the thermal impedance of the Si3200 device and its maximum junction temperature.

To achieve the thermal impedance (θ_{ja}) stated in Table 2, it is necessary to provide a suitably-designed PCB heat slug (copper fill) structure under the Si3200 package. The heat slug must be, as much as possible, contiguous with the system GND fill on the top circuit layer underneath the Si3200 package. The heat slug should be connected with a row of eight vias that are at least 10 mils (~0.25 mm) in diameter to inner PCB circuit layers, such as the ground plane layer, and to the bottom circuit side GND fill. The Si3220DC-EVB Rev. 2 evaluation board layout from Silicon Laboratories provides an example of a suitable heat slug design for the Si3200.

Table 2. Si3200 Thermal Parameters

Parameter	Value	Units
θ_{ja}	55	°C/Watt
$T_{j(max)}$	140	°C

The primary objective of the power offload circuit is to ensure that the power dissipation in the Si3200 device will remain under $P_{d(max)}$ at up to the maximum required ambient temperature under the required operating conditions of loop length, battery voltage, loop current, and bias current.

Optimal VBLO Determination

The power dissipation in the Si3200 device, during the forward/reverse active off-hook state is obtained from Equation 2 below.

$$P_{Si3200} = (I_{LIM} + I_{BIAS}) \times V_{BAT} - (R_w \times L_w + R_{ph}) \times I_{LIM}^2$$

Equation 2.Power Dissipated in Si3200 Linefeed

where:

P_{Si3200} is the power dissipated in the Si3200 in watts.

I_{lim} is the required off-hook loop current as set by the ILIM register in amps.

I_{bias} is the required bias current as set by the ABIAS field in the SBIAS register in amps.

V_{BAT} is the battery voltage (may be set to VBHI or VBLO, depending on loop length) in volts.

R_w is the resistance per linear foot (or linear meter) of the wire (e.g., 24AWG or 26AWG wire).

L_w is the loop length in feet or meters.

R_{ph} is the off-hook dc resistance of the telephone.

V_{BAT} may be either VBHI or VBLO depending on which battery voltage the Si3200 is using. The Si322x devices feature automatic battery selection, which is based upon the measurement of the dc voltage present on the RING terminal. "Battery Switching Threshold Settings," on page 5 describes a method for selecting the correct value for the BATHTH, BATLTH, and BATLPF RAM locations, which control the voltage thresholds at which the system will switch battery voltage and the filtering of the RING dc signal. These RAM locations must be programmed with the correct values that optimize the switching point between VBHI and VBLO.

When the system is using the lower battery voltage (VBLO), the worst-case power dissipation in the Si3200 occurs when the loop length is zero. If the loop length is zero, the R_w x L_w term in Equation 2 vanishes resulting in Equation 3 .

$$P_{Si3200} = (I_{LIM} + I_{BIAS}) \times V_{BAT} - R_{ph} \times I_{LIM}^2$$

Equation 3.Power Dissipated in the Si3200 (at zero loop length)

Replacing P_{Si3200} in Equation 3 with $P_{d(max)}$ and V_{BAT} with VBLO, an expression for VBLO is obtained as shown in Equation 4.

$$VBLO = \frac{P_{d(max)} + R_{ph} \times I_{LIM}^2}{I_{LIM} + I_{BIAS}}$$

Equation 4.VBLO

Equation 4 yields the low battery voltage (VBLO) at which the power dissipation in the Si3200 will equal $P_{d(max)}$ at zero loop length. Actually, it is desired to have P_{Si3200} under $P_{d(max)}$ by some margin. Hence, Equation 4 is modified to include a factor to scale $P_{d(max)}$ to provide margin, resulting in Equation 5. For example, let k = 0.80 so that power dissipation in the Si3200 will be at 80% of $P_{d(max)}$ when operating from VBLO on a zero

loop length line.

$$VBLO = \frac{k \times P_{d(max)} + R_{ph} \times I_{LIM}^2}{I_{LIM} + I_{BIAS}}$$

Equation 5.VBLO (with margin factor)

The selection of VBLO may require several iterations in order to derive the optimal solution that ensures power dissipation in both the Si3200 and the offload circuit under all operating conditions. The “Power Offload Tool” section of this document describes a Power Offload Calculation tool to facilitate the iterative process to determine the optimal VBLO.

Power Offload Circuit Component Selection

Once the optimal VBLO has been determined, it is a simple matter to determine the resistor value needed for the resistive power offload circuit or the Zener diode voltage for the linear regulator offload circuit.

Resistive Offload Circuit

The value of the resistor used in the resistive offload circuit is readily computed from Equation 6.

$$R_{offload} = \frac{|VBHI| - |VBLO|}{I_{LIM} + I_{BIAS}}$$

Equation 6.Offload Resistor Calculation

Choose the standard 5% resistor value nearest to the calculated $R_{offload}$ value.

The power dissipation in the offload resistor is obtained from Equation 7:

$$P_{offload} = R_{offload} \times (I_{LIM} + I_{BIAS})^2$$

Equation 7.Resistor Power Dissipation

Choose a resistor power rating that can accommodate $P_{offload}$ plus an adequate margin.

Linear Regulator Offload Circuit

The nominal Zener diode voltage is obtained from VBLO, and the typical V_{be} voltage drop in a bipolar transistor.

$$V_z = |VBHI| - |VBLO| - 0.6V$$

Equation 8.Zener Voltage

Choose a 5% Zener diode with nominal Zener voltage (Vz) as close as possible to the value determined by Equation 8. Zener diodes in SOT23 packages are typically rated at 350 mW, which is ample power dissipation capacity for this application.

The power dissipated in the transistor used in the linear regulator is obtained using Equation 9 (with both channels simultaneously off-hook – hence the 2x factor in Equation 9). The designer must ensure that the selected transistor and its corresponding PCB footprint can adequately handle the power dissipated with some margin while taking into consideration the manufacturer’s rated $P_{d(max)}$ and its corresponding derating as ambient temperature increases. For most applications, a PNP transistor, such as the ON Semiconductor, MJD2955, in a DPAK package or equivalent, is well suited for this application, provided that a suitable PCB heat slug (copper fill) is designed under the transistor package. (See "Typical Design Example," on page 6).

$$P_Q = 2 \times (|VBHI| - |VBLO|) \times (I_{LIM} + I_{BIAS})$$

Equation 9.Transistor Power Dissipation

Equation 10 provides the worst-case power dissipation in the Zener diode based on the rated Zener voltage and the rated minimum current gain (β_{min}) of the transistor for the case when both channels are simultaneously off-hook. The Central Semiconductor CMPZ4678-CMPZ4717 Zener diode family in an SOT-23 package provides adequate power dissipating margin. (See "Typical Design Example," on page 6).

$$P_Z = 2 \times V_Z \times \frac{I_{LIM} + I_{BIAS}}{\beta_{min}}$$

Equation 10.Zener Diode Power Dissipation

Thermal Considerations

The system designer must carefully consider the PCB placement of the offload resistor or the linear regulator so as to optimize system heat dissipation. The offload circuit (resistor or linear regulator) is not electrically required to be placed close to pin 6 (VBATL) of the Si3200 and should therefore be placed up to two inches (approximately 5 cm) away from the Si3200 device, thus, physically separating components that are dissipating appreciable power.

To minimize the resistor cost, the offload resistors can be through-hole instead of SMT. To further spread heat dissipation and reduce the power rating of the individual resistors, the offload resistors can be split into two or more equal-value resistors whose parallel combination forms the desired $R_{offload}$ value.

In the case of the linear regulator, the system designer must consider the manufacturer's rated maximum power dissipation of the Zener diode and transistor and ensure that these ratings are not exceeded under all expected operating conditions. The manufacturer's recommended PCB footprint for the Zener diode and transistor must be followed to ensure proper heat dissipation.

As with any line card system design, the designer must take into consideration proper ventilation and airflow to carry heat away from power-dissipating components in the system and to ensure that the maximum allowable ambient temperature within the system enclosure is not exceeded under all expected operating conditions.

Battery Switching Threshold Settings

The Si322x device provides two threshold registers that allow software to select the thresholds at which the system switches battery supply. Two thresholds are used to provide hysteresis. The value of the BATHTH RAM location determines the RING dc voltage at which the system switches from VBLO to VBHI upon going on-hook. The value of BATLTH determines the RING dc voltage at which the system switches from VBHI to VBLO upon going off-hook.

The value of BATLPF determines corner frequency of the digital low-pass filter used to filter the RING dc voltage for the purposes of comparing against the set thresholds.

For a given loop condition, the SLIC must be able to supply enough voltage to the loop (V_{tr}) in the off-hook state, and maintain the required overhead voltage ($V_{oh} = V_{cm} + V_{ov}$). This requirement is expressed in Equation 11 (see "DC Feed Characteristics" in the Si3220/Si3225 Data Sheet for a more detailed explanation of V_{OV} and V_{CM}.)

$$VBAT \geq V_{tr} + V_{CM} + V_{OV}$$

Equation 11.Battery Voltage Requirement

V_{tr} is the product of ILIM and the total dc resistance of the loop, as shown in Equation 12.

$$V_{tr} = I_{LIM} \times (R_w \times L_w + R_{ph})$$

Equation 12.TIP-RING Voltage

The optimal battery-switching threshold is selected based upon the ability of VBLO to satisfy Equation 11. So long as VBLO is able to satisfy the requirement in Equation 11, the VBLO battery source must be selected. When VBLO can no longer satisfy Equation 11, VBHI must be selected.

Since the battery switching mechanism monitors the dc voltage at the RING terminal (TIP in reverse active mode), and the RING voltage with respect to system GND already includes V_{CM}, the switching threshold is obtained from Equation 13.

$$V_{thres} = |VBLO| - V_{OV}$$

Equation 13.Battery Switching Threshold Voltage

The RAM locations, BATHTH and BATLTH, can assume any value in the range from 0 to 160.2 in Volts. One LSB of BATHTH or BATLTH is 628 mV. The values for BATHTH and BATLTH occupy bits 7 through 14 in their corresponding RAM locations and must be shifted up by 7 bit positions, hence the multiplication by 2^7 in Equations 14 and 15.

Equations 14 and 15 provide a means of calculating BATHTH and BATLTH, which provides for two LSBs of hysteresis (2 x 0.628 = 1.256V).

$$BATLTH = 2^7 \times DEC2HEX\left(\frac{V_{thres}}{0.628} + 1\right)$$

Equation 14.BATHTH

$$BATHTH = 2^7 \times DEC2HEX\left(\frac{V_{thres}}{0.628} - 1\right)$$

Equation 15.BATLTH

The value of BATLPF is obtained from Equation 16, where f is the desired cut-off frequency for the low-pass filter. BATLPF occupies bits 3 through 15 and must be shifted up 3 bit positions, hence the multiply by 2^3 in Equation 16. Typically, f is set to 10 Hz, which yields BATLPF = 0xA10.

$$BATLPF = 2^3 \times DEC2HEX\left(\frac{2 \times \pi \times f \times 4096}{800}\right)$$

Equation 16.BATLPF

Power Offload Tool

This application note is bundled with an Excel file titled "Si3200_power_calc.xls".

The bundled Excel file provides a very useful tool for analyzing the power dissipation of the Si3200 as a function of loop length and other user-entered parameters. The user enters the desired values for the various parameters at the top of the worksheet and the

worksheet calculates and displays the power limit for the Si3200 and the power dissipated in the Si3200 as a function of loop length. The worksheet also takes care of calculating the battery switching voltage threshold between VBLO and VBHI so that the displayed power dissipation takes into consideration which is the applicable battery supply (VBLO or VBHI), depending on loop length.

The Si3200_power_calc.xls file should be used to fine tune the optimal low battery voltage (VBLO) such that the power dissipation in the Si3200 will remain under $P_{d(max)}$ for all applicable loop lengths.

Step-by-Step Procedure

Perform the following steps:

1. Determine the value of all parameters required in Table 1.
2. Using the application's required maximum ambient temperature, calculate the maximum allowable power dissipation for the Si3200 (Equation 1).
3. Calculate the optimal VBLO using Equation 5 initially using k = 0.80. To arrive at the optimal value for VBLO, it may be necessary to perform several iterations while using the Power Calculation Tool until a value of VBLO that results in $P_{Si3200} < P_{d(max)}$ for all loop lengths is obtained.
4. Determine the appropriate resistor value (Equations 6 and 7) or select the appropriate Zener diode and transistor (Equations 8, 9, and 10). Verify the power dissipation in the transistor and Zener diode and corresponding thermal management.
5. Calculate the correct values for BATHTH, BATLTH and BATLPF using Equations 13, 14, 15, and 16.

Typical Design Example

Perform the following steps:

1. Determine The value of all parameters required in Table 1. An application has the requirements shown in Table 3:

Table 3. System Requirements

Parameter	Symbol	Value	Units
Maximum Ambient Temperature	Ta (max)	85	°C
Loop Current (ILIM)	I_{lim}	20.625	mA
Bias Current (SBIAS)	I_{bias}	4	mA
Telephone DC Resistance (typ)	R_{ph}	200	Ω
Maximum Loop Length	$L_{w\ (max)}$	18000	ft
Wire Resistance per Foot	R_w	0.09	Ω/foot
Battery Supply Voltage	VBHI	–56	V
Overhead Voltages ($V_{CM} + V_{OV}$)	V_{oh}	7	V

2. Using the application's required maximum ambient temperature, calculate the maximum allowable power dissipation for the Si3200 (Equation 1):

$P_{d(max)}$ = (140 °C – 85 °C) / 85 °C/W = 1 W

3. Calculate the optimal VBLO using Equation 5 and k = 0.80 (20% margin).

VBLO = (0.80 x 1 + 200 x 0.020625^2) / (0.020625 + 0.004) = 35.94 V (round to 36 V)

Use the Power Calculation Tool to verify the value of VBLO = –36 V satisfies P_{Si3200} < Pd(max) for all required loop lengths:

The Si3200 Power Calculation Tool yields the result shown in Figure 3, which is clearly acceptable as the power dissipation for the Si3200 remains well under 1 W as required for an ambient temperature of 85 °C.

The discontinuity in the P_{Si3200} line of Figure 3 corresponds to the point at which battery switching occurs. Below approximately 13500 feet, VBLO is used, and for longer loop lengths, VBHI is used. Note that the maximum power for the VBLO segment, which occurs at zero loop length, is approximately equal to the maximum power for the VBHI segment. When using the Power Calculation Tool, it is desirable to equalize these two peak powers by optimizing the value of the derived VBLO.

4. Determine the appropriate resistor value (Equations 6 and 7) or select the appropriate Zener diode and transistor (Equations 8, 9, and 10):

For resistive offload:

$R_{offload}$ = (56 V – 36 V) / 24.625 mA = 812 Ω (nearest standard 5% value is 820 Ω).

$P_{offload}$ = 820 Ω x $(24.625\ mA)^2$ = 497mW

(choose 0.75 W or 1 W resistor – typically in a 2010 package size for SMT or use a through-hole resistor)

For Linear Regulator offload:

Vz = |–56 V| – |–36 V| – 0.6 V = 19.4 V

(choose 19 V or 20 V 5% Zener diode).

Figure 1 depicts the ON Semiconductor MJD2955 (DPAK) transistor and Central Semiconductor CMPZ4707 (SOT-23) 20 V Zener diode, which are well suited for the constraints of this example. The MJD2955 transistor, when installed on the manufacturer's recommended minimum PCB pad size, provides $P_{d(max)}$ = 1.75 W at 25 °C and derates by 0.014 W/°C at ambient temperatures above 25 °C. Thus, at Ta = 85°C, the transistor with its minimum specified PCB pad is rated at 1.75 W – 0.014 W/°C x (85 °C – 25 °C) = 0.91 W.

The following equation gives the expected off-hook transistor power dissipation:

$P_Q = 2 \times (56V - 36V) \times (0.020625A + 0.004A) = 0.985W$

The nominal operating point for the transistor (V_{CE} = 20 V, I_C = 49.25 mA) is well within the "Maximum Forward Bias Safe Operating Area" given by the transistor manufacturer, which typically assumes that the transistor is mounted on an "infinite" heat sink (T_c = 25 °C).

However, P_Q exceeds the transistor's derated $P_{d(max)}$ of 0.91 W at 85 °C, which is based on the minimum pad size shown in the manufacturer's data sheet. Therefore, the pad size for the transistor must be increased from the minimum size recommended by the transistor manufacturer in order to ensure that the transistor's junction temperature will remain below 150 °C when operating at Ta = 85 °C and while dissipating the nominal 985 mW plus a reasonable safety margin.

For the MJD2955 transistor, heat is primarily dissipated via the paddle of the DPAK package, which is electrically connected to the collector. The minimum pad size recommended by the manufacturer for the paddle is 4.826 mm x 4.191 mm, which yields θ_{ja} = 71.4 °C/W. This minimum collector pad size must be enhanced sufficiently to provide enough heat dissipation in order to reduce the resulting θ_{ja} below 60 °C/W (i.e. $\theta_{ja(max)} = (T_{j(max)} - T_{a(max)}) / P_{d(max)}$ = (150 °C – 85 °C) / 0.985 W = 66 °C; use 60 °C/W for added margin). Generally, the effective θ_{ja} will be reduced by increasing the size of PCB heat slug pad for the transistor paddle and/or by tying the PCB component-side heat slug copper pad to copper fill on other PCB layers using multiple vias.

The final PCB heat slug design must be verified by measuring the actual θ_{ja} and verifying it is 60 °C/W or less.

The following equation gives the worst-case Zener diode power dissipation:

$P_Z = 2 \times 20 V \times (0.020625 A + 0.004 A) / 20 = 0.050 W$

The diode manufacturer's data sheet states a rating of $T_{j(max)}$ = 150 °C and $P_{d(max)}$ = 350 mW @ 25 °C. The estimated thermal resistance of a Zener diode in an SOT-23 package is 500 °C/W.

The junction temperature of the diode can be estimated as: $T_j = \theta_{ja} \times P_d + T_a$, which yields:

Tj = 500 °C/W x 0.050 W + 85 °C = 110 °C

which is well below T_j(max) = 150 °C.

5. Calculate the correct values for BATHTH, BATLTH, and BATLPF using Equations 13, 14, 15, and 16:

V_{thres} = 36 V – 4 V = 32 V

BATHTH = 2^7 x DEC2HEX ((32V/0.628 V) + 1) = 0x1A00

BATLTH = 2^7 x DEC2HEX ((32V/0.628 V) – 1) = 0x1900

BATHLPF = 2^3 x DEC2HEX ((2 x 3.14159 x 10 x 4096) / 800) = 0xA10

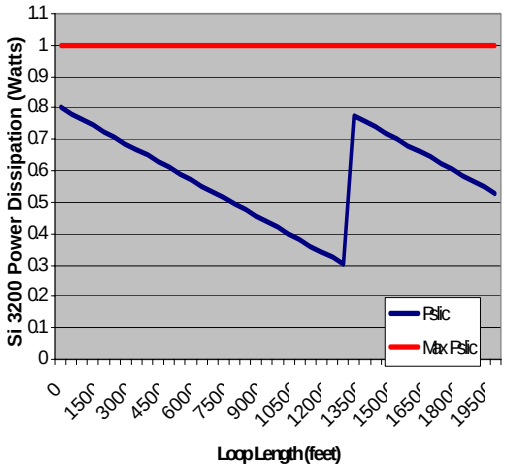

Figure 3. Si3200 Power Calculation (example)

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