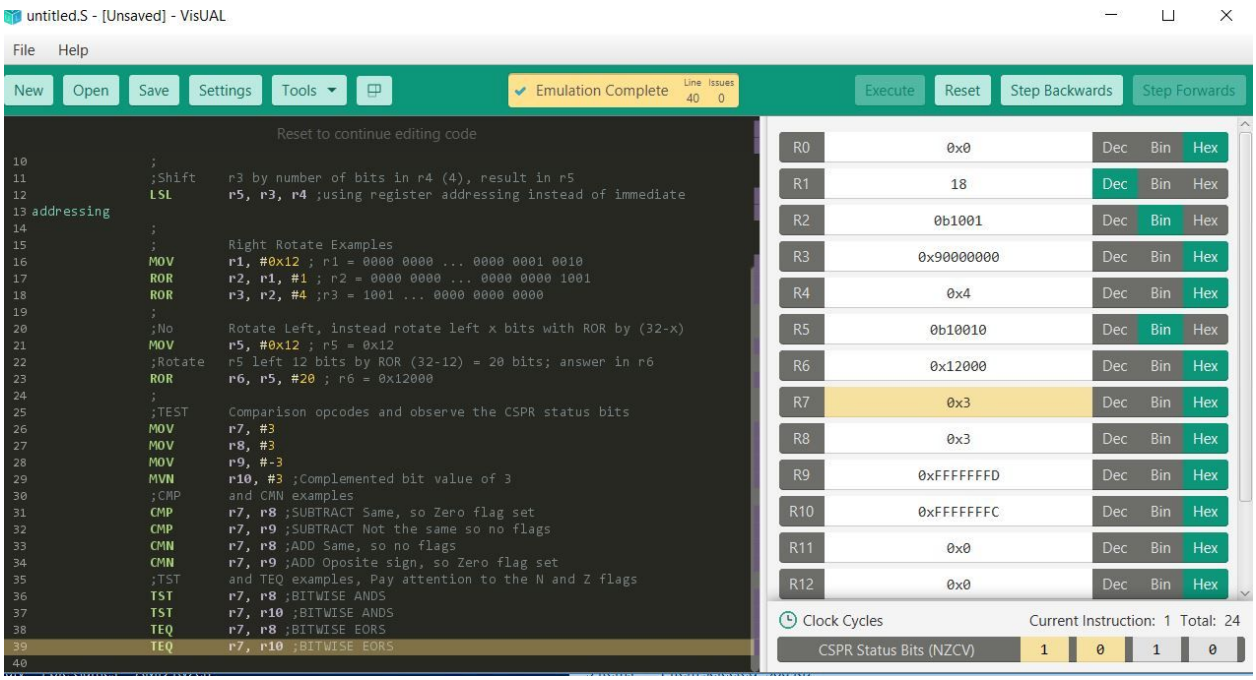
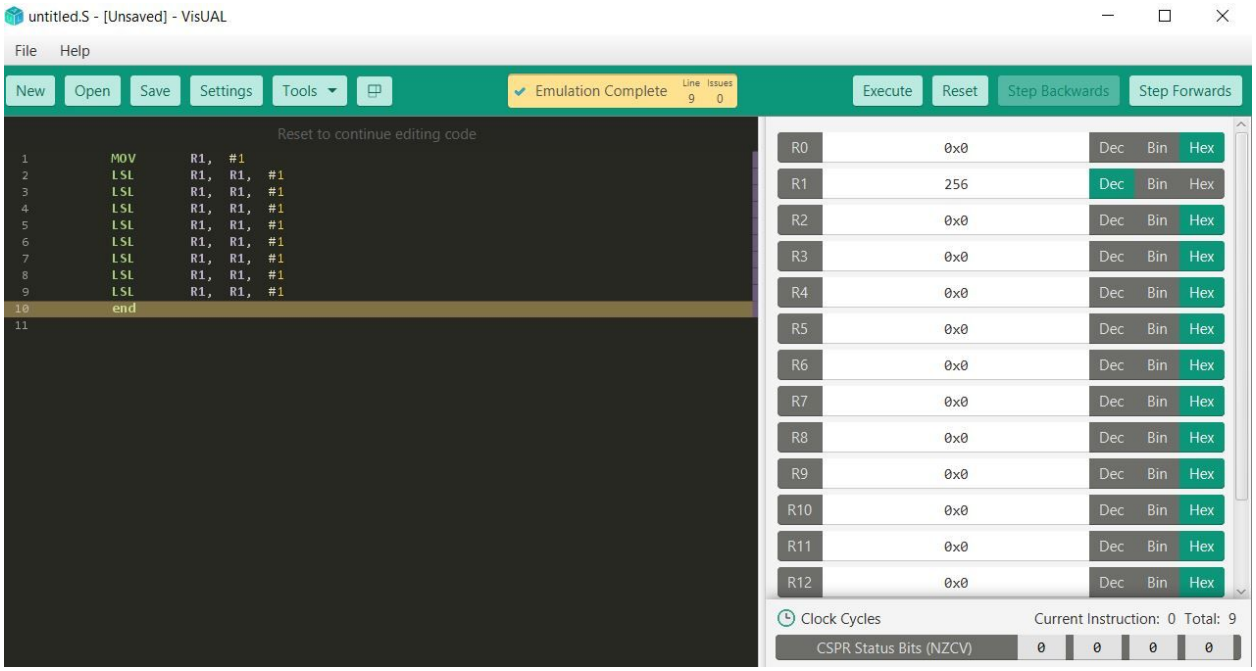
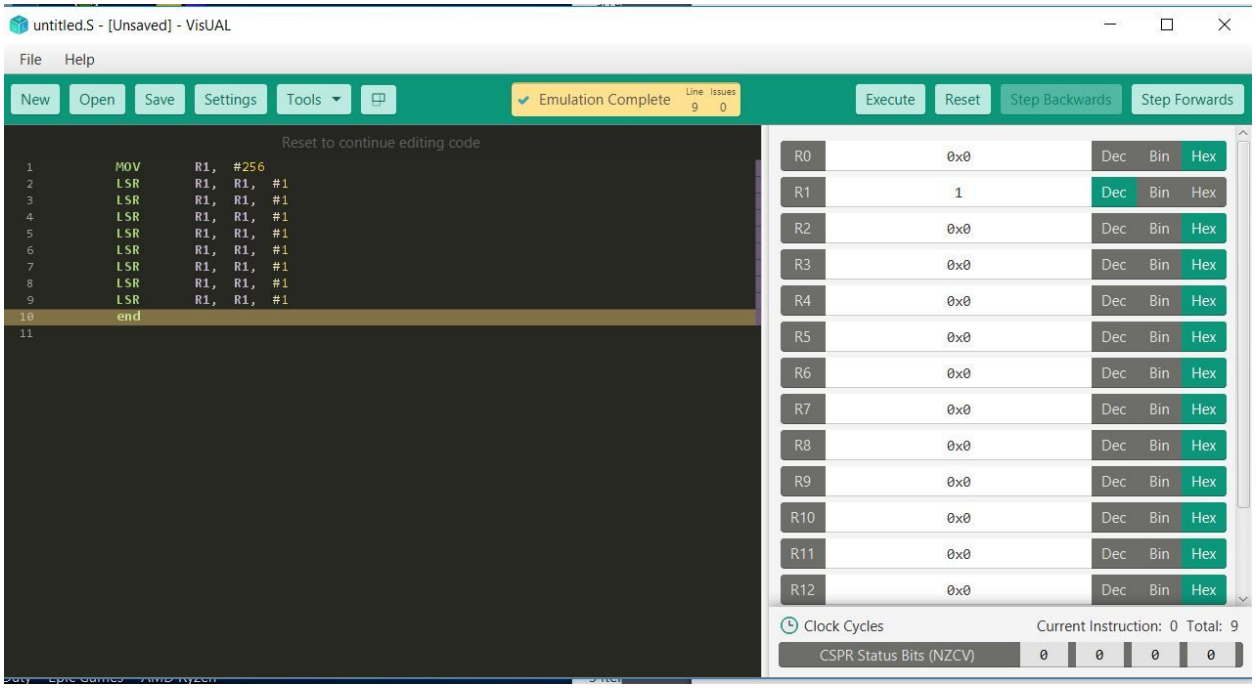
Part 1:


untitled.S - [Unsaved] - VisUAL
File Help
New Open Save Settings Tools
Emulation Complete Line 40 Issues 0
Execute Reset Step Backwards Step Forwards
Reset to continue editing code
; ;Shift r3 by number of bits in r4 (4), result in r5
LSL r5, r3, r4 ;using register addressing instead of immediate
addressing
; ; Right Rotate Examples
MOV r1, #0x12 ; r1 = 0000 0000 ... 0000 0001 0010
ROR r2, r1, #1 ; r2 = 0000 0000 ... 0000 0000 1001
ROR r3, r2, #4 ;r3 = 1001 ... 0000 0000 0000
; ;No Rotate Left, instead rotate left x bits with ROR by (32-x)
MOV r5, #0x12 ; r5 = 0x12
;Rotate r5 left 12 bits by ROR (32-12) = 20 bits; answer in r6
ROR r6, r5, #20 ; r6 = 0x12000
; ;TEST Comparison opcodes and observe the CSPR status bits
MOV r7, #3
MOV r8, #3
MOV r9, #-3
MVN r10, #3 ;Complemented bit value of 3
;CMP and CMN examples
CMP r7, r8 ;SUBTRACT Same, so Zero flag set
CMP r7, r9 ;SUBTRACT Not the same so no flags
CMN r7, r8 ;ADD Same, so no flags
CMN r7, r9 ;ADD Oposite sign, so Zero flag set
;TST and TEQ examples, Pay attention to the N and Z flags
TST r7, r8 ;BITWISE ANDS
TST r7, r10 ;BITWISE ANDS
TEQ r7, r8 ;BITWISE EORS
TEQ r7, r10 ;BITWISE EORS
R0 0x0 Dec Bin Hex
R1 18 Dec Bin Hex
R2 0b1001 Dec Bin Hex
R3 0x90000000 Dec Bin Hex
R4 0x4 Dec Bin Hex
R5 0b10010 Dec Bin Hex
R6 0x12000 Dec Bin Hex
R7 0x3 Dec Bin Hex
R8 0x3 Dec Bin Hex
R9 0xFFFFFFFD Dec Bin Hex
R10 0xFFFFFFFC Dec Bin Hex
R11 0x0 Dec Bin Hex
R12 0x0 Dec Bin Hex
Clock Cycles Current Instruction: 1 Total: 24
CSPR Status Bits (NZCV) 1 0 1 0

Part 2:


untitled.S - [Unsaved] - VisUAL
File Help
New Open Save Settings Tools
Emulation Complete Line 9 Issues 0
Execute Reset Step Backwards Step Forwards
Reset to continue editing code
MOV R1, #1
LSL R1, R1, #1
LSL R1, R1, #1
LSL R1, R1, #1
LSL R1, R1, #1
LSL R1, R1, #1
LSL R1, R1, #1
LSL R1, R1, #1
LSL R1, R1, #1
end
R0 0x0 Dec Bin Hex
R1 256 Dec Bin Hex
R2 0x0 Dec Bin Hex
R3 0x0 Dec Bin Hex
R4 0x0 Dec Bin Hex
R5 0x0 Dec Bin Hex
R6 0x0 Dec Bin Hex
R7 0x0 Dec Bin Hex
R8 0x0 Dec Bin Hex
R9 0x0 Dec Bin Hex
R10 0x0 Dec Bin Hex
R11 0x0 Dec Bin Hex
R12 0x0 Dec Bin Hex
Clock Cycles Current Instruction: 0 Total: 9
CSPR Status Bits (NZCV) 0 0 0 0

Part 3:


untitled.S - [Unsaved] - VisUAL
File
Help
New
Open
Save
Settings
Tools
Emulation Complete
Line 9
Issues 0
Execute
Reset
Step Backwards
Step Forwards
Reset to continue editing code
1 MOV R1, #256
2 LSR R1, R1, #1
3 LSR R1, R1, #1
4 LSR R1, R1, #1
5 LSR R1, R1, #1
6 LSR R1, R1, #1
7 LSR R1, R1, #1
8 LSR R1, R1, #1
9 LSR R1, R1, #1
10 end
11
R0 0x0 Dec Bin Hex
R1 1 Dec Bin Hex
R2 0x0 Dec Bin Hex
R3 0x0 Dec Bin Hex
R4 0x0 Dec Bin Hex
R5 0x0 Dec Bin Hex
R6 0x0 Dec Bin Hex
R7 0x0 Dec Bin Hex
R8 0x0 Dec Bin Hex
R9 0x0 Dec Bin Hex
R10 0x0 Dec Bin Hex
R11 0x0 Dec Bin Hex
R12 0x0 Dec Bin Hex
Clock Cycles
Current Instruction: 0 Total: 9
CSPR Status Bits (NZCV) 0 0 0 0