Low Power High Performance 2.4 GHz GFSK Transceiver

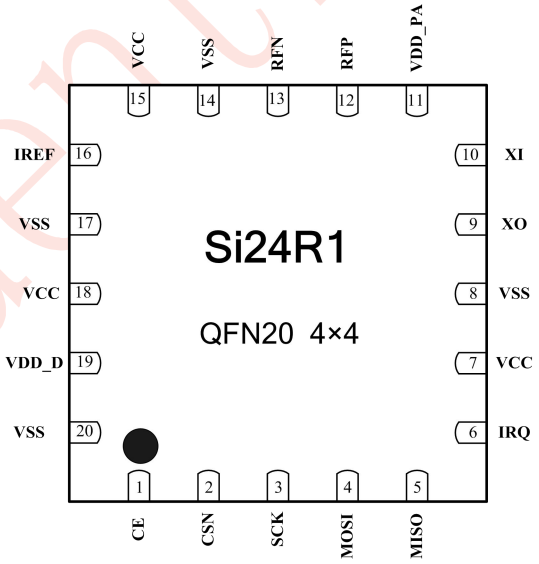
Key Features

- 2.4GHz ISM band operation
- Modulation：GFSK/FSK
- Air data rate：2Mbps/1Mbps/250Kbps
- Ultra low shutdown current：1uA
- Ultra low standby current：15uA
- Receiver sensitivity：-83dBm @2MHz
- Maximum transmission power：7dBm
- RX supply current @ 2Mbps：15mA
- TX supply current @ 2Mbps: 12mA（0dBm)
- Internal integrated high PSRR LDO
- Supply range：1.9-3.6V
- Digital I/O voltage range: 1.9-5.25V
- Maximum 130us start-up from standby mode
- Maximum 10MHz, 4-pin hardware SPI
- Embedded ARQ baseband protocol engine
- Hardware interrupt output
- Support 1bit RSSI output
- Low cost crystal：16MHz±60ppm
- Few peripheral components needed
- QFN package or COB package

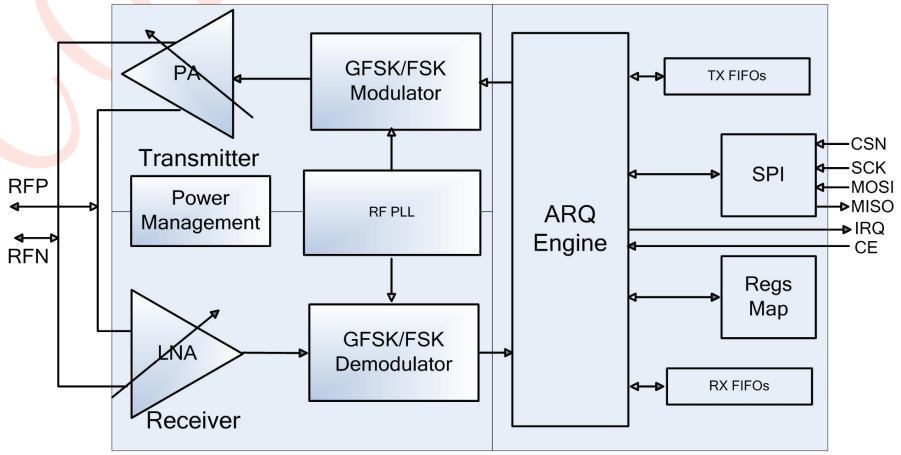
Applications

- Wireless mice and keyboards
- Remote control
- Active RFID、NFC
- Smart Grid、Home automation
- Wireless audio
- Wireless data transceiver module
- Ultra low power wireless Ad hoc sensor networks

Pin Assignments



Block diagram



Abbreviations

AI	Analog Input
ARQ	Auto Repeat Re-quest
ART	Auto Re-Transmission
ARD	Auto Retransmission Delay
AO	Analog Output
BER	Bit Error Rate
CE	Chip Enable
CRC	Cyclic Redundancy Check
CSN	Chip Select NOT
DPL	Dynamic Payload Length
DI	Digital Input
DO	Digital Output
GFSK	Gaussian Frequency Shift Keying
IRQ	Interrupt Request
ISM	Industrial-Scientific-Medical
LSB	Least Significant Bit
Mbps	Megabit per second
MCU	Microcontroller Unit
MHz	Mega Hertz
MISO	Master In Slave Out
MOSI	Master Out Slave In
MSB	Most Significant Bit
PA	Power Amplifier
PID	Packet Identity Bits
PLD	Payload
PO	Power Output
PWR_DWN	Power Down
PWR_UP	Power UP
RF_CH	Radio Frequency Channel
RSSI	Received Signal Strength Indicator
RX	Receiver
RX_DR	Receive Data Ready
SCK	SPI Clock
SPI	Serial Peripheral Interface
TX	Transmitter
TX_DS	Transmit Data Sent
XTAL	Crystal

Contents

1 Introduction

Si24R1 is a single chip transceiver with an embedded ARQ baseband protocol engine, operating in the world wide ISM frequency band, suitable for ultra low power wireless applications. The operating frequency band from 2400MHz to 2525MHz is divided into 126 RF channels and the resolution of the RF channel frequency setting is 1MHz.

Si24R1 uses GFSK/FSK digital modulation and demodulation. Both air data rate and output power are configurable. The air data rate can be programmed to 2Mbps, 1Mbps and 250Kbps. The higher data rate contributes the lower power consumption because it takes less time to transmit or receive signals.

Si24R1 is especially optimized for low power wireless applications. All register values and FIFO values are maintained in shutdown mode, and the shutdown supply current is 1uA. In standby mode, the clock still works, and the standby supply current is 15uA. It takes less than 130us to start data transmitting and receiving.

Si24R1 is easy to use, and it can realize communication only by configuring several registers through the SPI with an MCU. The embedded ARQ baseband protocol engine is based on packet communication and supports various modes from manual operation to advanced autonomous ARQ protocol operation. Internal FIFOs ensure a smooth data flow between the radio front end and the system's MCU. Enhanced ARQ baseband protocol engine reduces system cost by handling all the high speed link layer operations.

To design a radio system with the Si24R1, only an MCU and a few external passive components are needed. Internal high PSRR LDO power ensures reliable work in a wide supply range from 1.9V to 3.6V. Digital I/O is compatible with several I/O voltage standards such as 2.5V/3.3V/5V, and it can be directly connected to various MCU I/O ports.

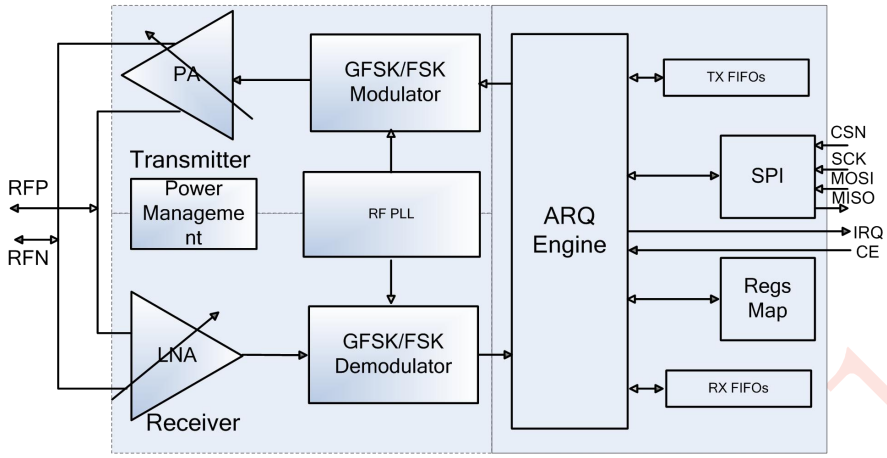


Figure 1-1 Si24R1 block diagram

2 Pin Information

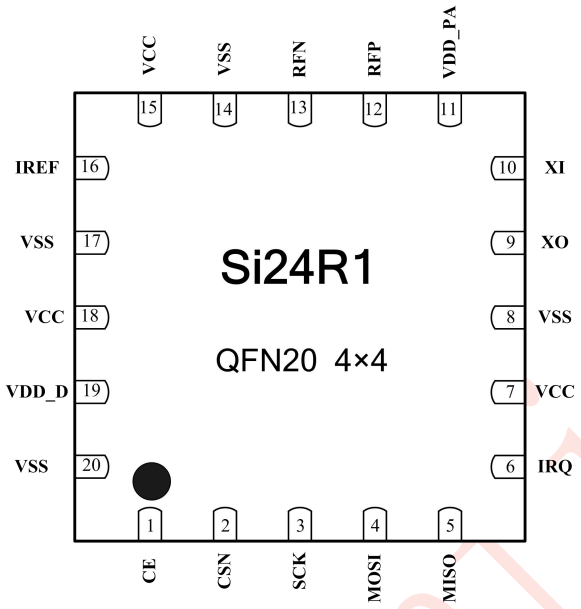


Figure 2-1 Si24R1 pin information（QFN20 4×4 package）

Table 2.1 pin function

Pin	Name	Type	Pin function
1	CE	DI	Chip Enable Activates RX or TX mode
2	CSN	DI	SPI Chip Select, Active low
3	SCK	DI	SPI Clock
4	MOSI	DI	SPI Slave Data Input
5	MISO	DO	SPI Slave Data Output
6	IRQ	DO	Maskable interrupt pin. Active low
7，15，18	VCC	Power	Power supply（+1.9～+3.6V，DC）
8，14，17，20	VSS	Power	Ground（0V）
9	XO	AO	Crystal oscillator output
10	XI	AI	Crystal oscillator input
11	VDD_PA	Power	1.8V power supply output for the internal Power Amplifier
12	RFP	RF	Antenna Positive
13	RFN	RF	Antenna Negative
16	IREF	AI	Reference current.
19	VDD_D	PO	Internal digital supply output for de-coupling purposes
	Die exposed	Power	Ground（0V），connect die exposed to PCB ground

3 Operational modes

3.1 State Control Diagram

The built-in state machine in Si24R1 controls the transitions between the chip's different operating modes.

The state transition diagram in Figure3-1 shows five operating modes of the Si24R1. The five operating modes are: Shutdown、Standby、Idle-TX、TX and RX.

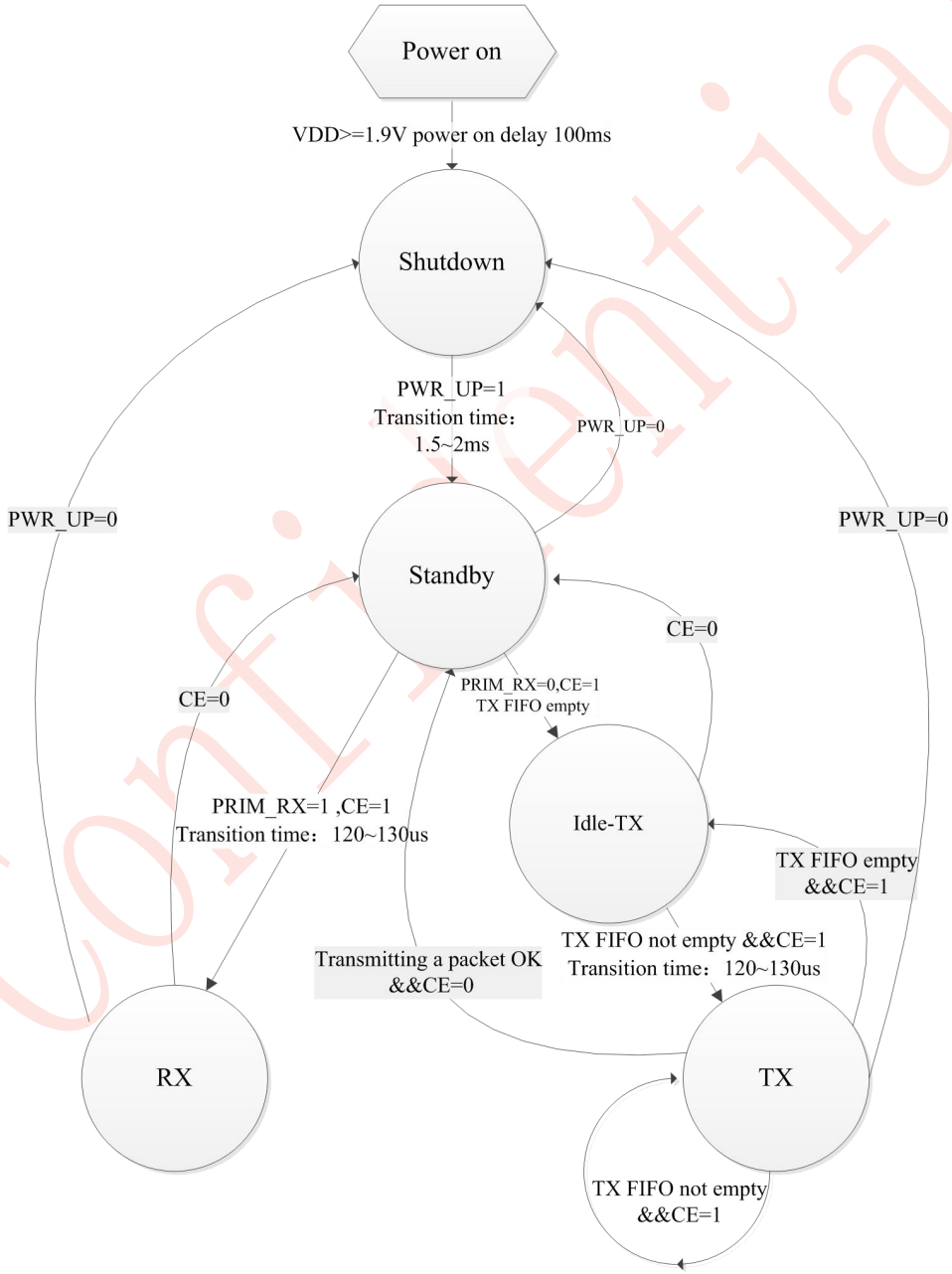


Figure 3-1 Si24R1 state control diagram

3.1.1 Shutdown Mode

In shutdown mode Si24R1 is disabled, the function of data transmitting and receiving is stopped, and the current consumption is minimal. All register values available are maintained and can be written or read by SPI which is kept active. Shutdown mode is entered by clearing the PWR_UP bit in the CONFIG register.

3.1.2 Standby Mode

In standby mode only part of crystal oscillator is active. Standby mode ensures minimum average current consumption while maintaining short start-up time. Standby mode is entered after the crystal oscillator works stably by setting PWR_UP bit in the CONFIG register to 1. The crystal oscillator startup time is about 1.5~2ms, responding to the oscillator quality. The Si24R1 enters Idle-TX mode or RX mode by setting CE high. When CE pin is set low, Si24R1 returns to standby mode from Idle-TX mode, TX mode or RX mode.

3.1.3 Idle-TX Mode

In Idle-TX mode the crystal oscillator and clock buffers are active and more current is used compared to standby mode. Idle-TX mode is entered when CE is set high and TX FIFO is empty on a PTX device. If a new packet is uploaded to the TX FIFO, TX mode is entered and the packet is transmitted.

Both in standby and Idle-TX mode all register and FIFO values available are maintained and can be written or read by SPI.

3.1.4 TX Mode

The TX mode is an active mode for transmitting packets. When the PWR_UP is set high, the PRIM_RX is set low, a payload in the TX FIFO, and a high pulse on the CE pin for more than 10us, the Si24R1 enters this mode. The transition time from Idle-TX mode to TX mode takes 120us~130us. After transmitting a packet, if CE = 1, the status of TX determines the next mode. If the TX FIFO is not empty the Si24R1 remains in TX mode and transmits the next packet. If the TX FIFO is empty the Si24R1 returns to Idle-TX mode. If CE = 0, Si24R1 returns to standby mode. The Si24R1 provides an interrupt after finishing a packet transmitting.

3.1.5 RX Mode

The RX mode is an active mode for receiving packets. When the PWR_UP bit, the PRIM_RX bit and the CE pin are set high, the Si24R1 enters this mode. The transition time from Standby mode to RX mode is 120us~130us. When a valid packet is found by a matching address and a valid CRC, the payload of the packet will be downloaded to RX FIFOs automatically. Si24R1 can store 3 valid packets at most, if the RX FIFOs are full, the received packet will be discarded.

In RX mode the power of received signal can be detected by RSSI register. If the received signal power is higher than -60dBm, the RSSI bit of RSSI register will be set high. There are two methods for updating RSSI register, one is if Si24R1 received a valid packet, then RSSI will update automatically, the other is when operating mode changes from RX mode to Standby mode, RSSI will update automatically. Besides, RSSI will change (±5dBm at most) with the varying temperature.

4 Packet processing protocol

Si24R1 is based on packet communication and supports ARQ protocol. Internal ARQ baseband protocol engine can realize automatic ACK and NO_ACK packet handling without an extra MCU. ARQ baseband supports the handling of 1 to 32 bytes dynamic payload length. Besides, it supports static payload length which is set by registers. Baseband handling features automatic packet disassembly and assembly, automatic acknowledgement and retransmissions of packet. It also has 6 data pipes for 1:6 star networks.

4.1 ARQ packet format

A whole packet contains a preamble, address, packet control, payload and CRC field. Figure4-1 shows the packet format with MSB to the left.

Preamble	Address	Packet control	Payload	CRC
1Byte	3-5 Bytes	9 Bit	1-32 Bytes	0-2Bytes

Figure 4-1 A whole ARQ packet

The preamble is used to synchronize the receivers demodulator to the incoming bit stream. It is added by transmitter and discarded by receiver, and shielded for users.

The address field stores the packet address values for the receiver. A packet will be received only when the address of the packet matches the address of the receiver. The address field width in the AW register can be configured to be 3, 4 or 5 bytes.

Figure 4-2 shows the format of the 9 bit packet control field.

Payload length 6bit	PID 2bit	NO_ACK 1bit

Figure 4-2 Format of packet control field

The 6 bit payload length specifies the length of the payload in bytes ranges from 0 to 32 bytes.

For example：000000 = 0 byte (no payload)

100000 = 32 byte (32 bytes of payload)

The PID field is used to tell the receiver if the received packet is new or retransmitted. PID prevents the PRX device from receiving the same payload more than once. The PID field is incremented at the PTX device when a new packet is written to FIFO through SPI.

When NO_ACK equals 1, the RTX device doesn’t need to send ACK to the PTX device.

For the transmitter, to set NO_ACK high, the EN_DYN_ACK bit in the feature register must be set high first, and the NO_ACK flag bit is set with this command: W_TX_PAYLOAD_NOACK.

The CRC field is used to detect if there is an error in the packet. The number of bytes in the CRC is either 1 or 2 bytes, set by the CRCO bit in the CONFIG register.

4.2 ARQ communication mode

In the TX mode the PTX device assembles the preamble, address, packet control field, payload and CRC to make a complete packet first and then it transmits the packet with RF module.

In the RX mode the receiver constantly searches for a valid packet by a matching address and a valid CRC. After the packet is validated, the receiver disassembles the packet and presents the payload in a vacant slot in the RX FIFO and asserts the RX_DR IRQ. MCU can read data in the RX FIFO through SPI at any time.

4.2.1 ACK mode

4.2.1.1 Auto acknowledge on the PRX

The function of auto acknowledgement means the PRX will transmit an ACK packet to the PTX automatically after it has received and validated a packet. The function of auto acknowledgement is enabled by the EN_AA register. If the PTX needs to receive an ACK and tell it to PRX through packet, then the PRX must enable the auto acknowledgement feature.

Figure 4-3 shows ACK mode.

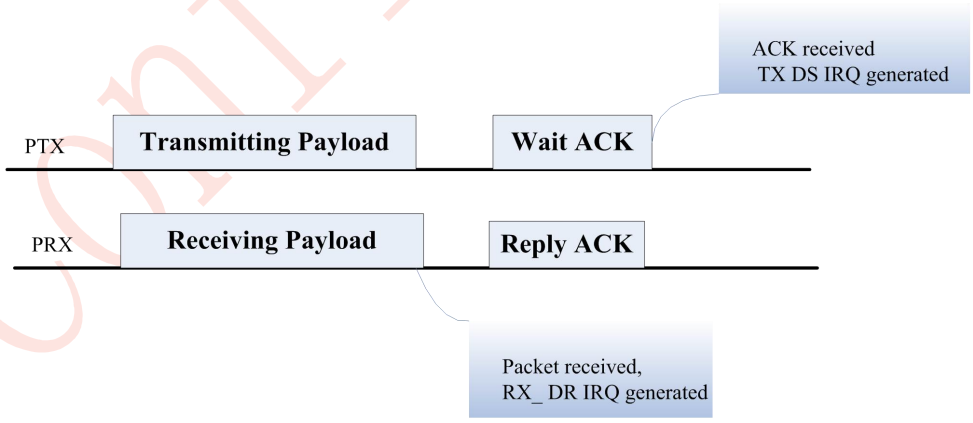


Figure 4-3 ACK mode

In general, an ACK packet is an empty one only containing Control, Address and CRC field. However, in ACK payload mode the PRX can transmit an ACK with an optional payload, and the PTX will download the payload into TX FIFO after receiving the ACK packet. In order to use this feature, the EN_ACK_PAY bit in the FEATURE register must be set and the Dynamic Payload Length (DPL) must be

enabled.

Figure 4-4 shows the ACK payload mode.

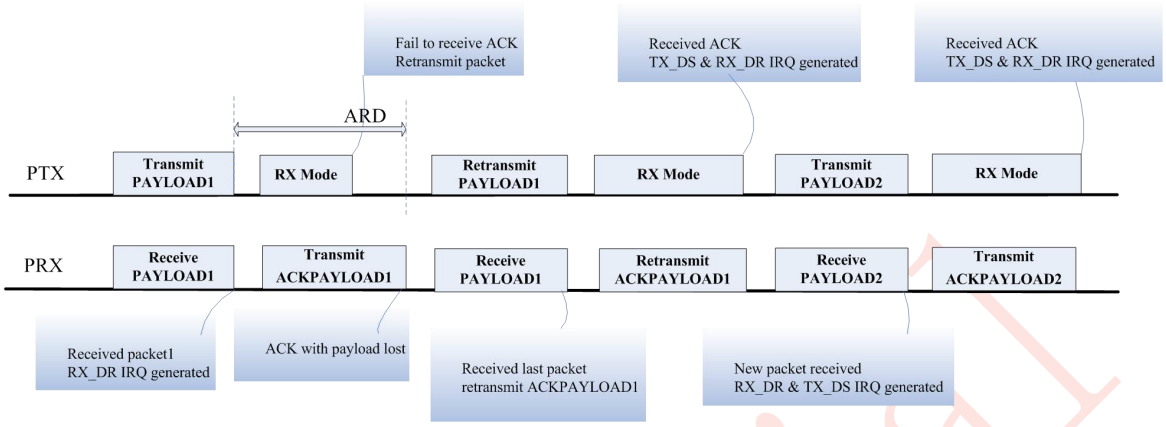


Figure 4-4 ACK payload mode

4.2.1.2 Auto retransmission on the PTX

The function of auto retransmission means that in an auto acknowledgement configuration on the PTX, the PTX will retransmit a packet if an ACK packet is not received. Each time a packet is transmitted, the PTX enters RX mode and waits a short period defined by ARD for an ACK packet. If the ACK packet is not received in the delay, Si24R1 goes back to TX mode to retransmit the data. ARD is a short delay time from the end of a transmitted packet to when a retransmit starts on the PTX. When the ACK packet is received, Si24R1 asserts the TX_DS IRQ. The retransmission continues until acknowledgment is received, or the maximum number of retransmits defined by ARC is reached. ARC is the programmed maximum number of times of retransmission. The ARC and ARD are set in the SETUP_RETR register.

The ARC_CNT counts the number of retransmissions for the current packet and is reset by transmitting a new packet. If the PTX doesn't receive an ACK during ARD, it will retransmit the packet and ARC_CNT will be incremented. MAX_RT interrupt request is asserted if the number of retransmission (ARC_CNT) exceeds ARC.

Additionally, it is possible to manually set the Si24R1 to retransmit a packet a number of times by the REUSE_TX_PL command. And when this command is used, the MCU must initiate each transmission of the packet with a pulse on the CE pin.

4.2.2 NOACK Mode

The NOACK flag in control field will be valid if PTX uses W_TX_PAYLOAD_NOACK command writing data into TX FIFO. Setting the flag means that the PRX needn't to transmit an ACK payload after receiving a packet, and the PTX will go directly into standby-I mode after transmitting the packet.

Additionally, the EN_DYN_ACK bit in FEATURE register must be set before using W_TX_PATLOAD_NOACK command.

4.2.3 Dynamic payload length (DPL) and static payload length

A payload can be 0-32 bytes wide, and Si24R1 provides two alternatives for payload length: static and dynamic. By default, it will be a static length payload. Static payload length is set by the RX_PW_PX registers on the receiver side.

DPL enables PTX to send packets with variable payload length to the receiver. The external MCU can read out the payload length by using R_RX_PL_WID command. In order to enable DPL the EN_DPL bit in Feature register must be set. For PRX, DYNPD must be set. A PTX device with DPL enabled must have the DPL_P0 bit in DYNPD register set.

4.2.4 Multi data pipes communication

Up to six Si24R1s configured as PTX can communicate with one Si24R1 configured as a PRX (primary receiver). The PRX can receive data from six different data pipes (six different PTXs) in one frequency channel at different time. Each data pipe has its own unique address and can be configured for individual behavior. The PRX searches for all the data pipe addresses simultaneously. And only one data pipe can work at a time. The data pipes are activated by setting the bits in the EN_RXADDR register. And each data pipe address is configured in RX_ADDR_PX registers. By default, pipe 0 and pipe 1 are enabled only. To ensure the PRX transmit an ACK packet to the correct PTX, the PRX takes the data pipe address where it received the packet and uses it as the TX address when transmitting the ACK packet. Only when a data pipe receives a complete packet can other data pipes begin to receive data. When multiple PTXs are transmitting to a PRX, the ARD can be used to skew the auto retransmission so that they only block each other once.

Figure 4-6 shows a transceiver configuration example.

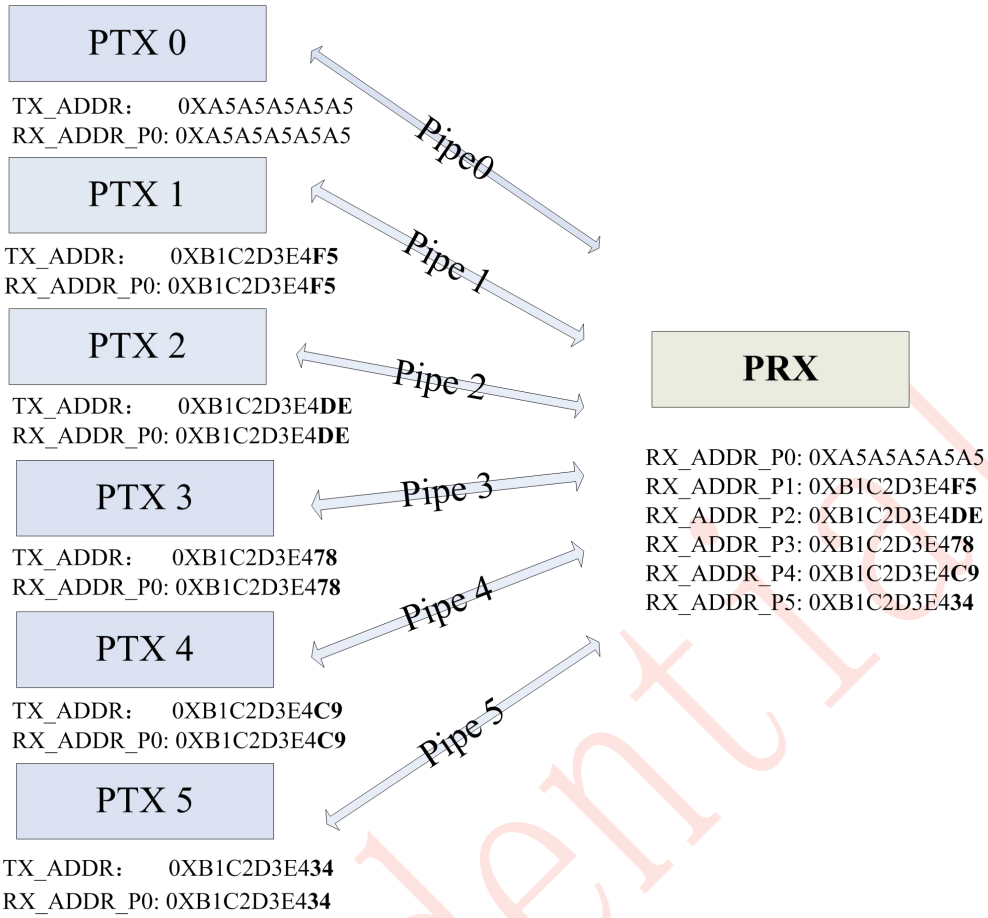


Figure 4-6 Multi pipes receiver example

5 SPI Interface

The SPI interface is a standard 4-wire SPI with a maximum data rate of 10 Mbps .

5.1 SPI Commands

Table 5-1 shows the SPI commands, and every new command must be started by a high to low transition on CSN pin.
In parallel to the SPI command word applied on the MOSI pin, the STATUS register is shifted serially out on the MISO pin.

- <Command byte: MSBit to LSBit > -- one byte
- <Data bytes: LSByte to MSByte, MSBbit of every byte first >

Command name	Command word (binary)	# Data bytes	Operation
R_REGISTER	000A AAAA	1 to 5 LSByte first	Read register command AAAAA= 5 bit Register address
W_REGISTER	001A AAAA	1 to 5 LSByte first	write register command AAAAA= 5 bit Register address Executable in power down or standby modes only.
R_RX_PAYLOAD	0110 0001	1 to 32 LSByte first	Read RX payload, used in RX mode. LSB is first read out , 1- 32 bytes
W_TX_PAYLOAD	1010 0000	1 to 32 LSByte first	Write TX payload, used in TX mode LSB is first write in, 1-32 bytes
FLUSH_TX	1110 0001	0	Flush TX FIFO , used in TX mode
FLUSH_RX	1110 0010	0	Flush RX FIFO, used in RX mode should not be used during transmission of ACK packet
REUSE_TX_PL	1110 0011	0	Used for PTX Reuse last payload Payload reuse is active until W_TX_PAYLOAD or FLUSH_TX is executed.
R_RX_PL_WID	0110 0000	1	Read RX payload width of the top RX FIFO
W_ACK_PAYLOAD	1010 1PPP	1 to 32 LSByte first	Used in RX mode Write payload to be transmitted with ACK packet on pipe PPP (0~5).
W_TX_PAYLOAD_NOACK	1011 0000	1 to 32 LSByte first	Used in TX mode. PTX needn't wait the ACK packet in this mode

NOP	1111 1111	0	No operation. Can be used to get the value of STATUS register

Table 5-1 SPI Commands

5.2 SPI Timing

Figure 5-1 to Figure 5-3 shows the SPI operation and timing restriction. The configuration registers can only be written in Shutdown/Standby/Idle-Tx mode.

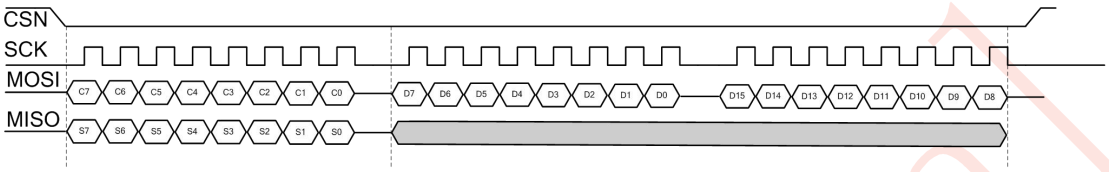


Figure 5-1 SPI write operation

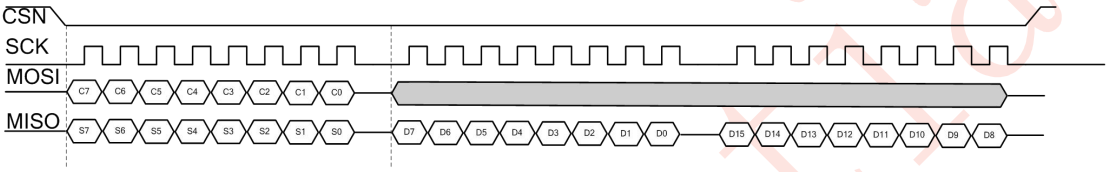


Figure 5-2 SPI read operation

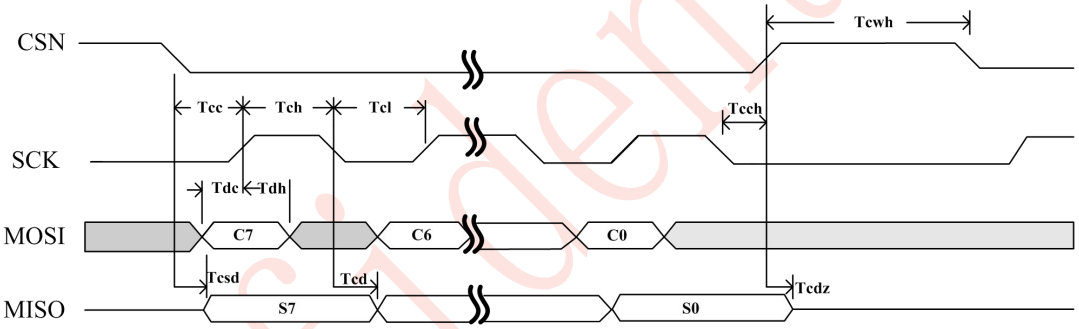


Figure 5-3 SPI typical timing

Table 5-1 shows SPI Interface typical timing parameter

Symbol	Parameters	Min	Max	Units
Tdc	Data to SCK Setup	2		ns
Tdh	SCK to Data Hold	2		ns
Tcsd	CSN to Data Valid		42	ns
Tcd	SCK to Data Valid		58	ns
Tcl	SCK Low Time	40		ns
Tch	SCK High Time	40		ns
Fsck	SCK Frequency	0	10	MHz
Tr,Tf	SCK Rise and Fall		100	ns
Tcc	CSN to SCK Setup	2		ns
Tcch	SCK to CSN Hold	2		ns
Tcwh	CSN Inactive time	50		ns
Tcdz	CSN to Output High Z		42	ns

Table 5-1 SPI timing parameter

6 Register Table

Address (Hex)	Mnemonic	Bit	Reset Value	Type	Description
00	CONFIG				Configuration Register
	Reserved	7	0	R/W	Only ‘0’ allowed
	MASK_RX_DR	6	0	R/W	Mask interrupt caused by RX_DR 1: Interrupt not reflected on the IRQ pin 0: Reflect RX_DR as active low interrupt on the IRQ pin
	MASK_TX_DS	5	0	R/W	Mask interrupt caused by TX_DS 1: Interrupt not reflected on the IRQ pin 0: Reflect TX_DS as active low interrupt on the IRQ pin
	MASK_MAX_RT	4	0	R/W	Mask interrupt caused by MAX_RT 1: Interrupt not reflected on the IRQ pin 0: Reflect MAX_RT as active low interrupt on the IRQ pin
	EN_CRC	3	1	R/W	Enable CRC. Forced high if one of the bits in the EN_AA is high
	CRCO	2	0	R/W	CRC encoding scheme '0' - 1 byte '1' - 2 bytes
	PWR_UP	1	0	R/W	1: POWER UP, 0:POWER DOWN
	PRIM_RX	0	0	R/W	RX/TX control, 1: PRX, 0: PTX
01	EN_AA				Enable „Auto Acknowledgment“ Function
	Reserved	7:6	00	R/W	Only '00' allowed
	ENAA_P5	5	1	R/W	Enable auto acknowledgement data pipe 5
	ENAA_P4	4	1	R/W	Enable auto acknowledgement data pipe 4
	ENAA_P3	3	1	R/W	Enable auto acknowledgement data pipe 3
	ENAA_P2	2	1	R/W	Enable auto acknowledgement data pipe 2
	ENAA_P1	1	1	R/W	Enable auto acknowledgement data pipe

					1
	ENAA_P0	0	1	R/W	Enable auto acknowledgement data pipe 0
02	EN_RXADDR				Enabled RX Addresses
	Reserved	7:6	00	R/W	Only '00' allowed
	ERX_P5	5	0	R/W	Enable data pipe 5
	ERX_P4	4	0	R/W	Enable data pipe 4
	ERX_P3	3	0	R/W	Enable data pipe 3
	ERX_P2	2	0	R/W	Enable data pipe 2
	ERX_P1	1	1	R/W	Enable data pipe 1
	ERX_P0	0	1	R/W	Enable data pipe 0
03	SETUP_AW				Setup of Address Widths
	Reserved	7:2	000000	R/W	Only '000000' allowed
	AW	1:0	11	R/W	RX/TX Address field width '00' – Illegal '01' - 3 bytes '10' - 4 bytes '11' - 5 bytes LSB bytes are used if address width is below 5 bytes
04	SETUP_RETR				Setup of Automatic Retransmission
	ARD	7:4	0000	R/W	Auto Retransmission Delay ‘0000’ – Wait 250uS ‘0001’ - Wait 500uS ‘0010’ - Wait 750uS …… ‘1111’ – Wait 4000uS
	ARC	3:0	0011	R/W	Auto Retransmit Count ‘0000’ – Retransmit disabled ‘0001’ – Up to 1 Re-Transmission ‘0010’ – …… ‘1111’ –Up to 15 Re-Transmission
					Up to 1 Re-Transmission
05	RF_CH				RF Channel
	Reserved	7	0	R/W	Only ‘0’ allowed
	RF_CH	6:0	0000010	R/W	Sets the frequency channel
06	RF_SETUP				RF Setup

	CONT_WAVE	7	0	R/W	'1' Const carrier wave, for test only
	Reserved	6	0	R/W	Only '0'allowed
	RF_DR_LOW	5	0	R/W	Set RF Data Rate. See RF_DR_HIGH for encoding
	PLL_LOCK	4	0	R/W	Only '0'allowed
	RF_DR_HIGH	3	1	R/W	Set RF Data Rate [RF_DR_LOW, RF_DR_HIGH]: '00' - 1Mbps '01' - 2Mbps '10' - 250kbps '11' - Reserved
	RF_PWR	2:0	110	R/W	Set RF output power in TX mode RF_PWR[2:0] 111: 7dBm 110: 4dBm 101: 3dBm 100: 1dBm 011: 0dBm 010:-4dBm 001:-6dBm 000:-12dBm
07	STATUS				Status Register (In parallel to the SPI command word applied on the MOSI pin, the STATUS register is shifted serially out on the MISO pin)
	Reserved	7	0	R/W	only '0' allowed
	RX_DR	6	0	R/W	Data ready RX FIFO interrupt Asserted when new data arrives RX FIFO Write '1' to clear bit
	TX_DS	5	0	R/W	Data sent TX FIFO interrupt Asserted when packet transmitted on TX. If AUTO_ACK is activated, this bit is set high only when ACK is received Write '1' to clear bit
	MAX_RT	4	0	R/W	Maximum number of TX retransmits interrupt. If MAX_RT is asserted, it must be cleared to enable further communication Write '1' to clear bit
	RX_P_NO	3:1	111	R	
	TX_FULL	0	0	R	TX FIFO full flag '1' – TX FIFO full '0' – Available locations in TX FIFO
08	OBSERVE_TX				Transmit observe register

	PLOS_CNT	7:4	0	R	Count lost packets. The counter is overflow protected to 15, and discontinues at max until reset. The counter is reset by writing to RF_CH
	ARC_CNT	3:0	0	R	Count retransmitted packet. The counter is reset when transmission of a new packet starts
09	RSSI				Received Power Detector
	Reserved	7:1	000000	R	
	RSSI	0	0	R	Received Power Detector： ‘0’ - Received Power is less than -60dbm
0A	RX_ADDR_P0	39:0	0xE7E7E7E7E7	R/W	Receive address data pipe 0. 5 Bytes maximum length. (LSByte is written first. Write the number of bytes defined by SETUP_AW)
0B	RX_ADDR_P1	39:0	0xC2C2C2C2C2	R/W	Receive address data pipe 1. 5 Bytes maximum length. (LSByte is written first. Write the number of bytes defined by SETUP_AW)
0C	RX_ADDR_P2	7:0	0xC3	R/W	Receive address data pipe 2. Only LSB MSB bytes is equal to RX_ADDR_P1[39:8]
0D	RX_ADDR_P3	7:0	0xC4	R/W	Receive address data pipe 3. Only LSB MSB bytes is equal to RX_ADDR_P1[39:8]
0E	RX_ADDR_P4	7:0	0xC5	R/W	Receive address data pipe 4. Only LSB MSB bytes is equal to RX_ADDR_P1[39:8]
0F	RX_ADDR_P5	7:0	0xC6	R/W	Receive address data pipe 5. Only LSB MSB bytes is equal to RX_ADDR_P1[39:8]
10	TX_ADDR	39:0	0xE7E7E 7E7E7	R/W	Transmit address. Used for a PTX device only. (LSB byte is written first) Set RX_ADDR_P0 equal to this address to handle automatic acknowledge if this is a PTX device
11	RX_PW_P0				
	Reserved	7:6	00	R/W	Only ‘00’ allowed

	RX_PW_P0	5:0	0	R/W	Number of bytes in RX payload in data pipe0(1 to 32 bytes) 0:not used 1: 1bytes …… 32: 32bytes
12	RX_PW_P1				
	Reserved	7:6	00	R/W	Only '00' allowed
	RX_PW_P1	5:0	0	R/W	Number of bytes in RX payload in data pipe 1(1 to 32 bytes) 0:not used 1: 1bytes …… 32: 32bytes
13	RX_PW_P2				
	Reserved	7:6	00	R/W	Only '00' allowed
	RX_PW_P2	5:0	0	R/W	Number of bytes in RX payload in data pipe 2(1 to 32 bytes) 0:not used 1: 1bytes …… 32: 32bytes
14	RX_PW_P3				
	Reserved	7:6	00	R/W	Only '00' allowed
	RX_PW_P3	5:0	0	R/W	Number of bytes in RX payload in data pipe 3(1 to 32 bytes) 0:not used 1: 1bytes …… 32: 32bytes
15	RX_PW_P4				
	Reserved	7:6	00	R/W	Only '00' allowed
	RX_PW_P4	5:0	0	R/W	Number of bytes in RX payload in data pipe 4(1 to 32 bytes) 0:not used 1: 1bytes …… 32: 32bytes

16	RX_PW_P5				
	Reserved	7:6	00	R/W	Only ‘00’ allowed
	RX_PW_P5	5:0	0	R/W	Number of bytes in RX payload in data pipe 5(1 to 32 bytes) 0:not used 1: 1bytes …… 32: 32bytes
17	FIFO_STATUS				FIFO Status
	Reserved	7	0	R/W	Only ‘0’ allowed
	TX_REUSE	6	0	R	Used for PTX, Reuse last transmitted data packet if set high TX_REUSE is set by the SPI command REUSE_TX_PL, and is reset by the SPI command W_TX_PAYLOAD or FLUSH_TX
	TX_FULL	5	0	R	TX FIFO full flag ‘1’ – TX FIFO full ‘0’ - TX FIFO not full
	TX_EMPTY	4	1	R	TX FIFO empty flag ‘1’ – TX FIFO empty ‘0’ - TX FIFO not empty
	Reserved	3:2	00	R/W	Only ‘0’ allowed
	RX_FULL	1	0	R	RX FIFO full flag ‘1’ – RX FIFO full ‘0’ - RX FIFO not full
	RX_EMPTY	0	1	R	RX FIFO empty flag ‘1’ – RX FIFO empty ‘0’ - RX FIFO not empty
1C	DYNPD				Enable dynamic payload length
	Reserved	7:6	0	R/W	Only ‘00’ allowed
	DPL_P5	5	0	R/W	Enable dynamic payload length data pipe5(Set EN_DPL & ENAA_P5)
	DPL_P4	4	0	R/W	Enable dynamic payload length data pipe4(Set EN_DPL & ENAA_P4)
	DPL_P3	3	0	R/W	Enable dynamic payload length data pipe3(Set EN_DPL & ENAA_P3)
	DPL_P2	2	0	R/W	Enable dynamic payload length data pipe2(Set EN_DPL & ENAA_P2)
	DPL_P1	1	0	R/W	Enable dynamic payload length data pipe1(Set EN_DPL & ENAA_P1)

	DPL_P0	0	0	R/W	Enable dynamic payload length data pipe0(Set EN_DPL & ENAA_P0)
1D	FEATURE			R/W	Feature Register
	Reserved	7:3	0	R/W	Only '00000' allowed
	EN_DPL	2	0	R/W	Enable dynamic payload length
	EN_ACK_PAY	1	0	R/W	Enable Payload with ACK
	EN_DYN_ACK	0	0	R/W	Enable the W_TX_PAYLOAD_NOACK command

7 Electrical specification

7.1 Limitation parameter

Operating Condition	Min.	Max.	Unit
Supply Voltages			
VDD	-0.3	3.6	V
VSS		0	V
Input Voltage			
VI	-0.3	5.25	V
Output Voltage			
VO	VSS to VDD	VSS to VDD	V
Power Dissipation			
		100	mW
Temperatures			
Operation Temperature	-40	+85	℃
Storage Temperature	-40	+125	℃
ESD Performance	HBM(Human Body Model): Class 1C		

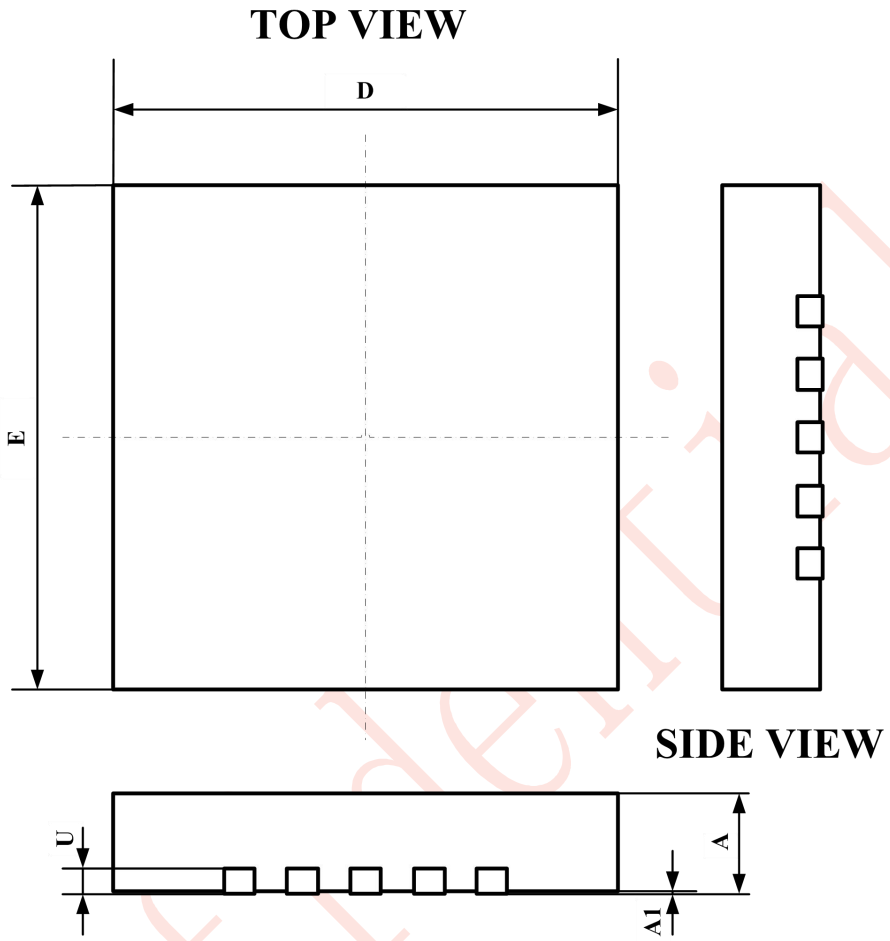
7.2 Electrical specification

Conditions: VDD = 3V, VSS = 0V , TA = 27℃ , crystal oscillator C_L=12pF

Symbol	parameter	Min.	Typ.	Max.	Unit	Comment
OP Parameters						
VDD	Supply voltage	1.9		3.6	V	
I_{SHD}	Supply current in shutdown mode		1		μA	
I_{STB}	Supply current in standby mode		15		μA	
I_{IDLE}	Supply current in idle-tx mode		380		μA	
I_{RX}@2MHZ	RX mode supply current @2Mbps		15		mA	
I_{RX}@1MHZ	RX mode supply current @1Mbps		14.5		mA	
I_{RX}@250kbps	RX mode supply current @250kbps		14		mA	
I_{TX}@7dBm	TX mode supply current @7dBm output power		25		mA	
I_{TX}@4dBm	TX mode supply current @4dBm output power		16		mA	
I_{TX}@0dBm	TX mode supply current		12		mA	

	@0dBm output power					
I_{TX}@-6dBm	TX mode supply current @-6dBm output power		9.5		mA	
I_{TX}@-12dBm	TX mode supply current @-12dBm output power		8.5		mA	
RF Parameter						
F_{OP}	RF operation frequency	2400		2525	MHz	
F_{CH}	RF channel space	1			MHz	2Mpbs 时至少为 2MHz
ΔF_{MOD}(2Mbps)	Frequency deviation		±330		KHz	
ΔF_{MOD}(1M/250Kbps)	Frequency deviation		±175		KHz	
R_{GFSK}	Data rate	250		2000	Kbps	
RX Parameter						
RX_{SENS}@2Mbps	Sensitivity@2Mbps		-83		dBm	BER=0.1%
RX_{SENS}@1Mbps	Sensitivity@1Mbps		-87		dBm	BER=0.1%
RX_{SENS}@250Kbps	Sensitivity@250kbps		-96		dBm	BER=0.1%
C/I_{CO}@2Mbps	C/I Co-channel		6		dB	
C/I_{1st}@2Mbps	1st ACS C/I 2MHz		0		dB	
C/I_{2ND}@2Mbps	2nd ACS C/I 4MHz		-20		dB	
C/I_{3RD}@2Mbps	3rd ACS C/I 6MHz		-26		dB	
C/I_{CO}@1Mbps	C/I Co-channel		7		dB	
C/I_{1st}@1Mbps	1st ACS C/I 2MHz		6		dB	
C/I_{2ND}@1Mbps	2nd ACS C/I 4MHz		-21		dB	
C/I_{3RD}@1Mbps	3rd ACS C/I 6MHz		-30		dB	
TX 参数						
P_{RF}	RF Output Power	-30		7	dBm	
P_{BW}@2Mbps	Modulation Bandwidth		2.1		MHz	
P_{BW}@1Mbps	Modulation Bandwidth		1.1		MHz	
P_{BW}@250Kbps	Modulation Bandwidth		0.9		MHz	
P_{RF1}	1st Adjacent CH Power 2MHz			-20	dBm	
P_{RF2}	2nd Adjacent CH Power 4MHz			-46	dBm	
Crystal Oscillator Parameter						
F_{XO}	Crystal frequency		16		MHz	
ΔF	Tolerance		±60		ppm	
ESR	Equivalent Series Resistance		100		Ω	

8 Package



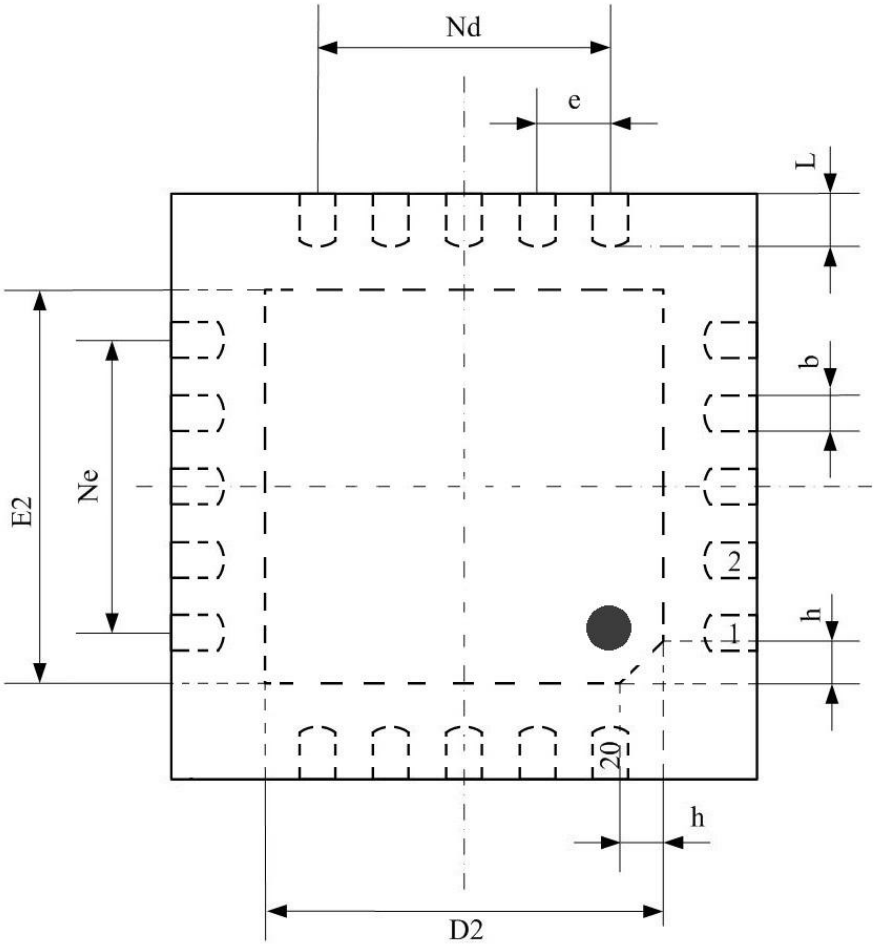


Figure 8-1 Top view

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.18	0.25	0.30
D	3.90	4.00	4.10
D2	2.55	2.65	2.75
e	0.50BSC		
E2	2.55	2.65	2.75
E	3.90	4.00	4.10
Ne	2.00BSC		
Nd	2.00BSC		
L	0.35	0.40	0.45
h	0.30	0.35	0.40
U	0.20 REF.		
L/F (mil)	114×114		

Table 8-2 Package measurement

9.1 Typical Application Schematic

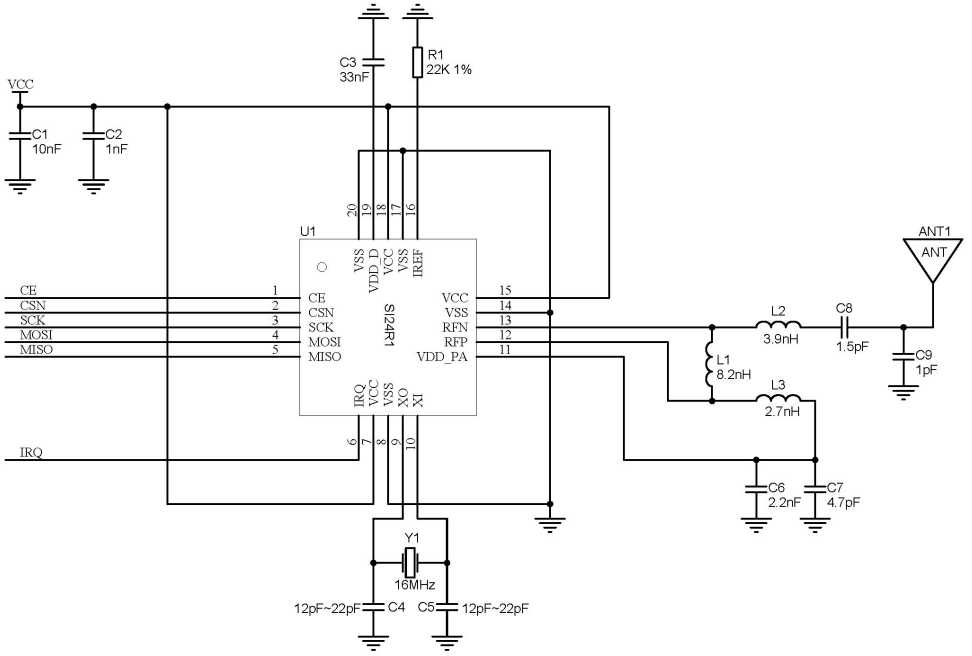


Figure 9-1 Typical application schematic

name	value	form	description
C1	10nF	0402	X7R, +/- 10%
C2	1nF	0402	X7R, +/- 10%
C3	33nF	0402	X7R, +/- 10%
C4	12~22pF	0402	NPO, +/- 2%
C5	12~22pF	0402	NPO, +/- 2%
C6	2.2nF	0402	X7R, +/- 10%
C7	4.7pF	0402	NPO, +/- 0.25pF
C8	1.5pF	0402	NPO, +/- 0.1pF
C9	1.0pF	0402	NPO, +/- 0.1pF
L1	8.2nH	0402	chip inductor, +/- 5%
L2	3.9nH	0402	chip inductor, +/- 5%
L3	2.7nH	0402	chip inductor, +/- 5%
R1	22KΩ	0402	+/- 1%
R2	Not mounted	0402	
Y1	16MHz		+/-60ppm, CL=12pF
U1		QFN20 04×04	

Table 9-1 Recommended components (BOM)

9.2 PCB layout

A double-sided FR-4 board of 1.6mm thickness is used. The bottom layer of PCB is the ground plane. To achieve good RF performance, the IC substrate die ground (die attach) should connect to PCB ground plane. It is strongly recommended to keep it connected.

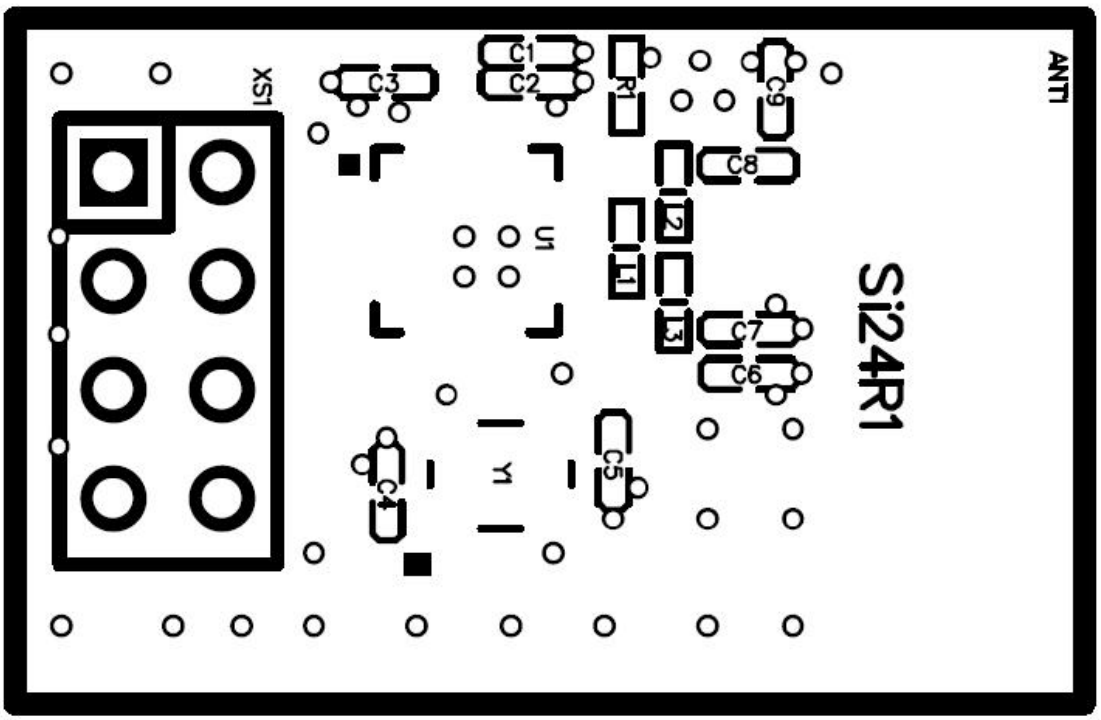


Figure 9-2 Top overlay（0402 size passive components）

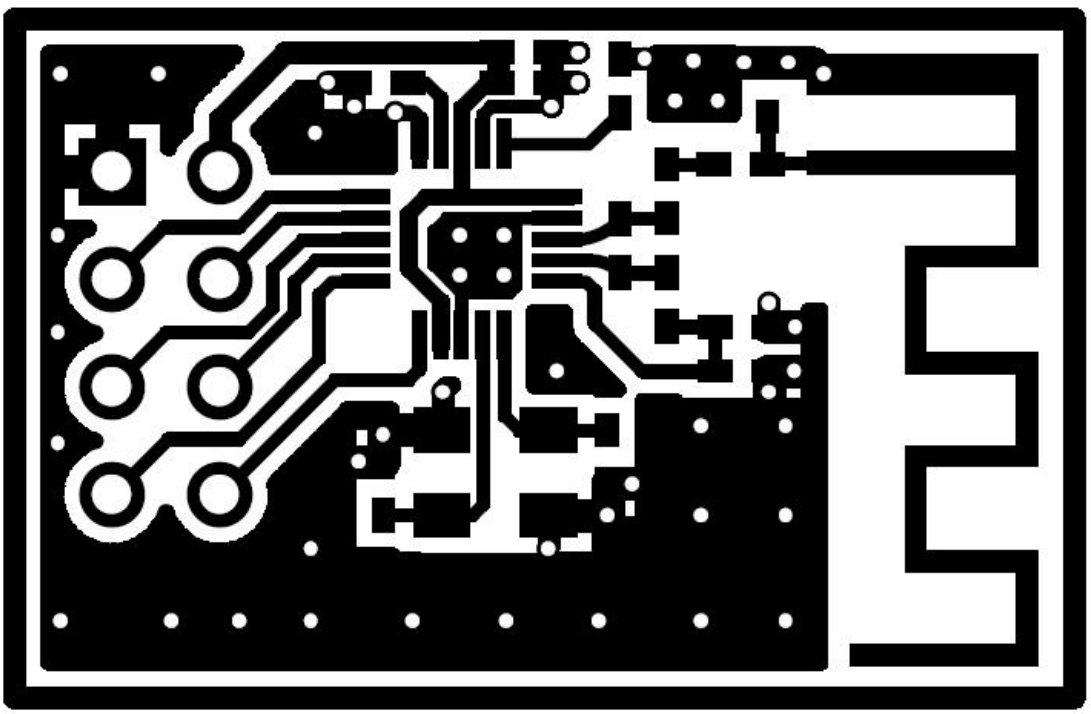


Figure 9-3 Top layer（0402 size passive components）

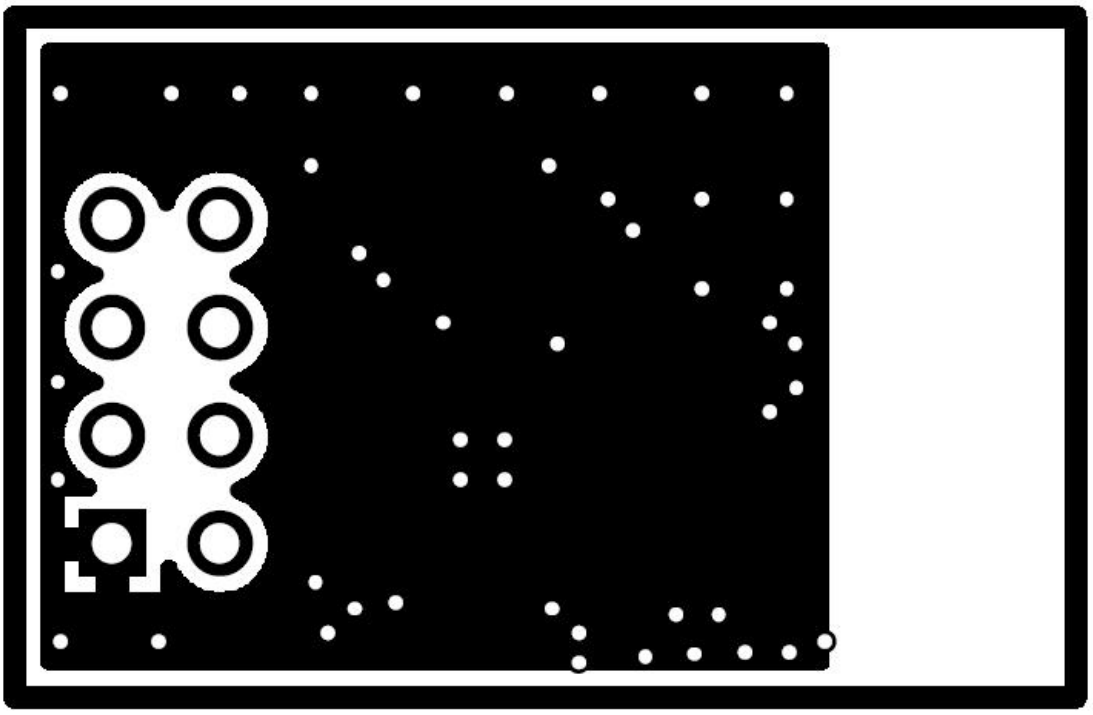


Figure 9-4 Bottom layer

10 Package Information

Package marking

Si24R1
PYYMMLL

Si24R1: chip name, fixed text

P: fixed text

YY: year number

MM: month number

LL: wafer number

order code	package	container	minimum
Si24R1-Sample	4×4mm 20-pin QFN	Box/Tube	5
Si24R1-P	4×4mm 20-pin QFN	Tray	1K
Si24R1-P	4×4mm 20-pin QFN	Tape and reel	1K

Table 10-1 Si24R1 order example

11 Contact Information

Wuxi Zhongke Microelectronic Industry Technology Research Institute Co., Ltd Technical Support Center,
Floor 9, Tower C, International Innovation Park of Chinese Sensing Networks, 200 Linghu Avenue, Wuxi,
Jiangsu, China, 214135
Phone: 86-510-85385948
Fax: 86-510-85385947
Postal Code: 214135
Email: sales-wxzk@casic.ac.cn
Website: www.wxzkme.com

Appendix A - Configuration and communication example

MODE 1: ACK MODE

PTX Configuration:

```
spi_rw_reg(SETUP_AW, 0x03);          // configure PTX address width 5 bytes
spi_write_buf(TX_ADDR, TX_ADDRESS, 5);          // write in TX address
spi_write_buf(RX_ADDR_P0, TX_ADDRESS, 5);     //address of pipe0 is the same with TX address
spi_write_buf(W_TX_PAYLOAD, buf, TX_PLOAD_WIDTH);       // write data in TX FIFO
spi_rw_reg(FEATURE, 0x04);      //Enable dynamic payload length
spi_rw_reg(DYNPD, 0x01);       //enable pipe0 dynamic payload length
spi_rw_reg(SETUP_RETR, 0x15);         //configure ARD=500us ,ARC=5
spi_rw_reg(RF_CH, 0x40);         // configure RF channel
spi_rw_reg(RF_SETUP, 0x0e);            // configure TX data rate=2Mbps,and TX power=4dbm
spi_rw_reg(CONFIG, 0x0e);           // set PWR_UP, enable CRC and CRC length is 2bytes,TX
MODE
CE = 1; // set CE , transmit data
```

PRX Configuration：

```
spi_write_buf(RX_ADDR_P0, TX_ADDRESS, 5);     // write in RX address
spi_rw_reg(EN_RXADDR, 0x01);       //Enable data pipe 0 .
spi_rw_reg(RF_CH, 0x40);         // configure RF channel
spi_rw_reg(SETUP_AW, 0x03);    // configure PRX address width:5 bytes
spi_rw_reg( FEATURE, 0x04);     //Enable dynamic payload length
spi_rw_reg(DYNPD, 0x01);      // enable pipe0 dynamic payload length
spi_rw_reg(RF_SETUP, 0x0e);     // configure TX data rate=2Mbps
spi_rw_reg(CONFIG, 0x0f);           // set PWR_UP, enable CRC and CRC length is 2bytes,RX
MODE
CE = 1; // set CE , receive data
```

MODE 2 : NOACK MODE

PTX Configuration:

```
spi_write_buf( TX_ADDR, TX_ADDRESS, 5);          // write in TX address
spi_rw_reg( FEATURE, 0x01);      // Enable W_TX_PAYLOAD_NOACK
spi_write_buf(W_TX_PAYLOAD_NOACK, buf, TX_PLOAD_WIDTH);    // write data in TX FIFO
spi_rw_reg(SETUP_AW, 0x03);          // configure PTX address width 5 bytes
spi_rw_reg( RF_CH, 0x40);          // configure RF channel
spi_rw_reg(RF_SETUP, 0x08);         // configure TX data rate=2Mbps, TX power=-12dbm
spi_rw_reg( CONFIG, 0x0e);       // set PWR_UP, enable CRC and CRC length is 2bytes,TX MODE
CE = 1; //set CE , transmit data
```

PRX Configuration：

```
spi_write_buf( RX_ADDR_P0, TX_ADDRESS, 5);    // write in RX address
spi_rw_reg( EN_RXADDR, 0x01);        // Enable data pipe 0
spi_rw_reg( RF_CH, 0x40);            // configure RF channel
spi_rw_reg( RX_PW_P0, TX_PLOAD_WIDTH);       //configure pipe 0 data length
spi_rw_reg( RF_SETUP, 0x08);        // configure TX data rate=2Mbps
spi_rw_reg( CONFIG, 0x0f);          // set PWR_UP, enable CRC and CRC length is 2bytes,RX MODE
CE = 1;      // set CE , receive data
```

MODE 3: PRX turn on multiple pipes

Dynamic length payload:

```
spi_rw_reg(FEATURE, 0x04);    //Enable dynamic payload length
spi_rw_reg(DYNPD, 0x3F) ;     //enable 6 pipes dynamic payload length
spi_rw_reg(EN_RXADDR, 0x3F);        // enable pipe 0-5 RX address
spi_rw_reg(RF_CH, 0x40);          // configure RF channel
spi_rw_reg(SETUP_AW, 0x03);    // configure PRX address width 5 bytes
spi_rw_reg(CONFIG, 0x0B);        // set PWR_UP, enable CRC and CRC length is 1bytes,RX MODE
CE = 1;
```

Static length payload:

```
spi_rw_reg(RX_PW_P0, 0x20);    //configure data length of pipe0
spi_rw_reg(RX_PW_P1, 0x20);    //configure data length of pipe1
spi_rw_reg(RX_PW_P2, 0x20);    //configure data length of pipe2
spi_rw_reg(RX_PW_P3, 0x20);    //configure data length of pipe3
spi_rw_reg(RX_PW_P4, 0x20);    //configure data length of pipe4
spi_rw_reg(RX_PW_P5, 0x20);    //configure data length of pipe5

spi_rw_reg(EN_RXADDR, 0x3F);      // enable pipe 0-5 RX address
spi_rw_reg(RF_CH, 0x40);          // configure RF channel
spi_rw_reg(SETUP_AW, 0x03);    // configure PRX address width 5 bytes
spi_rw_reg(CONFIG, 0x0F);        // set PWR_UP, enable CRC and CRC length is 2 bytes, RX MODE
CE = 1;
```