Hw4 Report

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Coding Environment:

Ubuntu(linux) 16.06

Type:

iverilog –o output *.v

vvp output

Module implementation explanation:

PC.v : render Add_PC.data_o to pc_i, and output pc_o to inst_addr.

Registers.v:render values to RS, RT, RD.

Instruction_Memory.v:receive instructions from inst_addr.

CPU.v:contain the prototype of each module.

Adder.v:add inst_addr by 4

Control.v:render corresponding values to RegDst_o, ALUOp_o, ALUSrc_o, RegWrite_o according to R-type or I-type.

ALU_Control.v:render right instructions to ALU.

Sign_Extend.v:extend 16-bits to 32-bits.

ALU.v:do corresponding instructions from ALU_Control.

MUX32.v: render corresponding values to ALU.data2_i according to either Registers.RTdata_o or Sign_Extend.data_o.

MUX5.v:render corresponding values to Registers.RDaddr_i according to either inst[20:16] or inst[15:11].