Computer Architecture, 2017 Fall

Homework 4 report
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學號：b03902129　系級：資工四　姓名：陳鵬宇

1 Coding Environment

Operating System: macOS High Sierra, version: 10.13.1

compile:
iverilog -o [output.txt][*.v]
run:
vvp [output.txt]

2 Module Implementation Explanation

We use *testbench.v* to see the output.

- **PC.v**: Read the pc_i from $Add\_PC.data\_o$ to output the pc_o to $inst\_addr$.
- **Registers.v**: Store the value and address of RS, RT and RD.
- **Instuction_Memory.v**: Get the instructions from $inst\_addr$.
- **CPU.v**: An important CPU unit states all the connections between each module.
- **Adder.v**: Simply add $data1\_i$ and $data2\_i$, then assign the value to $data\_o$.
- **Control.v**: Determine $RegDst\_o$, $ALUOp\_o$, $ALUSrc\_o$ and $RegWrite\_o$ by the 6 bits of Op_i.
- **ALU_Control.v**: Determine $ALUCtrl\_o$ by $funct\_i$ and $ALUOp\_i$.
- **Sign_Extend.v**: Get the 16 bit $data\_i$, then extend the value to 32 bit $data\_o$ according to the first bit of $data\_i$.
- **ALU.v**: Do the following operation:

$$data\_o = data1\_i[ALUCtrl\_i]data2\_i.$$

- **MUX32.v**: Choose the $data\_o$(ALU.data2_i) from $data1\_i$(Registers.RTdata_o) or $data2\_i$(Sign_Extend.data_o) according to $select\_i$(Control.ALUSrc_o).
- **MUX5.v**:
Choose the $data\_o$(Registers.RDaddr_i) from $data1$_(inst[20:16]) or $data2_i$(inst[15:11]) according to $select\_i$(Control.RegDst_o).