x86 Architecture			
Real Mode Protect Mode Virt	nal 8086 Mode Address Bu	us Data Bus PSE PAE	
8086	20-bit	16-bit	
80286 🔅 🔅	24-bit	16-bit	
i386 🔯 🕏	文 32-bit	32-bit	
Pentium * *	文 32-bit	32-bit 文	
P6 family to the	☆ 32-bit	32-bit 🛊 🛣	
AMD64 🔅 🔯	₩ 64-bit	64-Lit 🕱	
Control register			
CRO PE(bito) Protection Enable TS(bits) Task Switched	CR2 last limear address com		
WP(bit 16) Write-Protection AM(bit 18) Alignment Mask	CR3 physical address of Page		
NW(bit 29) Not Write-Through	CR4 PSE(bit4) Page Size E PAE(bit5) Physical Ad		
CD(bit 30) Cache Disable PG(bit 31) Paging			
Memory Management			
Logical Address → Linear Address → Physica	1 Address		
Segmentation Paging			
flags register			
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1	0		
N IO O D I T S Z A P F F F F F F F F F F F F F F F F F F			
1 1 1	^		
Signed C C C C 2 1			
Single-step interrupt			
CF Carry Flag A carry or borrow into the	most significant bit.		
OF Overflow Flag. The sum of two numbers		number with opposite sign.	
AF Auxiliary Flag A carry or borrow with th			
PF Parity Flag Whether the least significant		ts set	