x86 Architecture

	Real Mode	Protect Mode	Virtual 8086 Mode	Address Bus	Data Bus	4-MB Page
8086	☆			20-bit	16-bit	
80286	☆	☆		24-bit	16-bit	
80386	☆	☆	☆	32-bit	32-bit	
Pentium	☆	☆	☆	32-bit	32-bit	☆
AMD64	☆	☆	☆	64-bit	64-bit	☆
	↑ fixed segment	↑ with selector	↑ real code in protect mode			

Control Register

CR0
- PE = bit 0 — Real or Protect Mode
- TS = bit 3 — Task Switch
- PG = bit 31 — Paging

CR2 — last linear address caused page fault

CR3 — physical address of Page Directory Base
↑ PDBR

CR4
- PSE = bit 4 — Page Size Extensions
- PAE = bit 5 — Physical Address Extensions

Addressing Mode

Logical Address → Linear Address → Physical Address
- ↑ Segmentation
- ↑ Paging (PG)