x86 Architecture

	Real Mode	Protect Mode	Virtual 8086 Mode	Address Bus	Data Bus	PSE	PAE
8086	☆			20-bit	16-bit		
80286	☆	☆		24-bit	16-bit		
i386	☆	☆	☆	32-bit	32-bit		
Pentium	☆	☆	☆	32-bit	32-bit	☆	
P6 family	☆	☆	☆	32-bit	32-bit	☆	☆
AMD64	☆	☆	☆	64-bit	64-bit	☆	

Control register

CR0
- PE (bit 0) Protect Mode Enable
- TS (bit 3) Task Switched
- WP (bit 16) Write-Protection
- AM (bit 18) Alignment Mask
- NW (bit 29) Not Write-Through
- CD (bit 30) Cache Disable
- PG (bit 31) Paging

CR2 last linear address caused a page fault

CR3 physical address of Page Directory Base

CR4
- PSE (bit 4) Page Size Extension
- PAE (bit 5) Physical Address Extension

Memory Management

Logical Address → Linear Address → Physical Address
                  ↑   ↑
              Segmentation   Paging

flags register

```
 15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0
 ┌──┬──┬──┬──┬──┬──┬──┬──┬──┬──┬──┬──┬──┬──┬──┬──┐
 │  │ N│ IO│ O│ D│ I│ T│ S│ Z│  │ A│  │ P│  │ C│
 │  │ T│ PL│ F│ F│ F│ F│ F│ F│  │ F│  │ F│  │ F│
 └──┴──┴──┴──┴──┴──┴──┴──┴──┴──┴──┴──┴──┴──┴──┴──┘
```
← Unsigned

Signed

Single-step interrupt

C3   C2 C1 C0
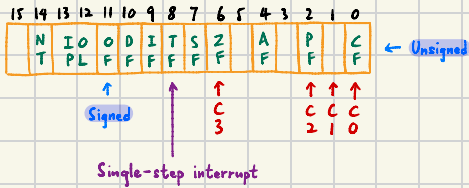
CF   Carry Flag   A carry or borrow into the most significant bit.

OF   Overflow Flag   The sum of two numbers with the same sign yields a number with opposite sign.

AF   Auxiliary Flag A carry or borrow with the least significant nibble.

PF   Parity Flag   Whether the least significant byte contains even number of bits set.