x86 Architecture

	Real Mode	Protect Mode	Virtual 8086 Mode	Address Bus	Data Bus	4-MB Page
8086	★			20-bit	16-bit	
80286	★	★		24-bit	16-bit	
80386	★	★	★	32-bit	32-bit	
Pentium	★	★	★	32-bit	32-bit	★
AMD64	★	★	★	64-bit	64-bit	★

↑ (Real Mode) fixed Segment

↑ (Protect Mode) with Selector

↑ (Virtual 8086 Mode) real code in protect mode

Control Register

CR0
- PE = bit 0 — Real or Protect Mode
- TS = bit 3 — Task Switch
- PG = bit 31 — Paging

CR4
- PSE = bit 4 — Page Size Extensions
- PAE = bit 5 — Physical Address Extensions

CR2 — last linear address caused page fault

CR3 — physical address of Page Directory Base
↑
PDBR

Memory Management

Logical Address → Linear Address → Physical Address
- ↑ Segmentation
- ↑ Paging (PG)

flags register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				OF	DF	IF	TF	SF	ZF		AF		PF		CF

← Unsigned

↑ Signed

Single-step interrupt

C3, C2, C0
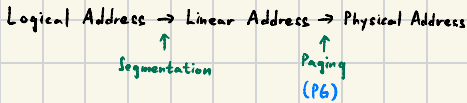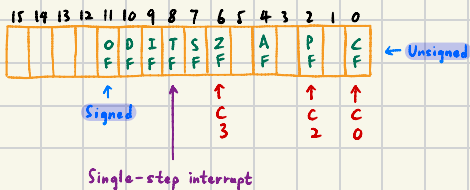
CF	Carry Flag	A carry or borrow into the most significant bit.
OF	Overflow Flag	The sum of two numbers with the same sign bits yields a number with opposite sign bit.
AF	Auxiliary Flag	A carry or borrow with the least significant nibble.
PF	Parity Flag	Whether the least significant byte contains even number of bits set.