Advanced Programming CPU/GPU using SYCL

Soner Steiner

Intel certified oneAPI Instructor VSC

intel.

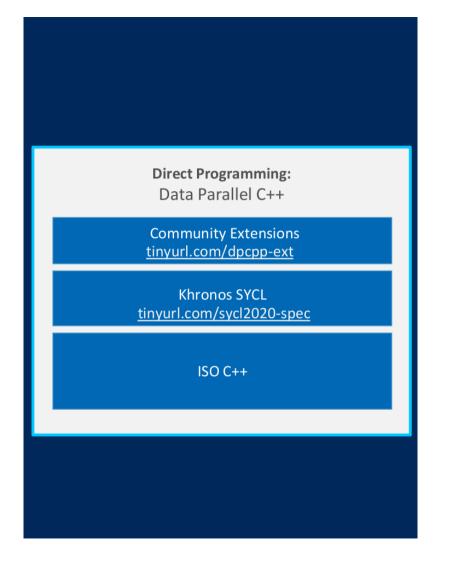
Overview

- Introduction
- Remainder of the lambda functions
- Compilation and run
- Queues and device selectors
- Manage the data transfer
 Buffers and Unified Shared Memory
- Basic parallel kernels
- ND-Range kernels
- Sub-groups

Data Parallel C++

• Standard-based, Cross-architecture Language

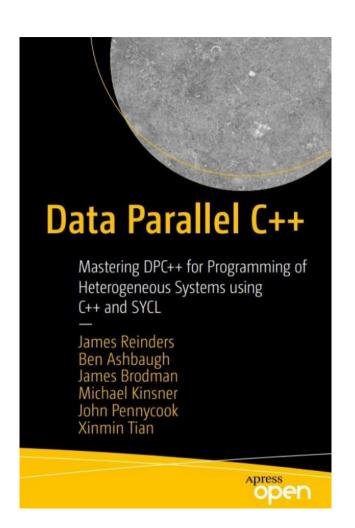
http://tinyurl.com/sycl2020-support-in-dpcpp



Many of the source examples are from Book:

Source code accessible from \$ oneapi-cl

```
Chapter 01 - Introduction
-Chapter 02 - Where Code Executes
-Chapter 03 - Data Management
-Chapter 04 - Expresssing Parallelism
-Chapter 05 - Error Handling
-Chapter 06 - Unified Shared Memory
-Chapter 07 - Buffers
-Chapter 08 - Scheduling Kernals and Data Movement
-Chapter 09 - Communication and Synchronization
-Chapter 10 - Defining Kernels
-Chapter 11 - Vectors
-Chapter 12 - Device Information
-Chapter 13 - Practical Tips
-Chapter 14 - Common Parallel Patterns
-Chapter 15 - Programming for GPUs
-Chapter 16 - Programming for CPUs
-Chapter 17 - Programming for FPGA
-Chapter 18 - Libraries
-Chapter 19 - Memory Model and Atomics
Chapter 20 - Epiloque Future Direction
```



Anatomy of a SYCL Application

```
#include <sycl.hpp>
using namespace sycl;
int main() {
std::vector<float> A(1024, 1.0f), B(1024, 2.0f), C(1024);
                                                                       Host code
      buffer bufA {A}, bufB {B}, bufC {C};
      queue q;
      q.submit([&](handler &h) {
          auto A = bufA.get_access(h, read_only);
          auto B = bufB.get_access(h, read_only);
          auto C = bufC.get_access(h, write_only);
          h.parallel_for(1024, [=](auto i){
                                                                      Accelerator
              C[i] = A[i] + B[i];
                                                                      device code
          });
      });
for (int i = 0; i < 1024; i++)
                                                                       Host code
       std::cout << "C[" << i << "] = " << C[i] << std::endl;</pre>
}
```

VSC WS 2013, Vienna

Anatomy of a SYCL Application

```
#include <sycl.hpp>
using namespace sycl;
int main() {
std::vector<float> A(1024, 1.0f), B(1024, 2.0f), C(1024);
                                                                      Application scope
      buffer bufA {A}, bufB {B}, bufC {C};
      queue q;
      q.submit([&](handler &h) {
          auto A = bufA.get_access(h, read_only);
                                                                      Command group
          auto B = bufB.get_access(h, read_only);
          auto C = bufC.get_access(h, write_only);
                                                                            scope
          h.parallel_for(1024, [=](auto i){
              C[i] = A[i] + B[i];
                                                                       Device scope
          });
      });
for (int i = 0; i < 1024; i++)
       std::cout << "C[" << i << "] = " << C[i] << std::endl;</pre>
                                                                       Application scope
```

Lambda-functions ... Lambdas

```
□q.parallel for(N, [=](auto i)
39
40
41
         a[i] -= 2;
42
             mutable throw()
         return n:
```

- 1. capture clause
- 2. parameter list optional
- 3. mutable specification optional
- 4. exceptionspecification optional
- 5. trailing-returntype optional
- 6. lambda body
 - [=] : capture by value
 - [&] : capture by reference

https://learn.microsoft.com/en-us/cpp/cpp/lambda-expressions-in-cpp

Kernel Code

Kernel Code
Cannot use
these features



- Run Asynchronously
- Limitation on what kind of C++ code
 - Dynamic Polymorphism
 - Dynamic memory allocations
 - Static variables
 - Function pointers
 - Runtime Type Informatoion (RTTI)
 - Exception Handling
 - Recursion

Where Code Executes

QueuesDevice Selectors

The queue class

Actions are submitted to a queue for execution on a single device

Always bound to a single device

 Several queues can point to the same device



Choosing Devices: Five use cases:

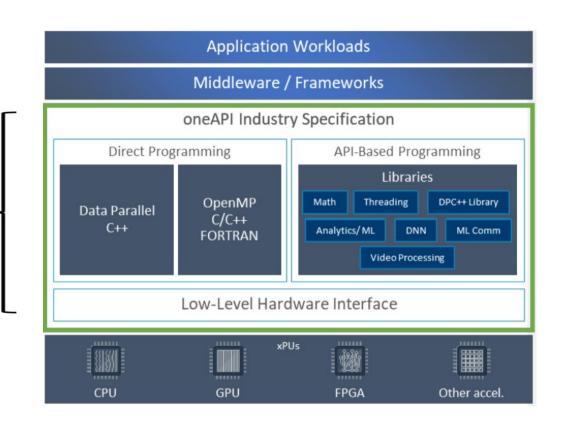
#	Methods	Comments	
1	Anywhere (don't care where)	Runtime chooses	
2	Always on Host	Good for debugging	
3	GPU or Accelerator		
4	Heterogeneous set of devices		
5	Specific Class of device	e.g. FPGA	

Actions

Work Type	Actions (handler class methods)	Summary
	single_task	Execute a single instance of a device function.
Device code execution	parallel_for	Multiple forms are available to launch device code with different combinations of work sizes.
	parallel_for_work_group	Launch a kernel using hierarchical parallelism, described in Chapter 4.
Explicit memory	сору	Copy data between locations specified by accessor, pointer, and/or shared_ptr. The copy occurs as part of the DAG, including dependence tracking.
operation	update_host	Trigger update of host data backing of a buffer object.
	fill	Initialize data in a buffer to a specified value.

Programmers' perspective: Three things to consider

- 1. Offload the code to device
- 2.Manage the transfer of Data
- 3.Implement Parallelism

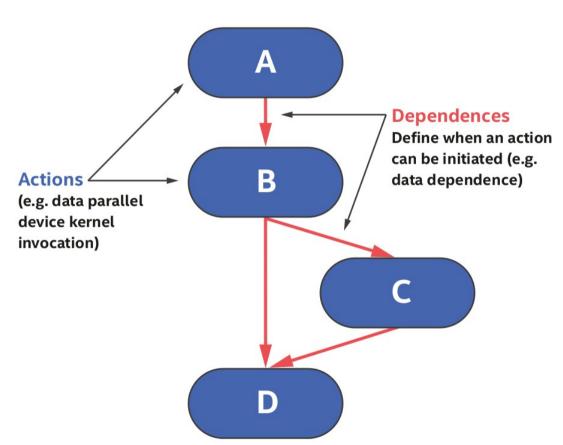


Memory Models

• Buffer Memory Model – abstract view of memory that can be local to the host or a device, and is accessible via accessors.

- Unified Shared Memory (USM)- pointer-based approach for memory model that os familiar for C++ programmers.
- Images: a special type of buffer that has an extra functionality specific to image processing

Task Graphs (Directed Acyclic Graph)



- Dependency resolution and node execution are controlled by the runtime
- Dependencies
 determine the order
 that kernels are
 executed in

 Dependencies can be explicit or implicit

Explicit Dependencies Using Events

```
constexpr int N = 101;
int main()
   queue q;
   int *data = malloc shared<int>(N, q);
   auto e = q.parallel for(N, [=] (id<1> i) { data[i] = i ;} );
   q.submit( [&] (handler &h)
       h.depends on(e);
       h.single task([=] ()
                for(int i = 1; i < N; ++i)
                    data[0] += data[i];
           } );
   q.wait();
   std::cout << "printing sum after computation \n" ;</pre>
   std::cout << data[0] << " ";</pre>
   std::cout << "\n" ;
}
```

 Create event to initialize the data in kernel1

 Kernel2 sums up the elements

• 5050

Buffer Memory Model

Buffers encapsulate data shared between host and device

Accessors provide access to data stored in buffers and create data dependencies in the graph.

Unified Shared Memory (USM)

provides an alternative pointer-based mechanism for managing memory

```
queue q:
std::vector<int> v(N, 3);
    buffer buf(v);
    q.submit( [&] (handler& h)
        accessor a(buf, h, write only);
        h.parallel for(N, [=] (auto i) { a[i] = i; } );
     } );
for (int i = 0; i < N; i++) std::cout << v[i] << " ";
```

Buffer Creation - two approaches

 Construct a new buffer using sycl::range to specify the size, data will not be initialized!

Create buffer from existing data, data will be copied!
 Buffer(T, hostData,
 const sycl::range<dimensions> &bufferRange,

const sycl::property list &proplist={});

Examples of Buffer Creation

```
Buffer for vectors
buffer b1{v};
buffer b2{v.begin(), v.end()};
// create a buffer of ints from std:array
std::array<int, 42> data;
                                                                 Buffer for std::array
buffer b3{data};
 // create a buffer of 5 doubles and initialize it from
// a host pointer
double dd[5] = {1.1, 2.2, 3.14, 4.4, 5.5};
                                                                Buffer from a host pointer
buffer b4{dd, range{5} };
std::cout << "printing v before computation \n" ;</pre>
for (int i = 0; i < N; i++) std::cout << v[i] << " ";
std::cout << "\n" ;
```

Accessors

Only means of accessing data in Buffers!

They create the dependencies for the runtime.

Accessor Modes

Access Mode	Description
read_only	Read only Access
write_only	Write-only accessor Previous Contents not discarded
read_write	Read and Write access

Code Walkthrough

```
#include <CL/sycl.hpp>
using namespace sycl;
int main() {
std::vector<float> A(1024, 1.0f), B(1024, 2.0f), C(1024);
      buffer bufA {A}, bufB {B}, bufC {C};
      queue q;
      q.submit([&](handler &h) {
          auto A = bufA.get access(h, read only);
          auto B = bufB.get access(h, read only);
          auto C = bufC.get access(h, write only);
          h.parallel for(1024, [=](auto i){
              C[i] = A[i] \uparrow + B[i];
          });
      });
```

Host Accessor (up to now our accessors have been in the command group)

- The Host Accessor is an accessor which uses host buffer access target.
- Host accessors make data available for access on the host.
- They synchronize with the host by defining a new dependence between the currently accessing graph and the host.
- Creating host accessor is a blocking call.

Some Dependency Patterns

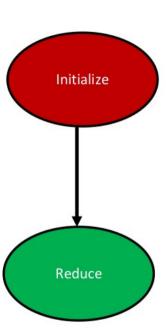
Linear Dependence Using In-order queue

Create In-order queue

Initialize the data in Kernel 1

Kernel 2 sums up the elements

```
constexpr int N=42;
int main()
    queue Q{property::queue::in order()};
    int *data = malloc shared<int>(N,Q);
    Q.parallel for(N, [=](id<1>i) { data[i] = 1; });
    Q.single task([=]()
        for(int i=1; i < N; ++i)
            data[0] += data[i];
      });
    Q.wait();
    assert(data[0] == N);
    for(int i = 0; i < N; ++i)
        std::cout << data[i] << " ":</pre>
    std::cout << "\n";</pre>
    return 0;
```

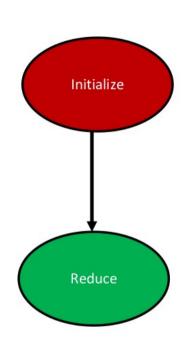


Linear Dependence Using Buffers and Accessors

Use Buffers and Accessors to Initialize the data in Kernel1

Kernel 2 sums up the elements

```
constexpr int N=101;
int main()
  queue q;
  buffer <int> data{ range{N} };
  q.submit( [&] (handler &h)
       accessor a{data, h};
       h.parallel for(N, [=] (id<1> i) { a[i] = i; } );
     } );
  q.submit( [&] (handler &h)
      accessor a{data, h};
      h.single task([=] ()
           for(int i = 1; i < N; ++i)
               a[0] += a[i];
       } );
     } );
  host accessor h a{data};
   std::cout << h a[0] << "\n";</pre>
   return 0;
```



5050

IT4I WS 2013 intel.

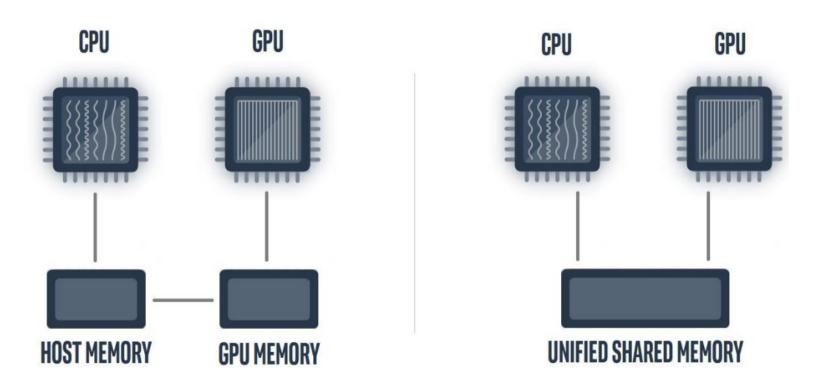
Unified shared memory (USM)

USM provides a pointer-based alternative in SYCL

- Simplifies porting to an accelerator
- Gives programmers the desired level of control
- Complementary to buffers

Developer View of USM

Developers can reference the same memory object in host and device code with USM



Unified shared memory (USM)

USM provides both explicit and implicit models for managing memory.

Allocation Type	Description	Accessible on HOST	Accessible on DEVICE
device	Allocations in device memory (explicit)	NO	YES
host	Allocations in host memory (implicit)	YES	YES
shared	Allocations can migrate between host and device memory	YES	YES
	(implicit)		

Automatic data accessibility and explicit data movement supported.

USM - Explicit Data Movement

```
queue q;
int hostArray[N];
                                                                 malloc device
int *deviceArray = (int*) malloc device(N * sizeof(int), q);
for(int i = 0; i < N; ++i) hostArray[i] = i;
// copy hostArray tp deviceArray
                                                                  mem copy
q.memcpy(deviceArray, &hostArray[0], N*sizeof(int));
q.wait();
q.submit( [&] (handler &h)
   h.parallel for(N, [=] (auto ID)
           deviceArray[ID] = ID*ID ;
       });
 q.wait();
//copy deviceArray back to hostArray
q.memcpy(&hostArray[0], deviceArray, N*sizeof(int));
                                                                       mem copy
q.wait();
free(deviceArray, q);
```

USM - Implicit Data Movement

```
queue q;
int *hostArray = (int*) malloc host(N * sizeof(int), q);;
int *sharedArray = (int*) malloc shared(N * sizeof(int), q);
for(int i = 0; i < N; ++i) hostArray[i] = i;
q.submit( [&] (handler &h)
    h.parallel for(N, [=] (auto ID)
            sharedArray[ID] = hostArray[ID] * hostArray[ID];
       });
 } );
  q.wait();
for (int i = 0; i < N; i++) hostArray[i] = sharedArray[i] ;</pre>
free(hostArray, q);
free(sharedArray, q);
```

malloc_host malloc_shared

No accessors in USM

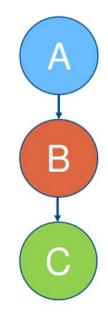
Dependences must be specified explicitly using events

- queue.wait()
- wait on event objects
- use the depens_on method inside a command group

```
queue q;
int *data = (int*) malloc shared(N * sizeof(int), g);
for(int i = 0; i < N; ++i) data[i] = i;
q.submit( [&] (handler &h)
    h.parallel for<class taskA>(range<1> (N), [=] (id<1> i)
            data[i] += 1;
  } );
q.wait();
q.submit([&] (handler &h)
    h.parallel for<class taskB>(range<1> (N), [=] (id<1> i)
            data[i] += 2;
        } );
  } );
q.wait();
g.submit([&] (handler &h)
    h.parallel for<class taskC>(range<1> (N), [=] (id<1> i)
            data[i] += 3:
        } );
  } );
q.wait();
for (int i = 0; i < N; i++) std::cout << data[i] << " ";</pre>
free(data, q);
```

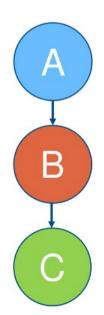
Explicit wait() used to ensure Data dependency is maintained

wait() will block execution on host



```
queue a:
int* data = malloc shared<int>(N, q);
for(int i = 0; i < N; ++i) data[i] = i;
auto e1 = q.submit( [&] (handler &h)
    h.parallel for<class taskA>(range<1> (N), [=] (id<1> i)
            data[i] += 1;
  } );
  auto e2 = q.submit( [&] (handler &h)
    h.depends on(e1):
    h.parallel for<class taskB>(range<1> (N), [=] (id<1> i)
            data[i] += 2;
  } );
// non-blocking: execution of host code is possible
g.submit( [&] (handler &h)
    h.depends on(e2):
    h.parallel for<class taskC>(range<1> (N), [=] (id<1> i)
            data[i] += 3;
  } );
  q.wait();
std::cout << "printing data after computation \n" ;</pre>
for (int i = 0; i < N; i++) std::cout << data[i] << " ";</pre>
free(data, q);
```

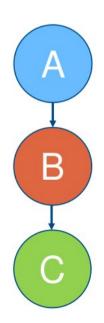
use depends_on method to let command group handler know that specified event should be complete before specified task can execute.



```
queue q{property::queue::in order()};
int* data = malloc shared<int>(N, q);
for(int i = 0; i < N; ++i) data[i] = i;
g.submit( [&] (handler &h)
    h.parallel for<class taskA>(range<1> (N), [=] (id<1> i)
            data[i] += 1;
q.submit([&] (handler &h)
    h.parallel for<class taskB>(range<1> (N), [=] (id<1> i)
            data[i] += 2;
  } );
q.submit([&] (handler &h)
    h.parallel for<class taskC>(range<1> (N), [=] (id<1> i)
            data[i] += 3;
  } );
q.wait();
free(data, q);
```

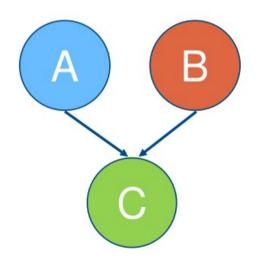
use in_queue property for the queue

Execution will not overlap even
If the queues have no data dependency



```
queue q;
int *data1 = (int*) malloc shared(N * sizeof(int), q);
int *data2 = (int*) malloc shared(N * sizeof(int), q);
for(int i = 0; i < N; ++i){ data1[i] = 10; data2[i] = 20;}
auto e1 = q.submit( [&] (handler &h)
    h.parallel for<class taskA>(range<1> (N), [=] (id<1> i)
            data1[i] += 1;
       } );
  } ):
auto e2 = q.submit( [&] (handler &h)
    h.parallel for<class taskB>(range<1> (N), [=] (id<1> i)
            data2[i] += 2;
       } );
 } ):
q.submit( [&] (handler &h)
   h.depends on({e1, e2}):
    h.parallel for<class taskC>(range<1> (N), [=] (id<1> i)
            data1[i] += data2[i];
       } );
 q.wait(
for (int 1 = 0; i < N; i++) std::cout << data1[i] << " ";
free(data1, q); free(data2, q);
```

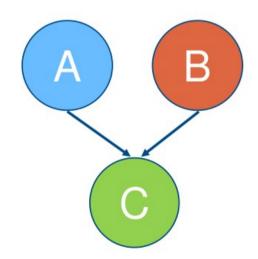
use depends_on() method to let command group handler know that specified events should be complete before specified tasks can execute.



USM - Data Dependency in Queues

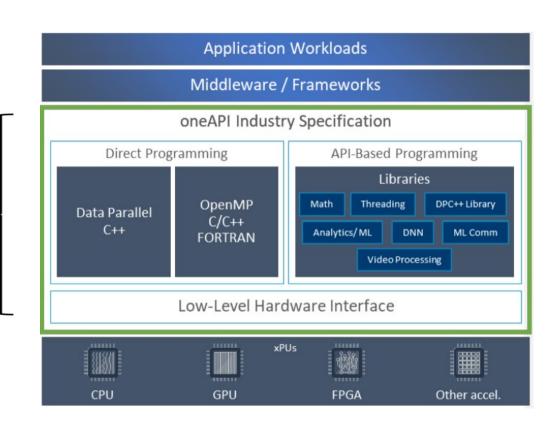
```
queue q;
int* data1 = malloc shared<int>(N, q);
int* data2 = malloc shared<int>(N, q);
for(int i = 0; i < N; ++i){ data1[i] = 10; data2[i] = 20;}
auto e1 = q.parallel for<class taskA>(range<1> (N), [=] (id<1> i)
            data1[i] += 1;
auto e2 = q.parallel for<class taskB>(range<1> (N), [=] (id<1> i)
            data2[i] += 2;
q.parallel for<class taskC>(range<1> (N), \{e1, e2\}, [=] (id<1> i)
            data1[i] += data2[i];
 q.wait(
free(data1, q); free(data2, q);
```

A more simplified way of specifying dependency as parameter of parallel_for



Programmers' perspective: Three things to consider

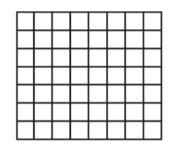
- 1. Offload the code to device
- 2.Manage the transfer of Data
- 3.Implement Parallelism

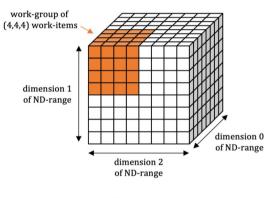


Three forms of Parallel Kernels

Basic Parallel Kernels

ND-range Parallel Kernels





ND-Range

Hierarchical Parallel Kernels ('Experimental alternative syntax')

- Parallel kernel allows multiple instances of an operation to execute in parallel.
- Useful to offload parallel execution of a basic for-loop in which each iteration is completely independent and in any order.
- Parallel kernels are expressed using the parallel_for function.
- Up to the programmer to handle/confirm that there are no dependencies.

for-loop in CPU application

Offload to a accelerator using parallel_for

```
for(int i = 0; i < N; ++i)
{
    c[i] = a[i] + c[i] ;
}</pre>
```

```
h.parallel_for(range<1>(N), [=](id<1> i)
{
    C[i] = A[i] + B[i];
});
```

The functionality of basic parallel kernels is exposed via range, id and item classes

- range class is used to describe the iteration space of parallel execution
- id class is used to index an individual instance of a kernel in a parallel execution

```
h.parallel_for(range<1>(N), [=](id<1> idx)
{
    //CODE THAT RUNS ON DEVICE
});
```

The functionality of basic parallel kernels is exposed via range, id and item classes

- range class is used to describe the iteration space of parallel execution
- id class is used to index an individual instance of a kernel in a parallel execution
- item class represents an individual instance of a kernel function, exposes additional functions to query properties of the execution range

```
h.parallel_for(range<1>(N), [=](id<1> idx)
{
    //CODE THAT RUNS ON DEVICE
});
```

```
h.parallel_for(range<1>(N)) [=] (item<1> item)
{
    auto idx = item.get_id();
    auto R = item.get_range();
    //CODE THAT RUNS ON DEVICE
});
```

The functionality of basic parallel kernels is exposed via range, id and item classes

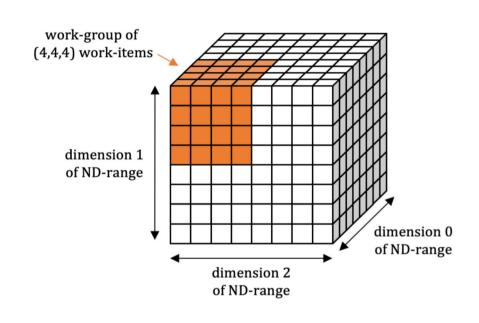
- Dimensionality
 <1>, <2> or <3>
 is templated and must be declared at COMPILE time
- Size is dynamic passed to constructor at runtime

```
h.parallel_for(range<1>N), [=](id<1>idx)
{
    //CODE THAT RUNS ON DEVICE
});
```

```
h.parallel_for(range<1>[N)] [=](item<1> item)
{
    auto idx = item.get_id();
    auto R = item.get_range();
    //CODE THAT RUNS ON DEVICE
});
```

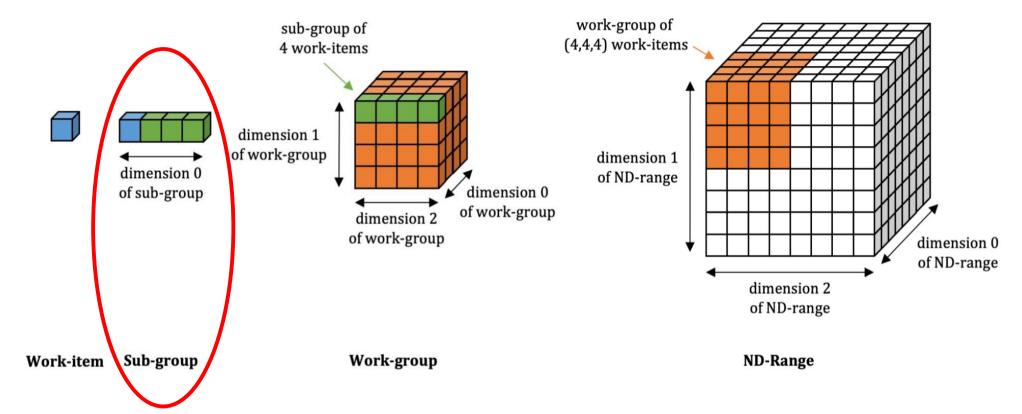
ND-range Kernels

- ND-range kernels enable low level performance tuning by providing access to local memory and mapping executions to compute units on hardware.
- The entire iteration space is divided into smaller groups called work-groups, work-items within a work-group are scheduled on a single compute unit on hardware.
- The grouping of kernel executions into work-groups will allow control of resource usage and load balance work distribution.



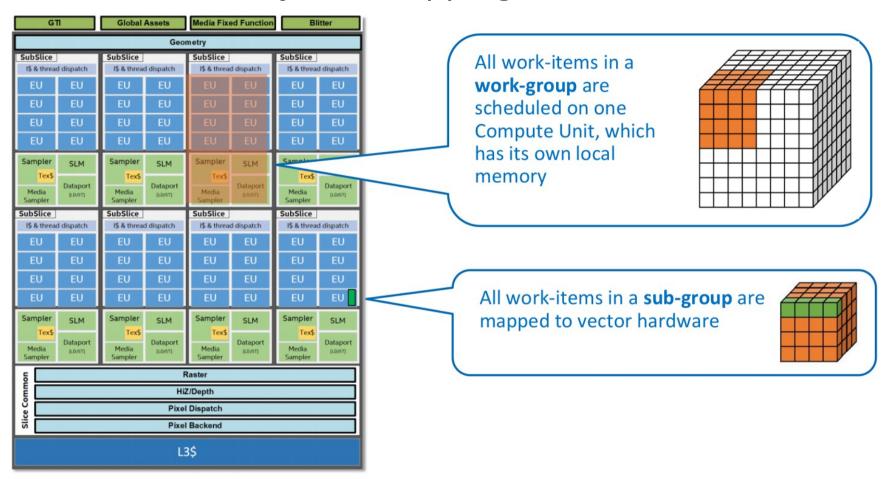
ND-Range

SYCL Thread Hierarchy and Mapping



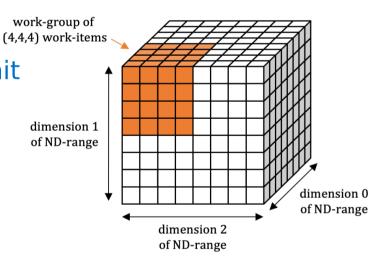
Covered later

SYLC Thread Hierarchy and Mapping



ND-range Kernels

- Basic Parallel Kernels are easy way to parallelize a for-loop but does not allow performance optimization at hardware level.
- ND-range kernel is another way to express parallelism which enable low level performance tuning by providing access to local memory and mapping executions compute units on hardware.
 - The entire iteration space is divided into smaller
 groups called work-groups, work-items within a
 work-group are scheduled on a single compute unit
 on hardware.
 - The grouping of kernel executions into workgroups will allow control of resource usage and load balance work distribution.



ND-Range

ND-range Kernels

The functionality of nd_range kernels is exposed via nd_range and nd_item classes

nd_range class represents a grouped execution range using global execution range and the local execution range of each work-group.

nd_item class represents an individual instance of a kernel function and allows to query for work-group range and index.

Understand how Sub-Groups map to GPU hardware

Understand how using Sub-Groups shuffle operations can achieve better performance and avoid repeated global memory access

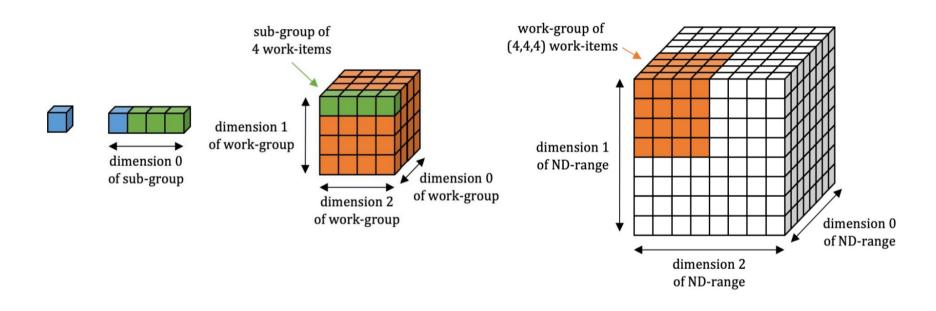
Write a SYCL program using Sub-Group and group algorithms to accomplish computation

Sub-groups are a subset of the work-items that are executed Simultaneously or with additional scheduling guerantees.

Leveraging sub-groups will help to map execution to low level hardware and may help in achieving higher performance.

Work-item

Sub-group



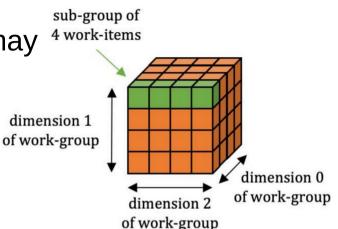
VSC WS 2013, Vienna intel. 52

ND-Range

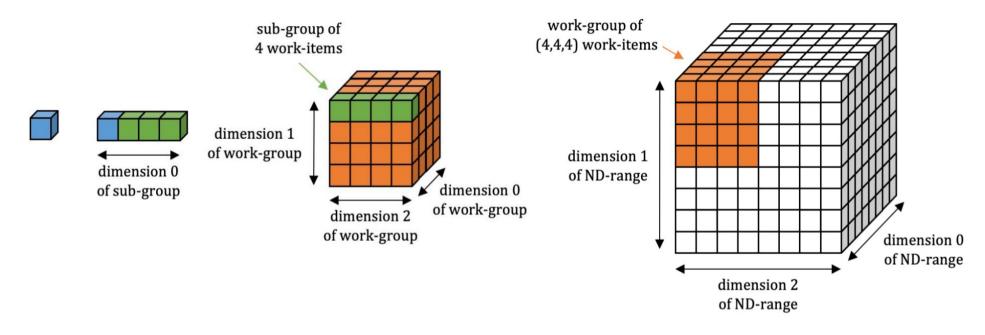
Work-group

 A subset of work-items withing a work-group that may map to vector hardware.

- Why use sub-groups?
 - Work-items in a sub_group can communicate directly using shuffle operations
 - Work-items in a sub_group can synchronize using sub_group barriers and guarantee memory consistency using sub_group memory fences
 - Work-items in a sub_group have access to sub_group collectives, providing fast implementations of common parallel patterns.



- Sub-group = subset of work-items withing a work-group
- Parallel execution with ND-RANGE kernel helps to get access to work-group and sub-group



Work-item Sub-group Work-group ND-Range

```
h.parallel_for(nd_range<1>(N,B), [=](nd_item<1> item)
{
    auto sg = item.get_sub_group();
    // KERNEL CODE
});
```

sub_group class

 The sub-group handle can be obtained from the nd_item using the get_sub_group().

- Once you have the sub-group handle, you can query for more information about the subgroup, do shuffle operations or use collective functions.
- Explicit kernel attribute
 [[intel::reqd_sub_group_size(N)]]
 to control the sub-group size

The sub-group handle can be quired to get other information:

- get_local_id() returns the index of the work-item within its subgroup
- get_local_range() returns the size of sub_group
- get_group_id() returns the index of the sub-group
- get_group_range() returns the number of sub-groups within the parent work-group

```
h.parallel_for(nd_range<1>(N,B), [=](nd_item<1> item){
         auto sg = item.get_sub_group();
        if(sg.get_local_id() == 0){
            out << "sub_group id: " << sg.get_group_id()[0]</pre>
                << " of " << sg.get_group_range()
                << ", size=" << sg.get_local_range()[0]
                                          << endl;
});
```

```
sub_group id: 1 of 4, size=16
sub_group id: 3 of 4, size=16
sub_group id: 2 of 4, size=16
sub_group id: 0 of 4, size=16
```

Sub-group Shuffles

- One of the most useful features of sub-groups is the ability to communicate directly between individual work-items without explicit memory operations.
- Shuffle operations enable us to remove work-group local memory usage from our kernels and/or to avoid unnecessary repeated accesses to global memory.

```
h.parallel_for(nd_range<1>(N,B), [=](nd_item<1> item){
               sg = item.get_sub_group();
        auto
        size t i = item.get global id(0);
        /* Shuffles */
        //data[i] = sg.shuffle(data[i], 2);
        //data[i] = sg.shuffle_up(0, data[i], 1);
        //data[i] = sg.shuffle_down(data[i], 0, 1);
        data[i] = sg.shuffle_xor(data[i], 1);
});
```

```
x: 0 1 2 3 4 5 6 7

mask: 1 1 1 1 1 1 1 1 1

shuffle_xor(x, mask): 1 0 3 2 5 4 7 6
```

Sub-group Collectives

- The collective functions provide implementations of closely- related common parallel patterns.
- Providing these implementations as library functions increases developer productivity and gives implementations the ability to generate highly optimized code for individual target devices.

```
h.parallel_for(nd_range<1>(N,B), [=](nd_item<1> item){
        auto sg = item.get_sub_group();
        size_t i = item.get_global_id(0);
        /* Collectives */
        data[i] = reduce(sg, data[i],
                                         plus<>())
        //data[i] = reduce(sg, data[i], std::maximum<>());
        //data[i] = reduce(sq, data[i], std::minimum<>());
});
```

Useful Links

Open source projects

oneAPI Data Parallel C++ compiler: github.com/intel/llvm

Graphics Compute Runtime: Graphics github.com/intel/compute-runtime

Compiler: <u>github.com/intel/intel-graphics-compiler</u>

SYCL 2020:

tinyurl.com/sycl2020-spec

DPC++ Extensions: <u>tinyurl.com/dpcpp-ext</u>

Environment Variables: <u>tinyurl.com/dpcpp-env-vars</u>

DPC++ book: <u>tinyurl.com/dpcpp-book</u>

SYCL Academy <u>github.com/codeplaysoftware/sycla</u> cademy/tree/main

Code samples:

github.com/intel/llvm/tree/sycl/sycl/test github.com/intel/llvm/tree/sycl/sycl/test-e2e github.com/oneapi-src/oneAPI-samples

Notices and Disclaimers

- Performance varies by use, configuration and other factors. Learn more at <u>www.Intel.com/PerformanceIndex</u>
- Performance results are based on testing as of dates shown in configurations and may not reflect all publicly available updates. See backup for configuration details. No product or component can be absolutely secure.
- You may not use or facilitate the use of this document in connection with any infringement or other legal analysis concerning Intel products described herein. You agree to grant Intel a non-exclusive, royalty-free license to any patent claim thereafter drafted which includes subject matter disclosed herein.
- The products described may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.
- No license (express or implied, by estoppel or otherwise) to any intellectual property rights is granted by this
 document, with the sole exception that a) you may publish an unmodified copy and b) code included in this
 document is licensed subject to the Zero-Clause BSD open source license (0BSD),
 https://opensource.org/licenses/0BSD. You may create software implementations based on this document and in
 compliance with the foregoing that are intended to execute on the Intel product(s) referenced in this document. No
 rights are granted to create modifications or derivatives of this document.
- No license (express or implied, by estoppel or otherwise) to any intellectual property rights is granted by this document, with the sole exception that code included in this document is licensed subject to the Zero-Clause BSD open source license (OBSD), http://opensource.org/licenses/0BSD.
- No license (express or implied, by estoppel or otherwise) to any intellectual property rights is granted by this
 document.
- Code names are used by Intel to identify products, technologies, or services that are in development and not publicly available. These are not "commercial" names and not intended to function as trademarks.
- © Intel Corporation. Intel, the Intel logo, and other Intel marks are trademarks of Intel Corporation or its subsidiaries. Other names and brands may be claimed as the property of others.

Back Up Details about Intel® oneAPI Toolkits

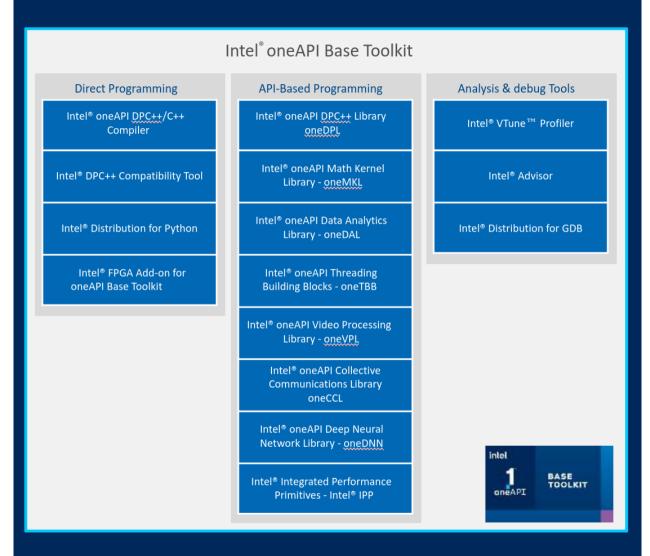
Intel® oneAPI Base Toolkit

Accelerate Data-centric Workloads

A core set of core tools and libraries for developing high-performance applications on Intel® CPUs, GPUs, and FPGAs.

Who Uses It?

- A broad range of developers across industries
- Add-on toolkit users since this is the base for all toolkits



Intel® oneAPI Base Toolkit

Accelerate Data-centric Workloads

Top Features/Benefits

- Data Parallel C++ compiler, library and analysis tools
- SYCLomatic / DPC++ Compatibility tool helps migrate CUDA code to C++ with SYCL
- Python distribution includes accelerated scikit-learn, NumPy, SciPy libraries
- Optimized performance libraries for threading, math, data analytics, deep learning, and video/image/signal processing

Learn More

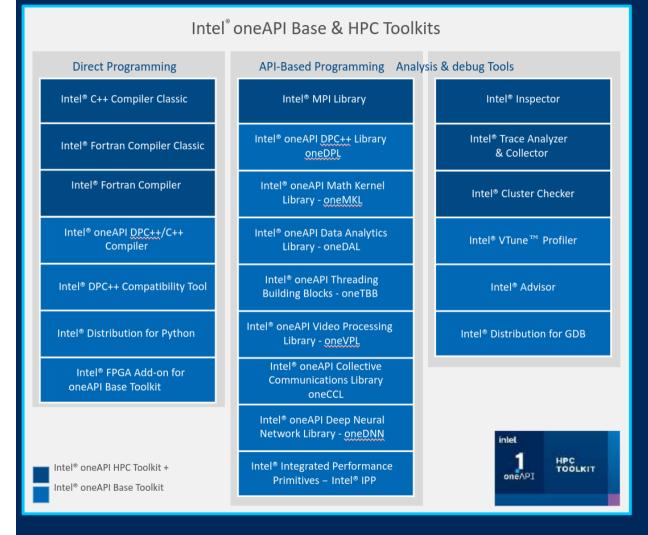
Intel® oneAPI HPC Toolkit

Accelerate Data-centric Workloads

A core set of core tools and libraries for developing high-performance applications on Intel® CPUs, GPUs, and FPGAs.

Who Uses It?

- A broad range of developers across industries
- Add-on toolkit users since this is the base for all toolkits



Intel® oneAPI HPC Toolkit

Accelerate Data-centric Workloads

Top Features/Benefits

- Data Parallel C++ compiler, library and analysis tools
- SYCLomatic / DPC++ Compatibility tool helps migrate CUDA code to C++ with SYCL
- Python distribution includes accelerated scikit-learn, NumPy, SciPy libraries
- Optimized performance libraries for threading, math, data analytics, deep learning, and video/image/signal processing

Summary

- oneAPI cross-architecture, one source programming model provides freedom of XPU choice.
 Apply your skills to the next innovation, not to rewriting software for the next hardware platform.
- Intel® oneAPI Toolkit products take full advantage of accelerated compute by maximizing performance across Intel CPUs, GPUs, and FPGAs.
- Develop confidently with a proven set of crossarchitecture libraries and advanced tools that interoperate with existing performance programming models.





Intel® oneAPI HPC Toolkit

Accelerate Data-centric Workloads

Top Features/Benefits

- Data Parallel C++ compiler, library and analysis tools
- SYCLomatic / DPC++ Compatibility tool helps migrate CUDA code to C++ with SYCL
- Python distribution includes accelerated scikit-learn, NumPy, SciPy libraries
- Optimized performance libraries for threading, math, data analytics, deep learning, and video/image/signal processing