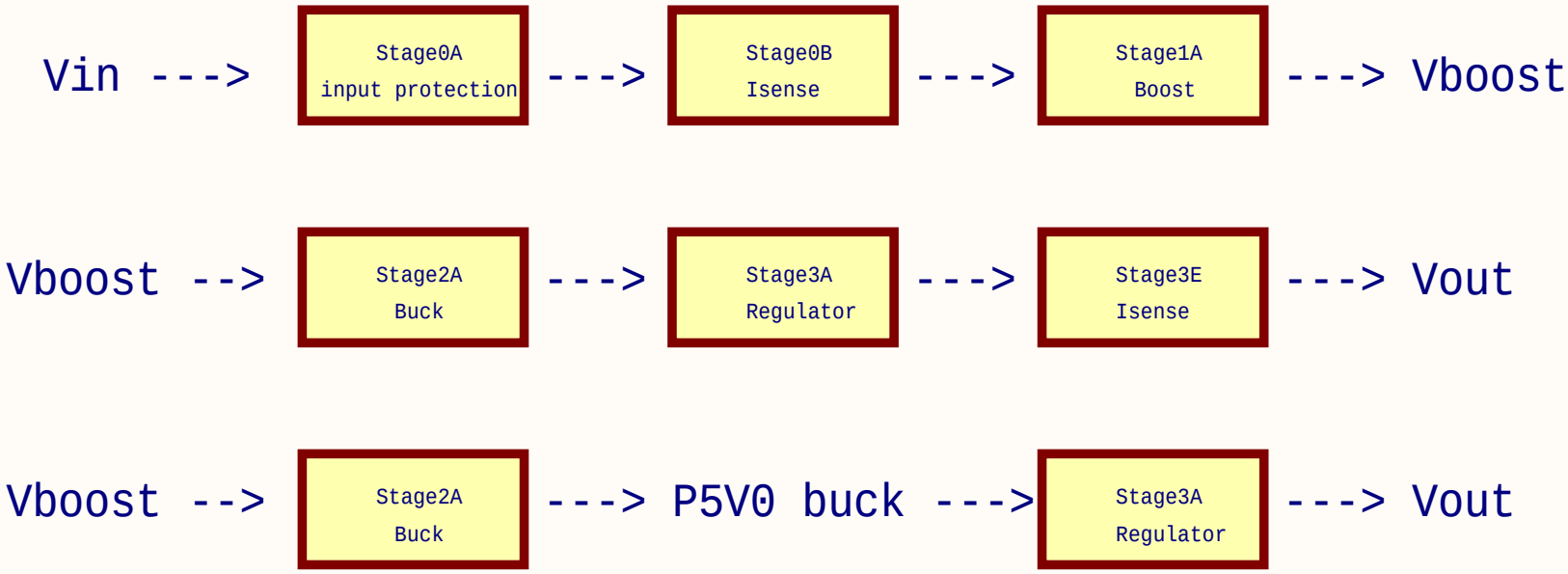

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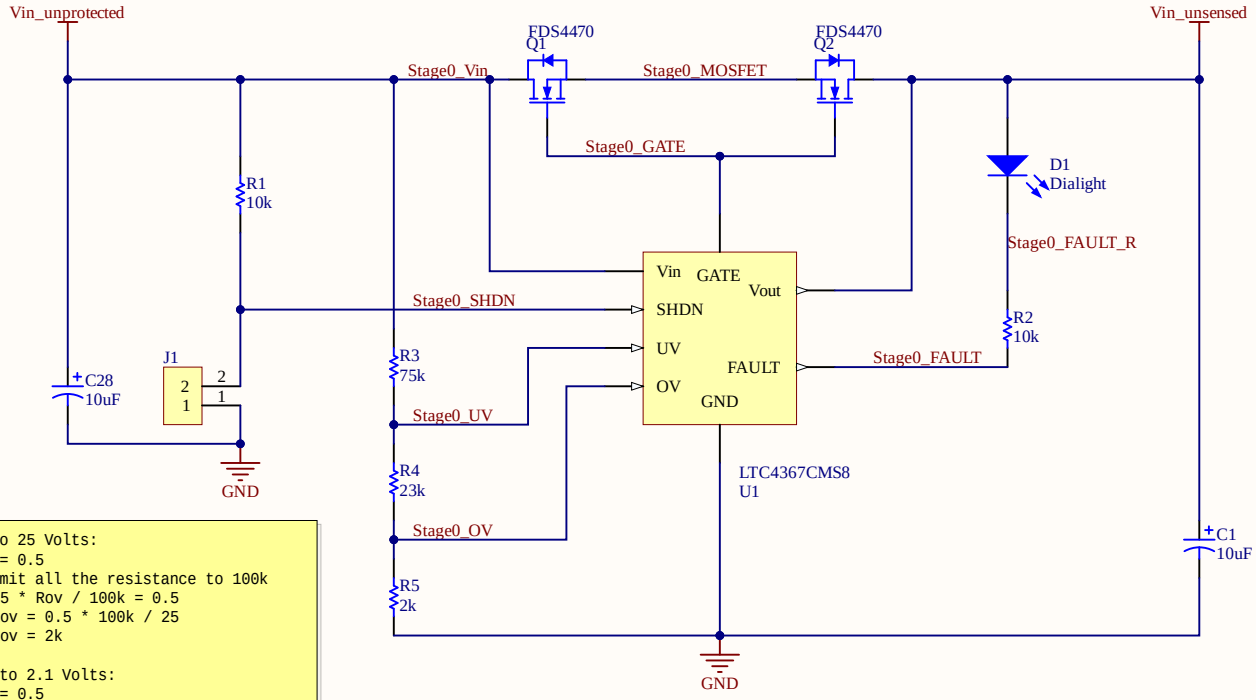


```
Overvoltage set to 25 Volts:
        Vtrigger = 0.5
        So, if limit all the resistance to 100k
                25 * Rov / 100k = 0.5
                Rov = 0.5 * 100k / 25
                Rov = 2k

Undervoltage set to 2.1 Volts:
        Vtrigger = 0.5
        So,
                2.1 * (Rov + Ruv) / 100k = 0.5
                2.1 * (2k + Ruv) / 100k = 0.5
                (2k + Ruv) = 0.5 * 100k / 2.1
                2k + Ruv = 23.81k
                Ruv = 21.81k  22k
```

Title		
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Date: 6/27/2022		Sheet of
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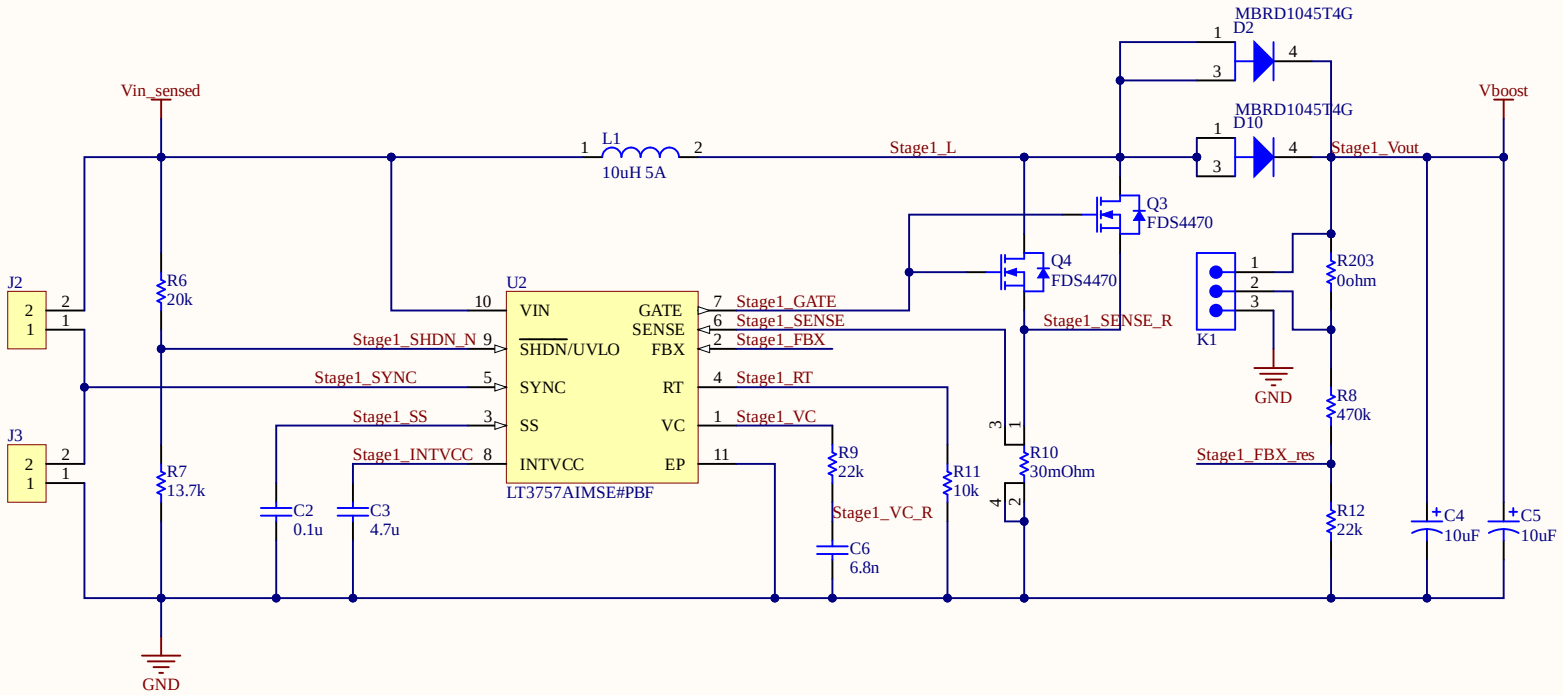
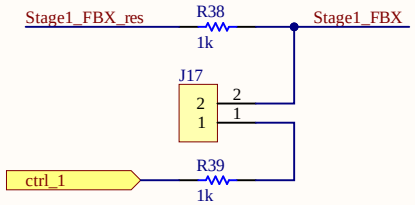



```
FB voltage set to 38 volts:
        Vfb = 1.7
        So,
                38 * Rbot / (Rtop + Rbot) = 1.7
                Rtop = 470k
                Rbot = 22k
But to control the voltage the Vfb comes
from an average between FB resistors and
PWM from arduino.
        Note that if FB is held above 1.7
        Vout will drop down to Vin  [NOT 0!]
```



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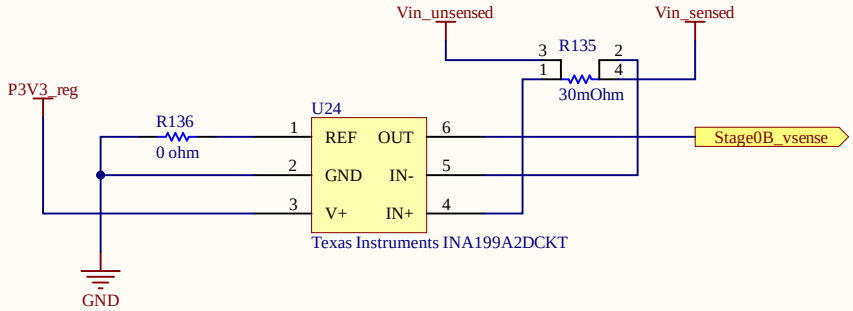

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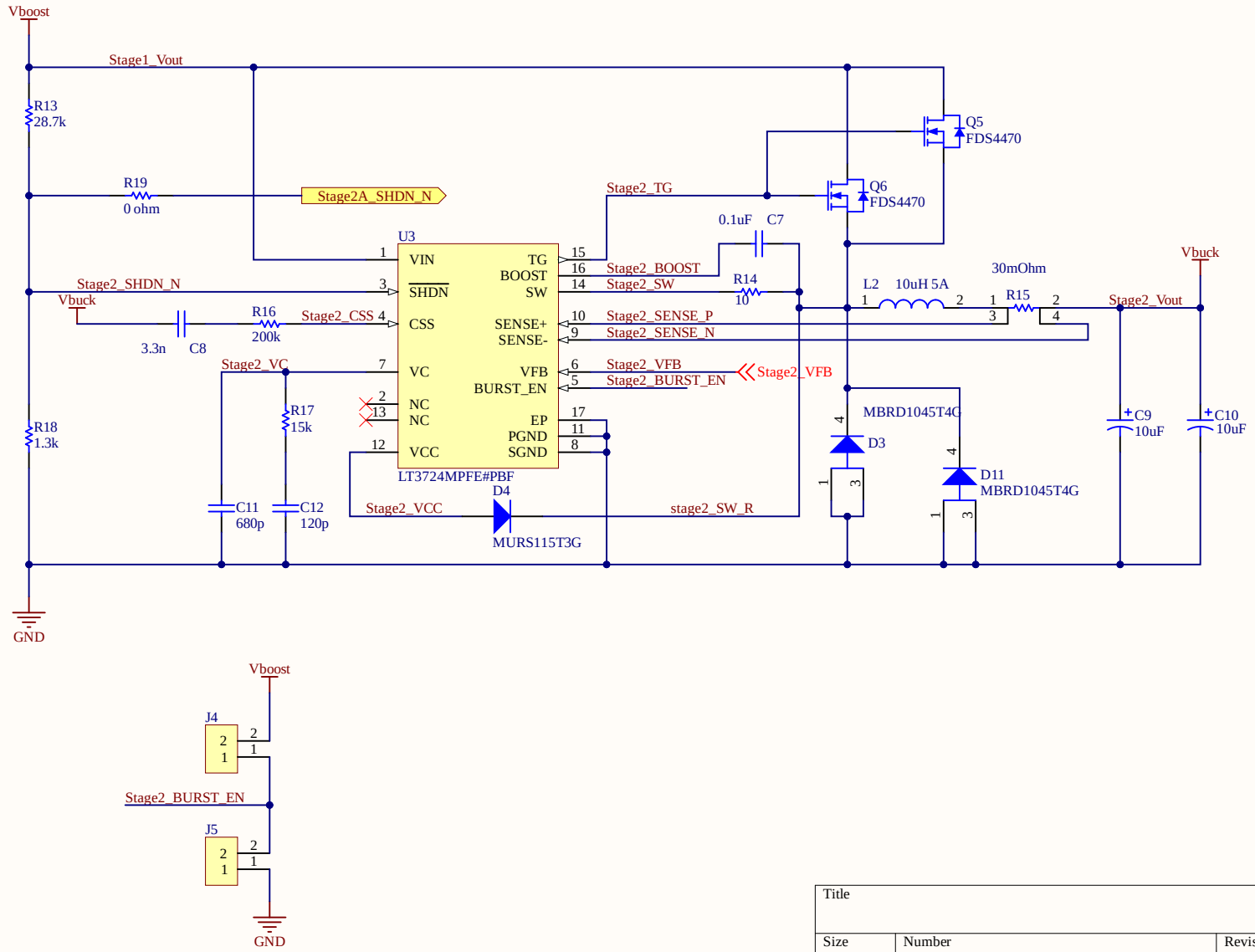

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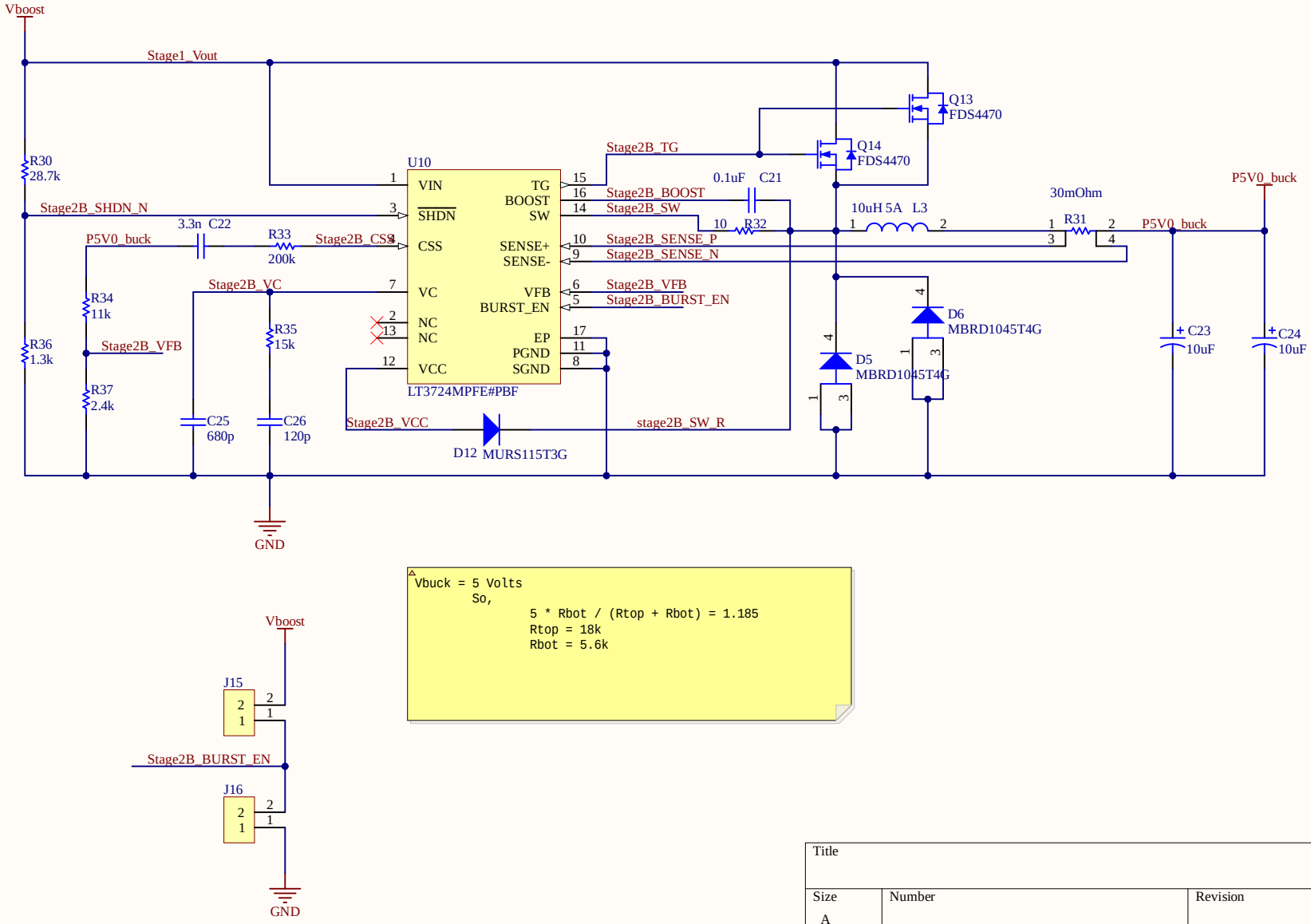

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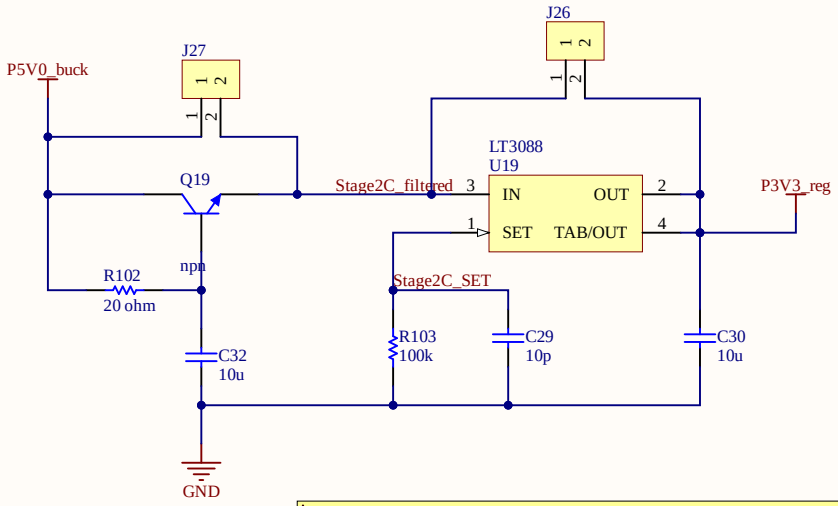

This should create a very clean P5V0 rail.
However, the voltage drop needed will be
1.1 - 1.6 V for LDO and 0.7 V for filter

Total of 1.8 - 2.3 Volts. So if Vin = 5V then Vout 3.2 - 2.7.
So if the pre filter is used the 5V0_buck voltage should
be raised 0.3 Volts

Title		
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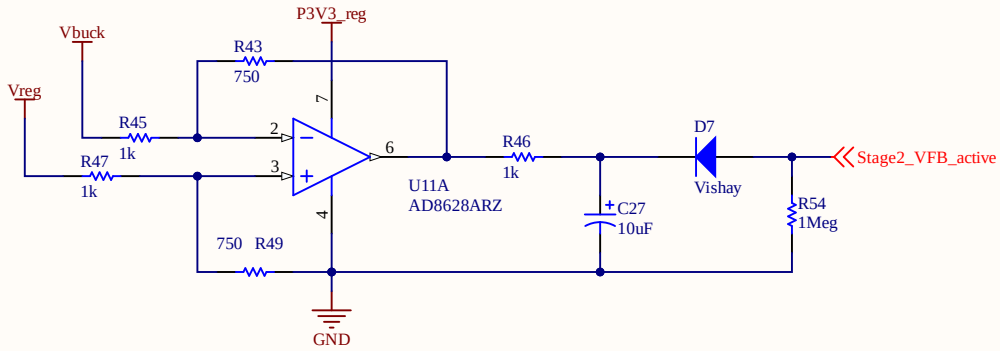

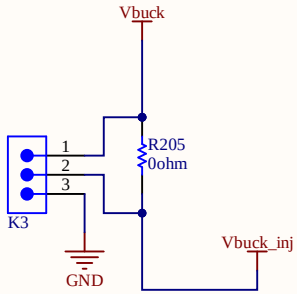

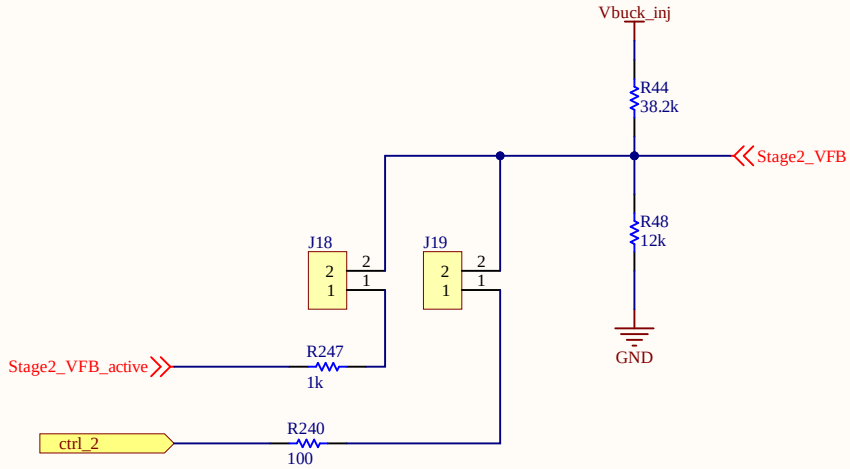

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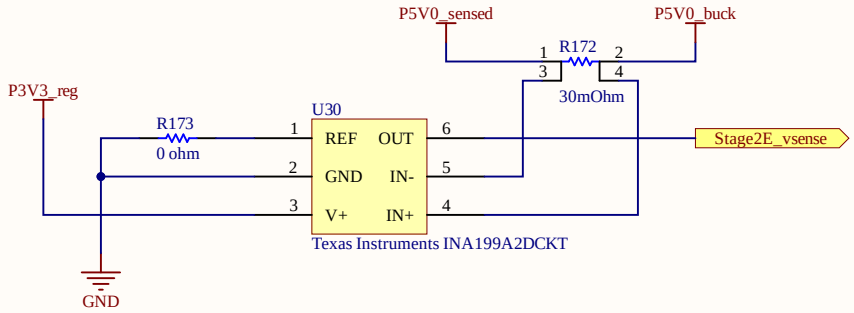

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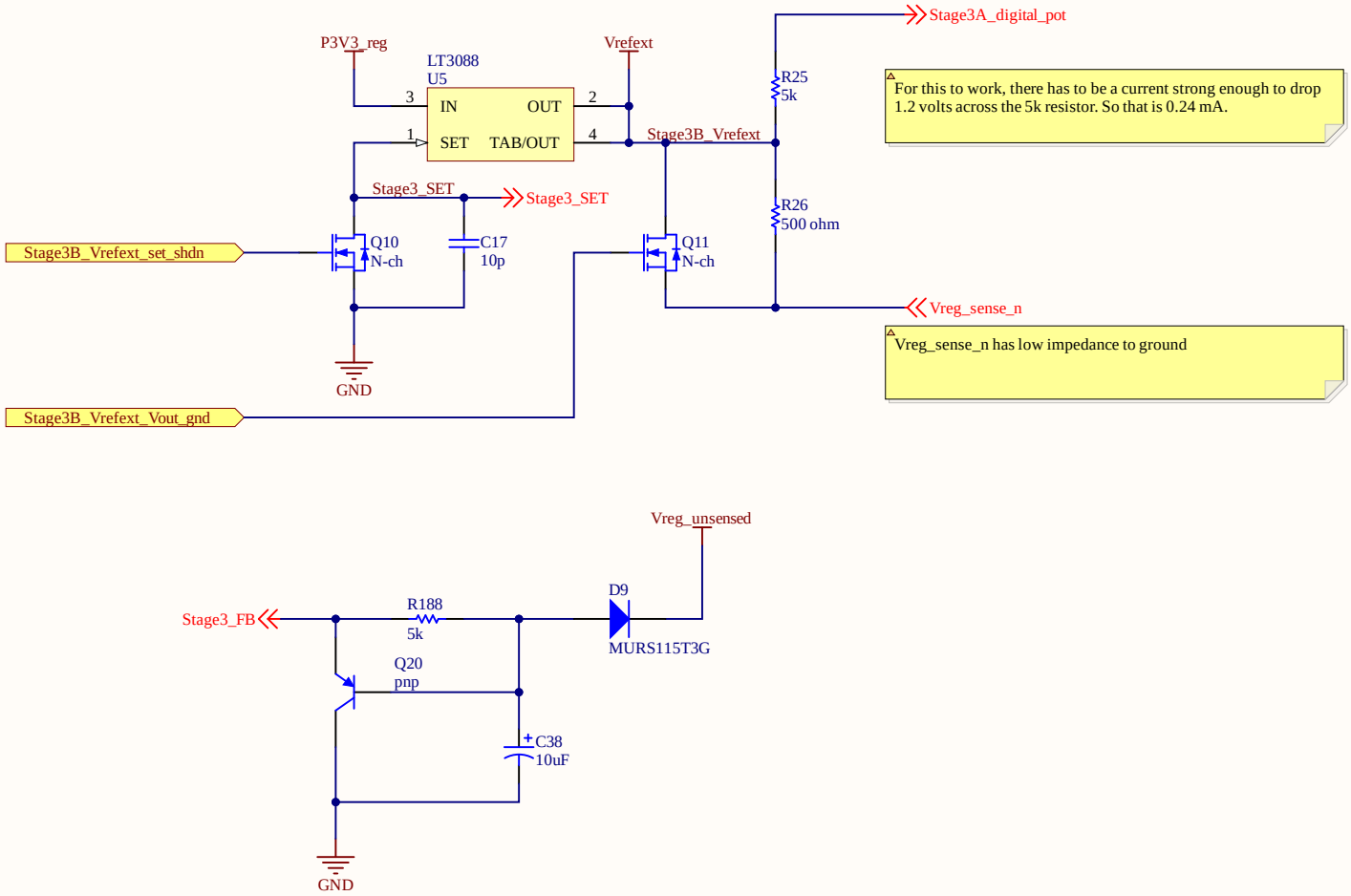

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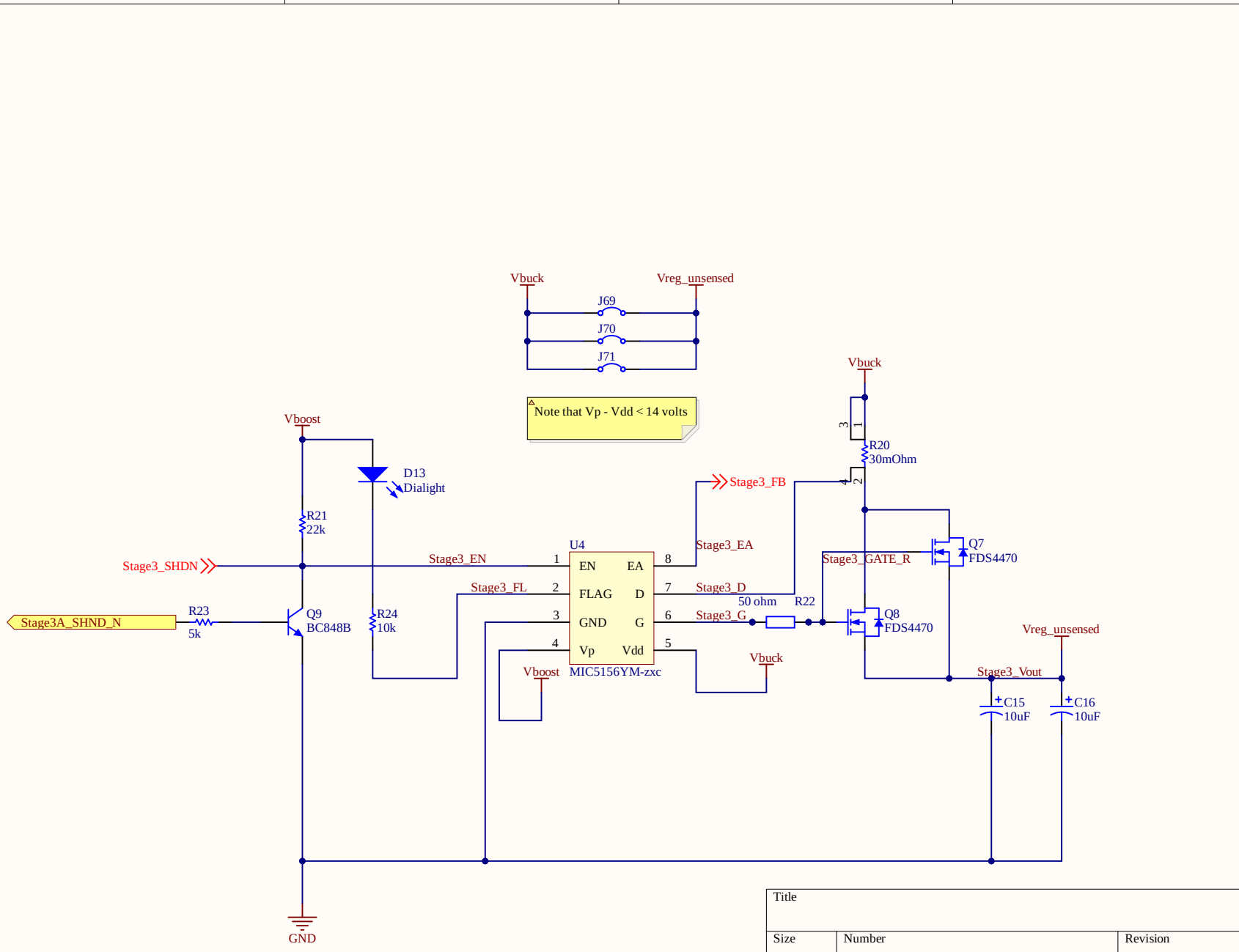

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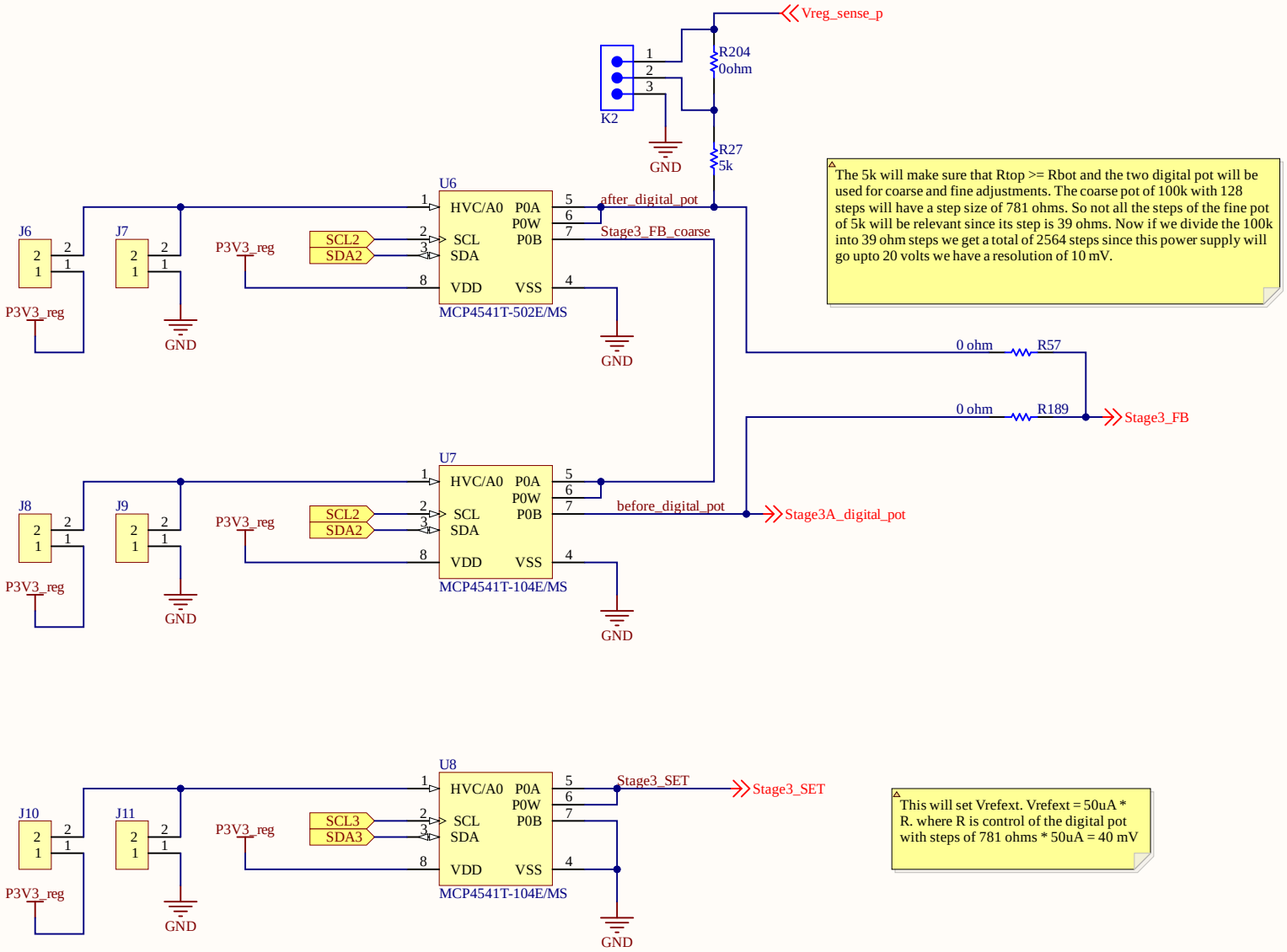

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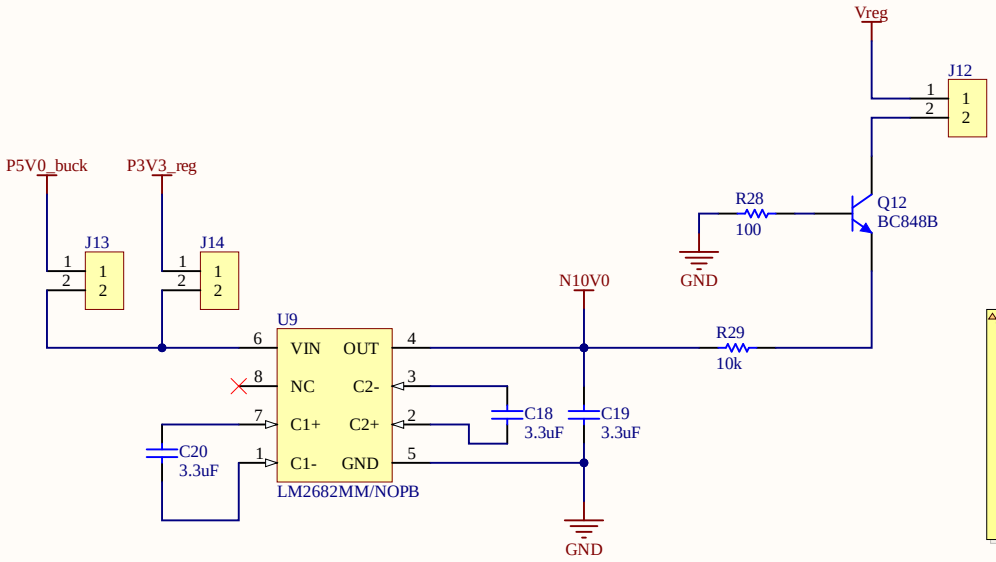

We just need a 0.25mA running on the output such that there is at least a 1.2V drop on a 5k resistor.

Title		
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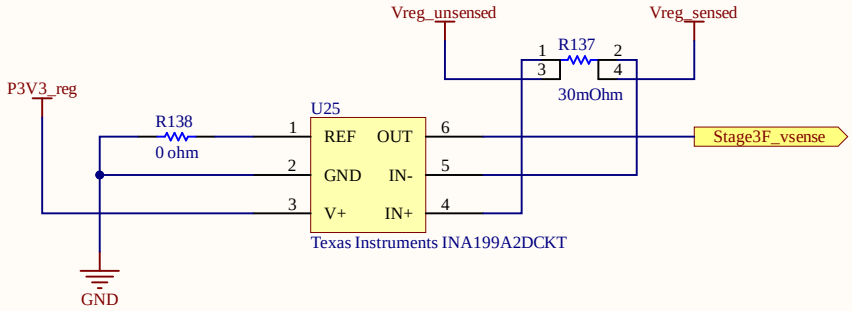

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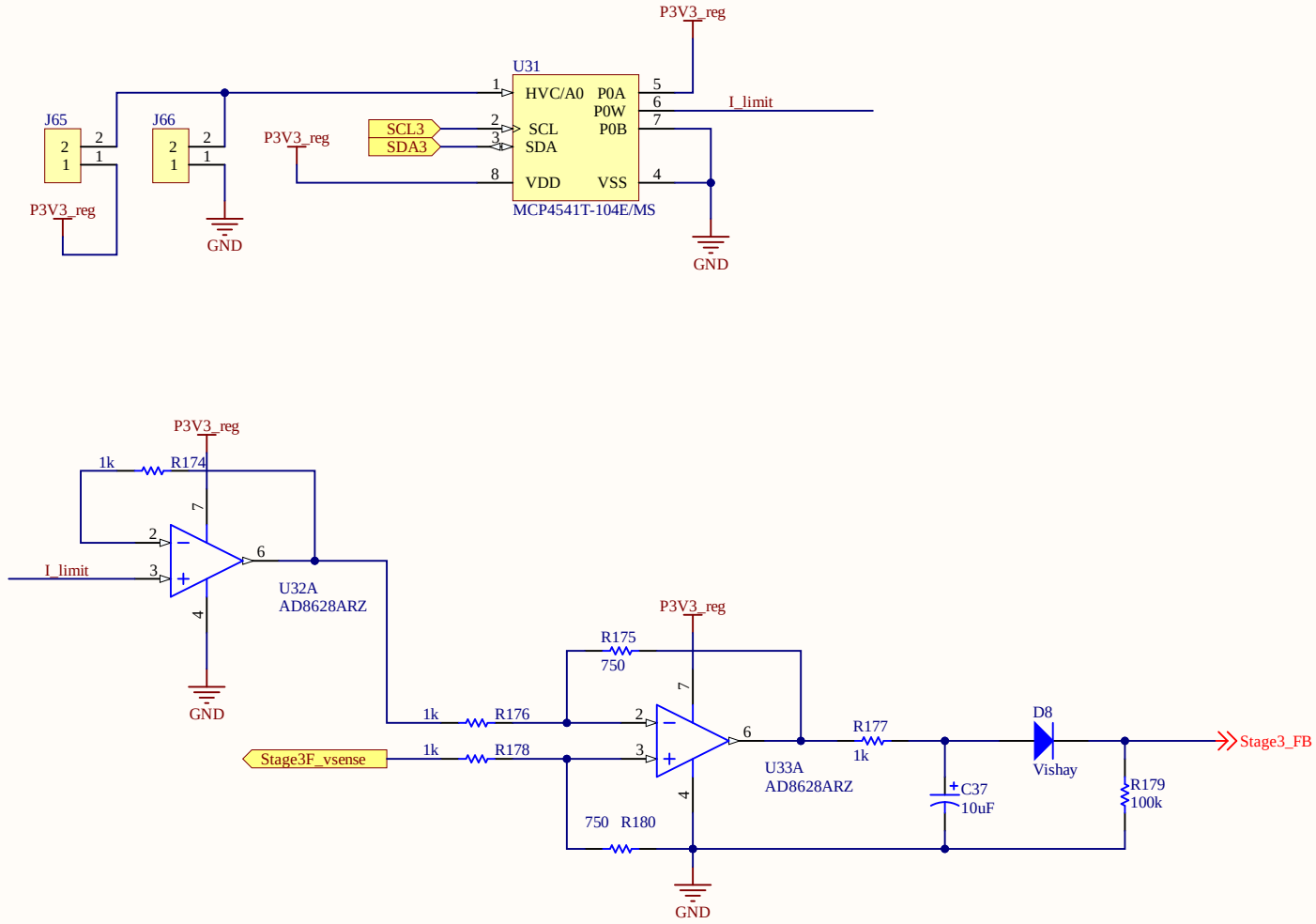

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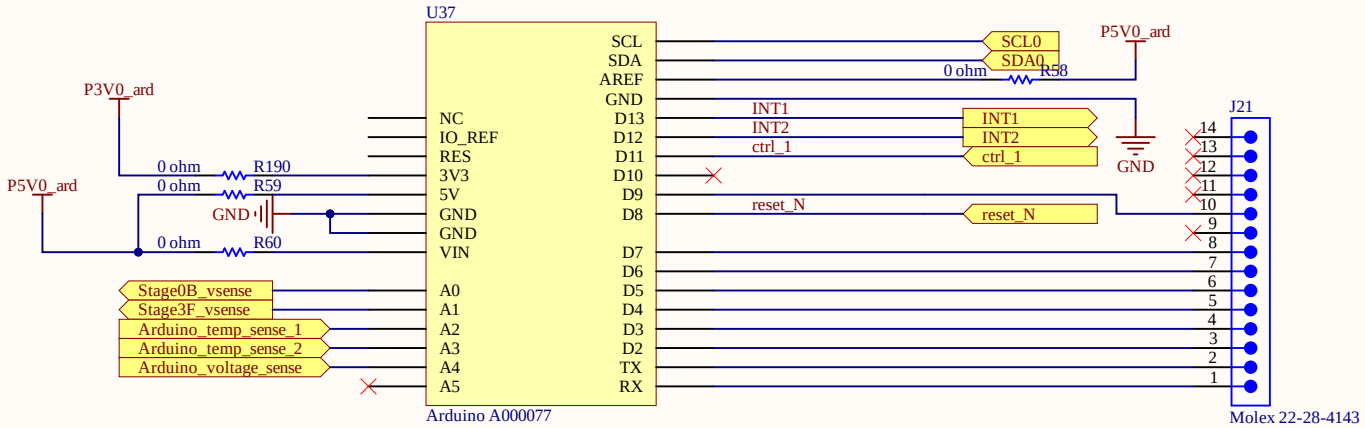

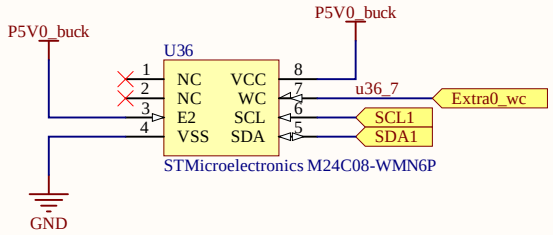

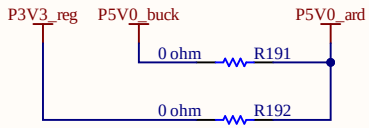

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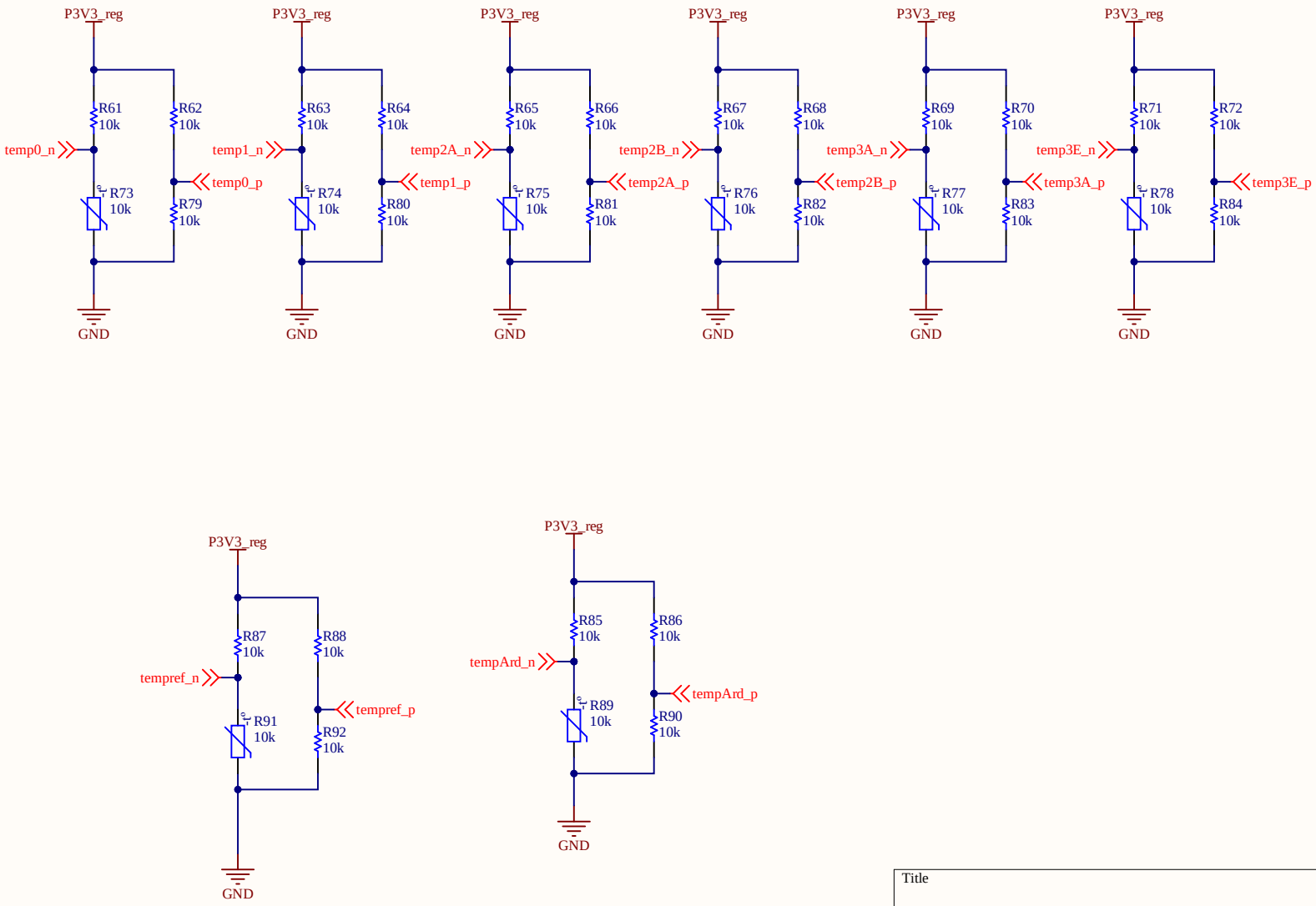

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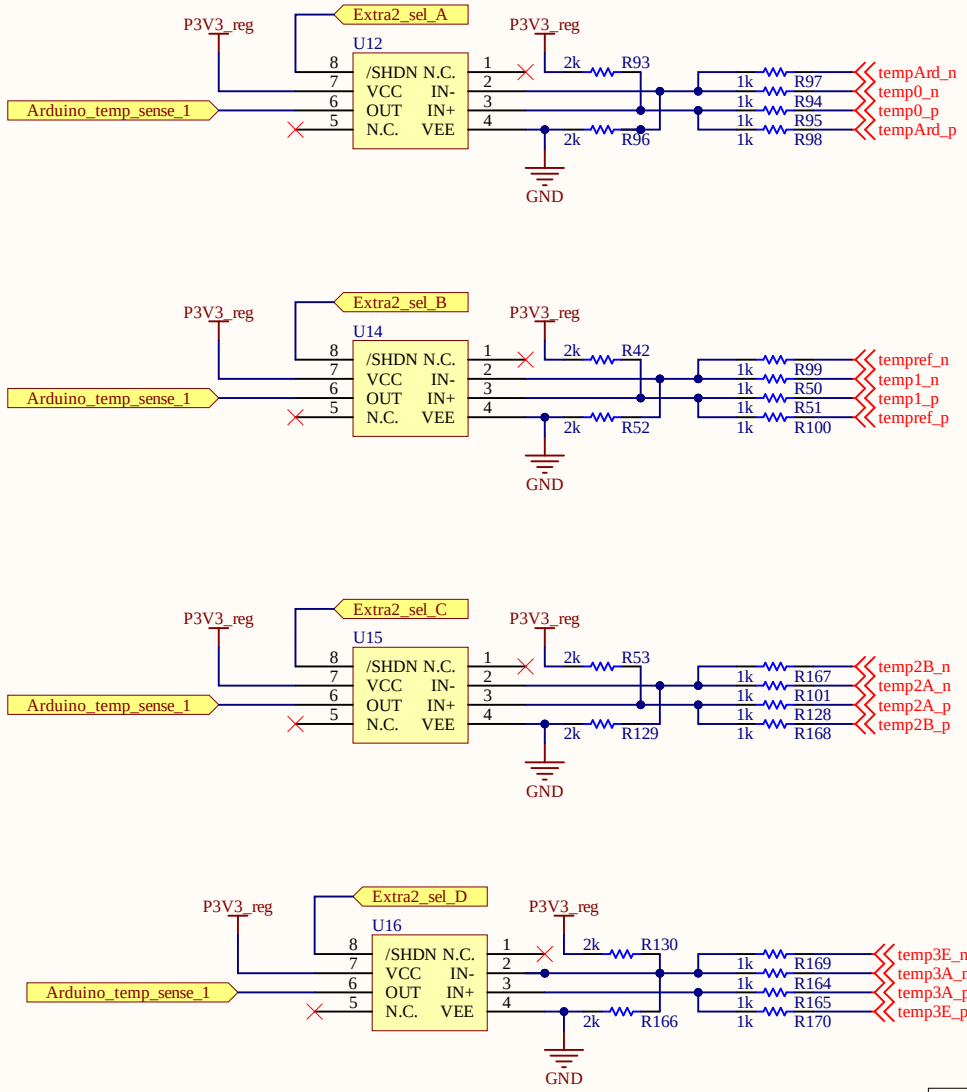

One should select just one differential pair going to the op-amp.

Title		
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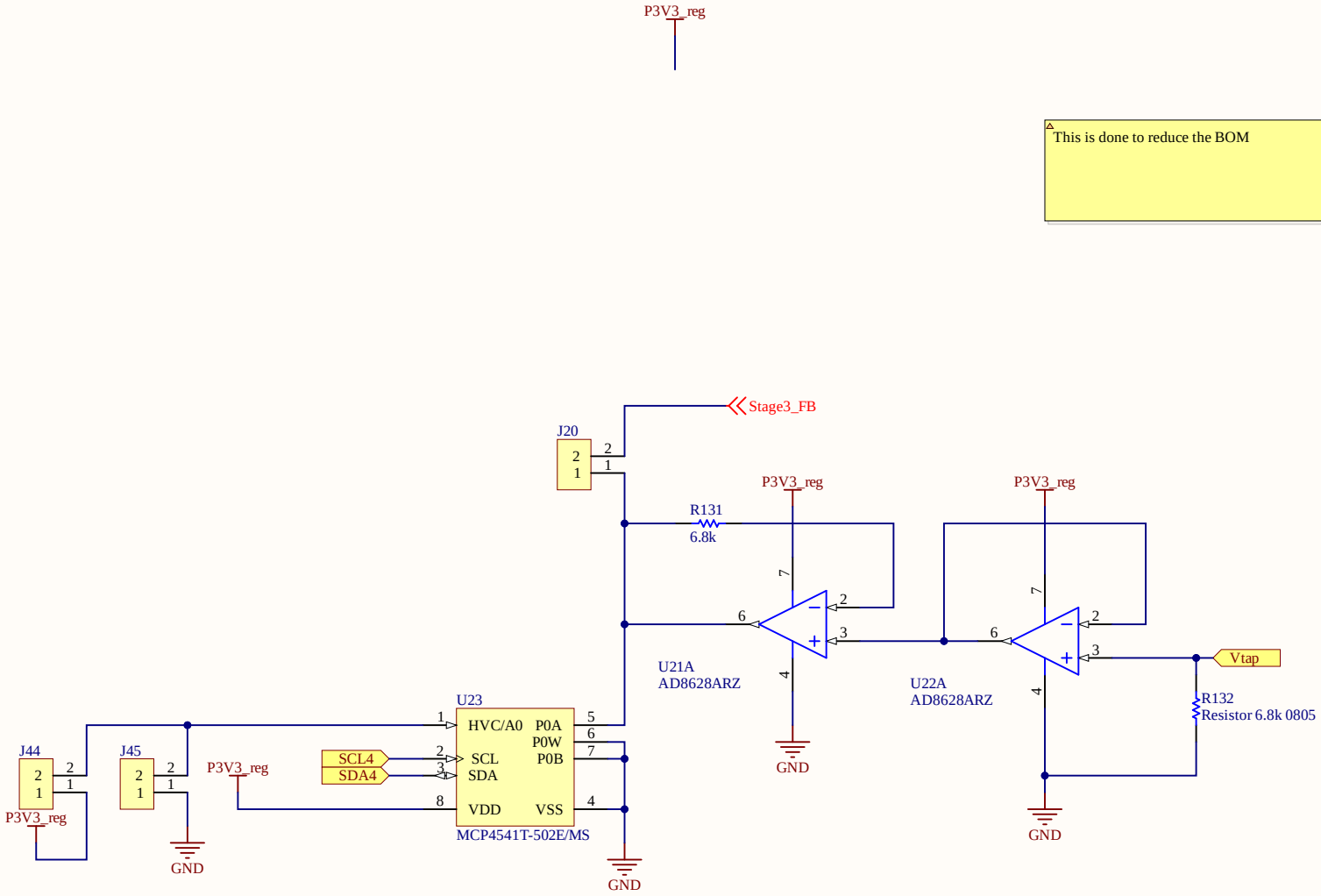

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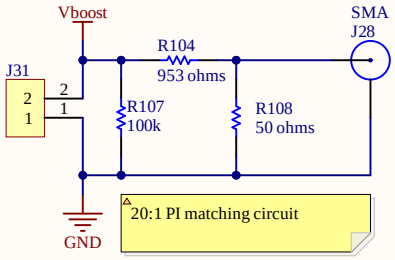

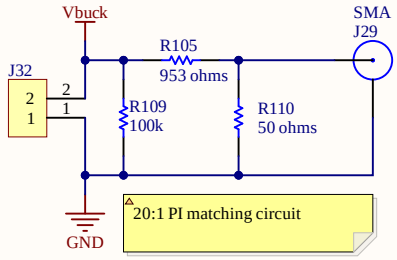

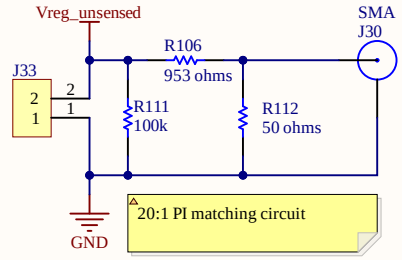

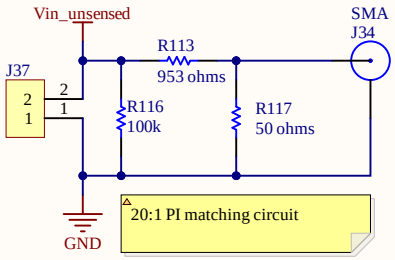

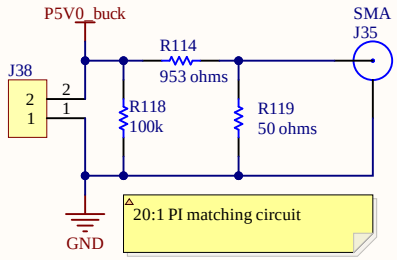

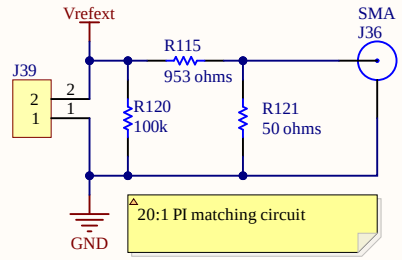

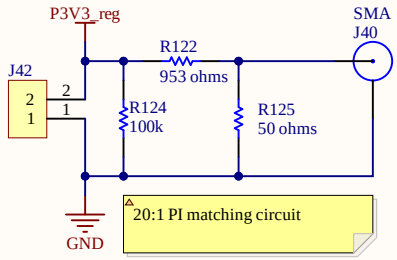

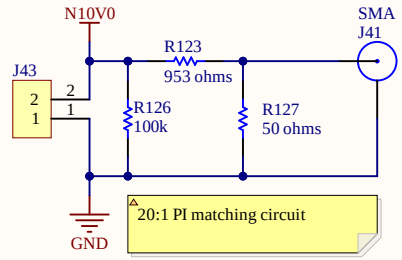

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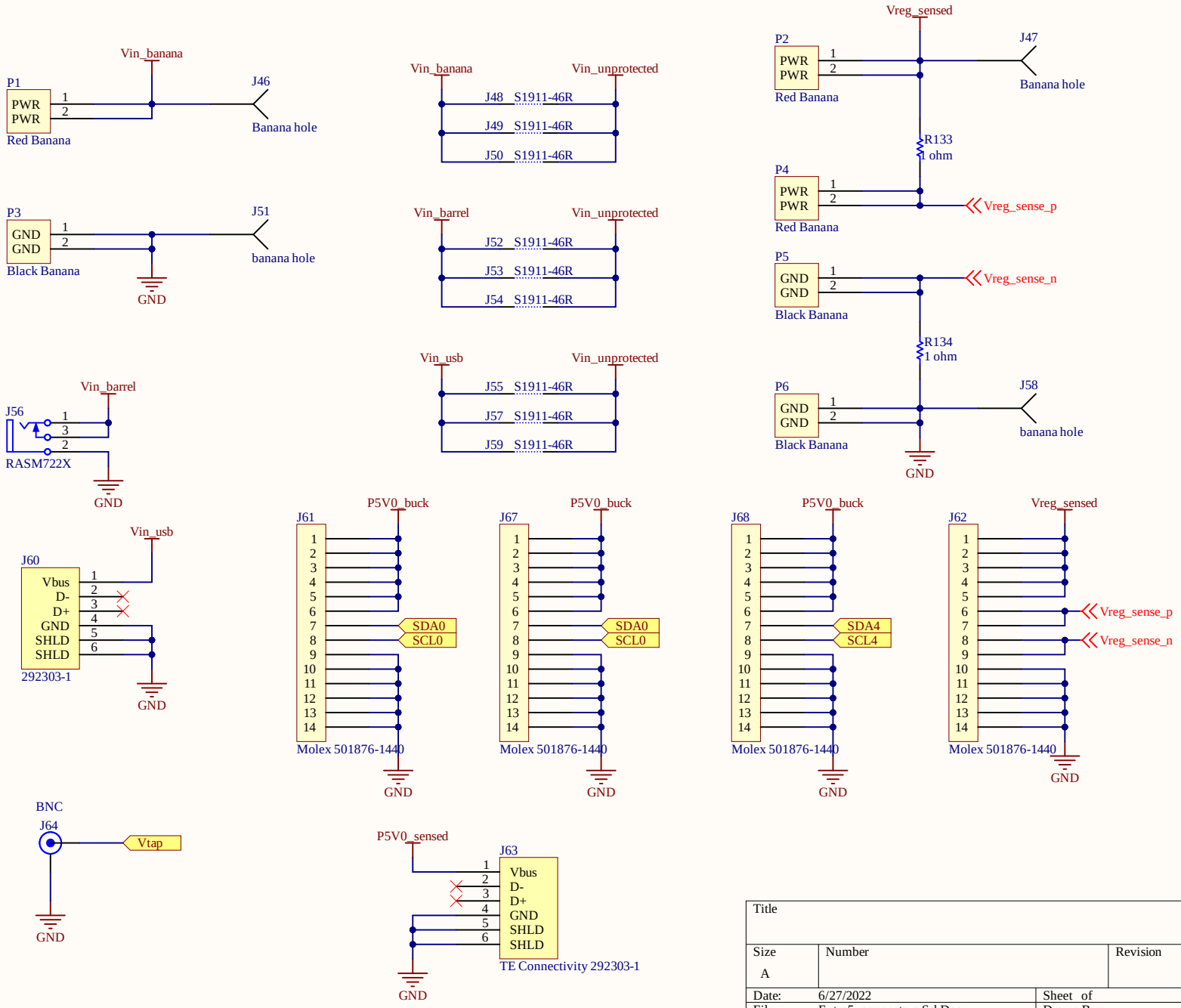
Vin_banana
P1
PWR
PWR
1
2
J46
Banana hole
Red Banana
Vin_banana
Vin_unprotected
J48 S1911-46R
J49 S1911-46R
J50 S1911-46R
Vreg_sensed
P2
PWR
PWR
1
2
J47
Banana hole
Red Banana
R133
1 ohm
P4
PWR
PWR
1
2
Vreg_sense_p
Red Banana
P3
GND
GND
1
2
J51
banana hole
Black Banana
GND
Vin_barrel
Vin_unprotected
J52 S1911-46R
J53 S1911-46R
J54 S1911-46R
P5
GND
GND
1
2
Vreg_sense_n
Black Banana
R134
1 ohm
P6
GND
GND
1
2
J58
banana hole
Black Banana
GND
Vin_barrel
J56
1
3
2
RASM722X
GND
Vin_usb
Vin_unprotected
J55 S1911-46R
J57 S1911-46R
J59 S1911-46R
Vin_usb
J60
Vbus
D-
D+
GND
SHLD
SHLD
1
2
3
4
5
6
292303-1
GND
P5V0_buck
J61
1
2
3
4
5
6
7
8
9
10
11
12
13
14
SDA0
SCL0
Molex 501876-1440
GND
P5V0_buck
J67
SDA0
SCL0
Molex 501876-1440
GND
P5V0_buck
J68
SDA4
SCL4
Molex 501876-1440
GND
Vreg_sensed
J62
Vreg_sense_p
Vreg_sense_n
Molex 501876-1440
GND
BNC
J64
Vtap
GND
P5V0_sensed
J63
Vbus
D-
D+
GND
SHLD
SHLD
TE Connectivity 292303-1
GND
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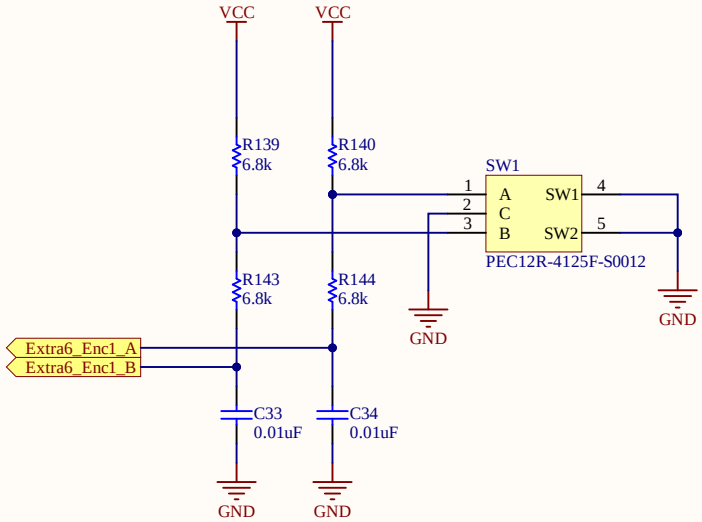

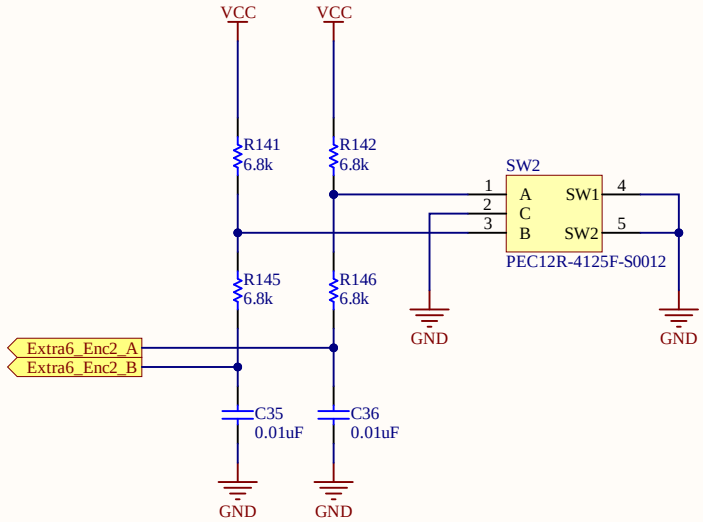

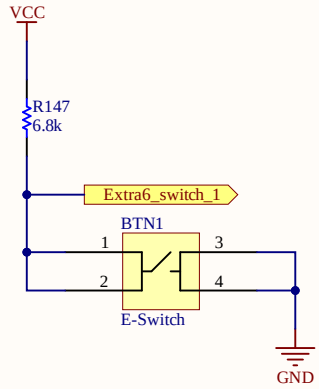

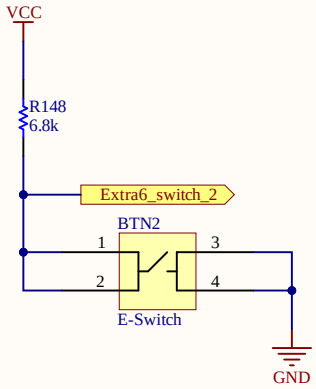

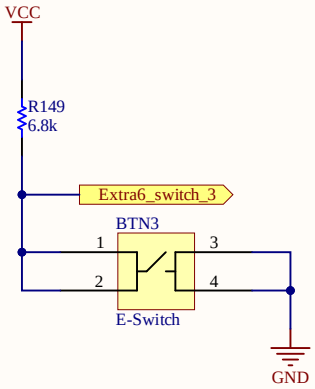

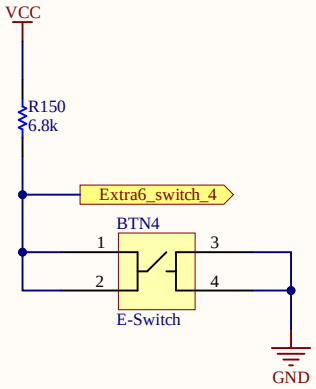

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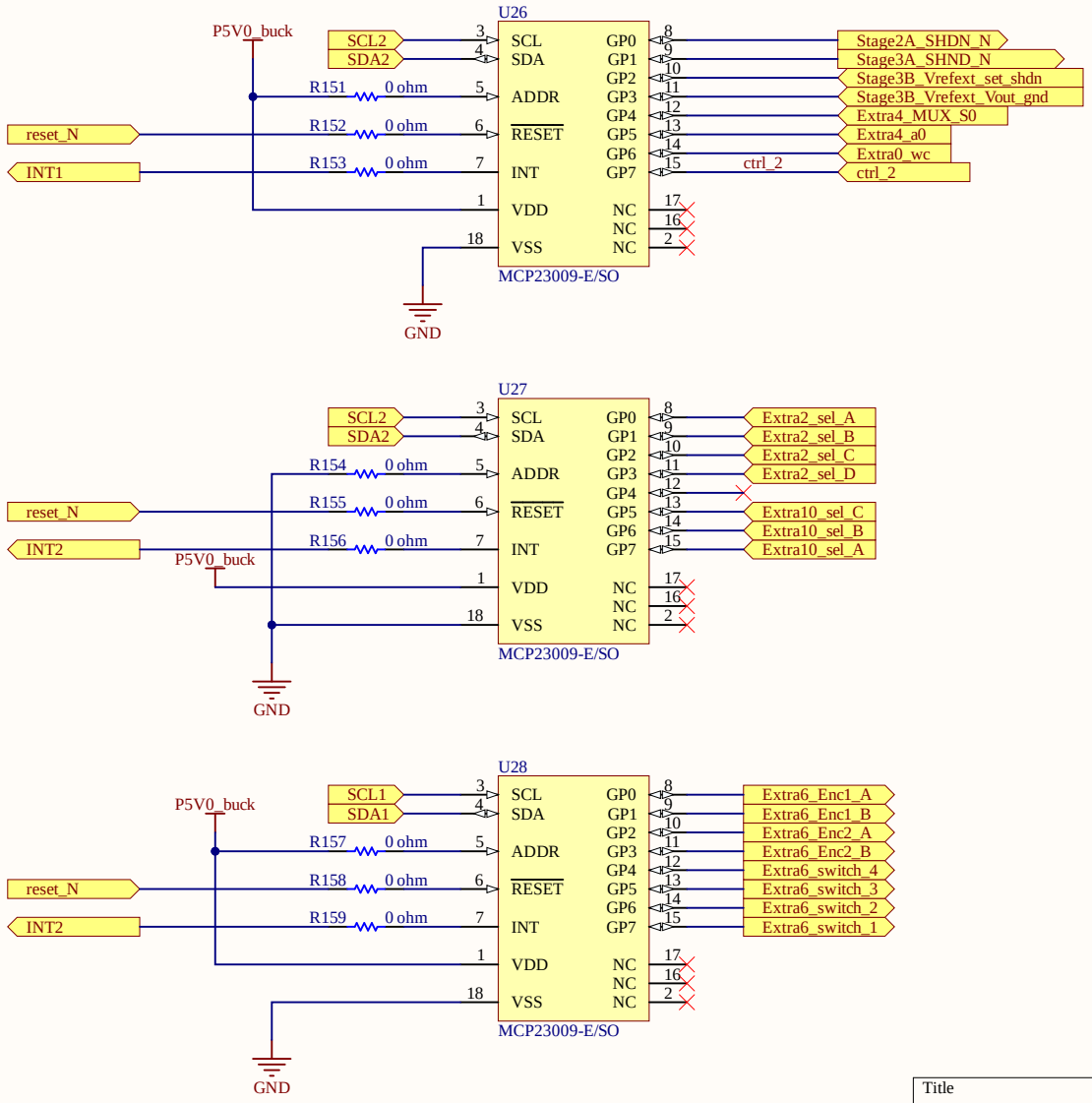

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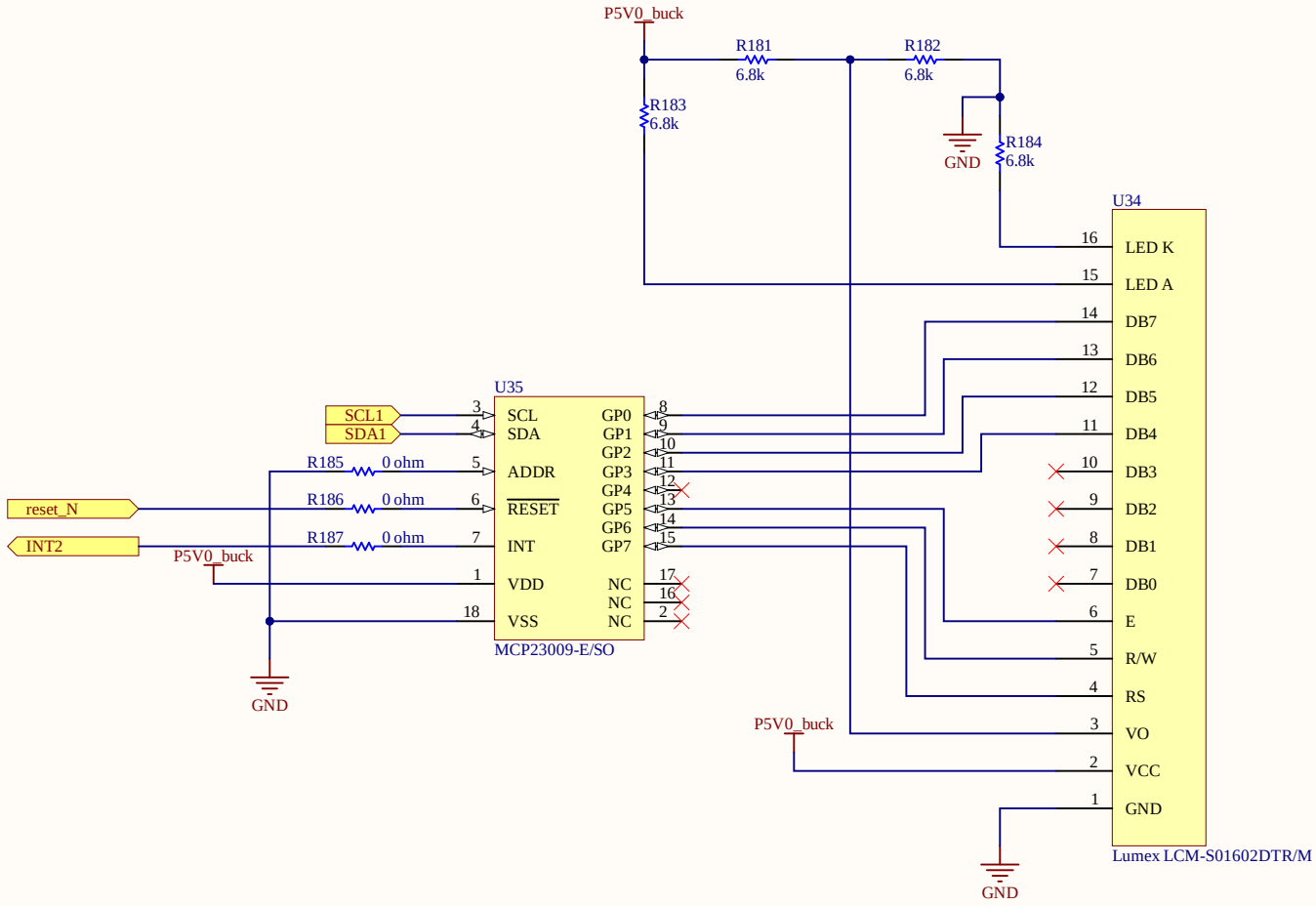

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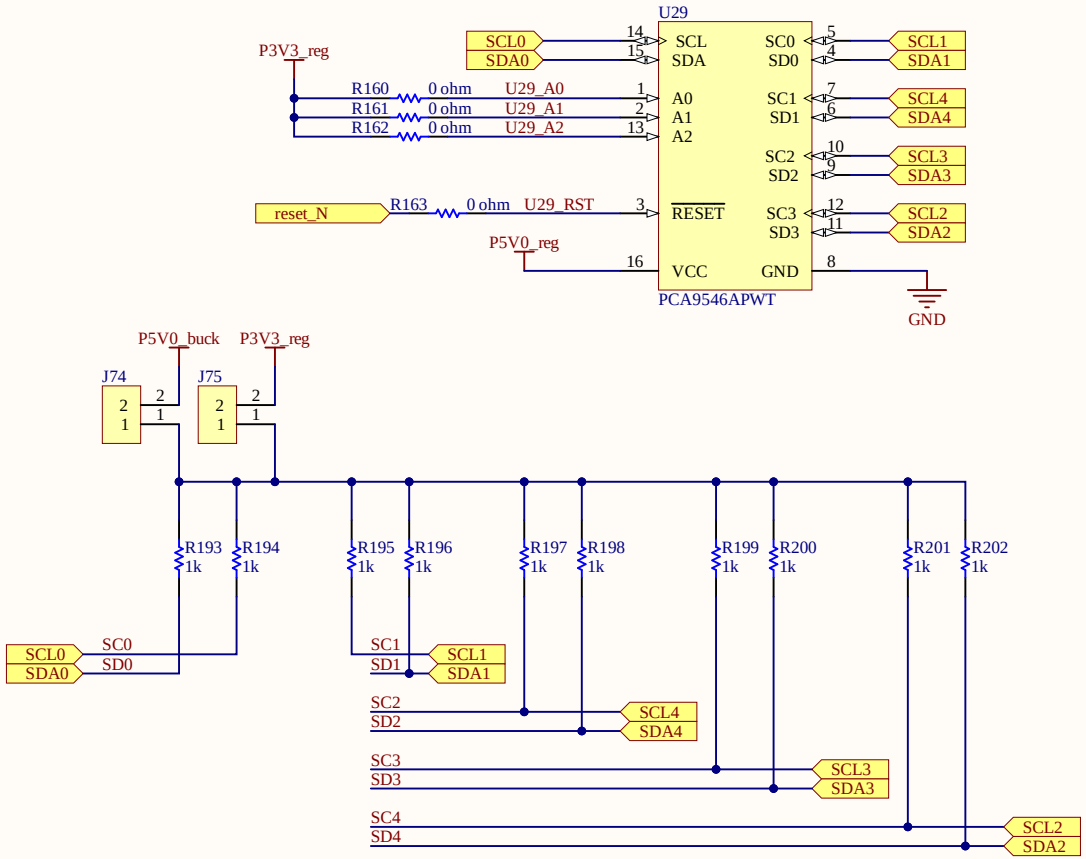

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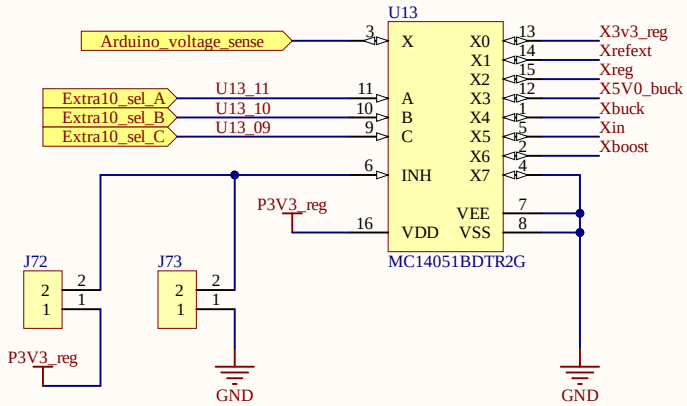

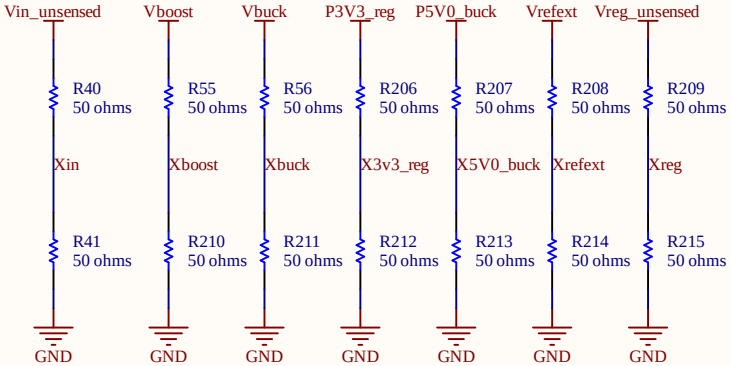

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