Lab 1: Floating Point Conversion

Ethan Ngo

TA: Ananya Ravikumar (Section 3)

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Contents

1 Introduction

The focus of the Floating Point Conversion lab is for students to become familiar with the Xilinx ISE software and utilize it to implement and test a floating point converter. This converter required us to build a combinational circuit that converts a 13-bit linear encoding input into a 9-bit Floating Point (FP) Representation output with a 1-bit sign (S), 3-bit exponent (E), and 5-bit significand/mantissa (F). The computation can be represented by this formula:

$$V = (-1)^S * F * 2^E$$

An additional focus of this lab is that this conversion is not as accurate, as there are less bits in the significand (5 bits) compared to the original value (13 bits). With this problem arose the situation of rounding and how how to handle these scenarios, along with other edge cases. Rounding and how other edge cases were handled will be described in later sections. The implementation would be tested for accuracy by a test bench that we design, which simulates the behaviors of various inputs.

2 Module Description

For the design of the floating point converting circuit, I adopted the block diagram provided in the lab specifications, shown below:

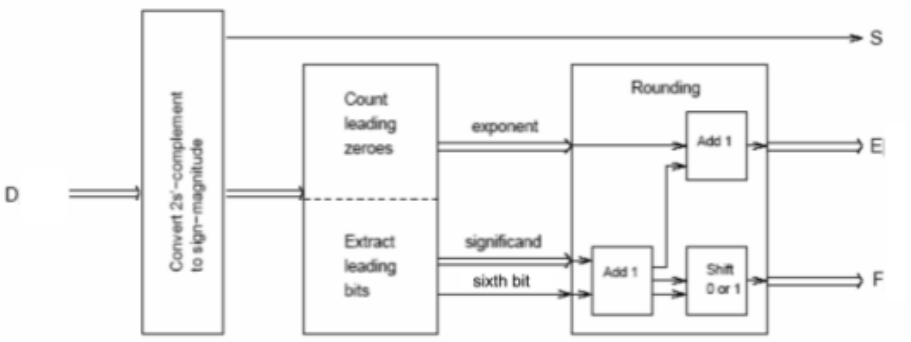

Figure 1: Floating Point Converter Block Diagram

To design each of the sub-blocks of the block diagram from left to right, I created 3 sub-modules, signMagConversion, bitExtraction and rounding. My main module FPCVT takes these three sub-modules and converts the 13-bit linear encoding into the compounded 9-bit floating point representation. FPCVT takes an input of [12:0] D as the 13-bit linear encoding and outputs S, [2:0] E, and [4:0] F, which represents the sign, exponent, and significand of the FP representation, respectively.

1. **Sub-Module 1:** signMagConversion

   This module converts the 13-bit 2's complement input into the equivalent sign-magnitude representation. In sign-magnitude, positive values are unaffected and negative values are set to their positive counterparts.

   To do this in Verilog, I take a [12:0] twosComplement input and output sign and [12:0] signMagnitude. I used a block of if else statements in an always block to save the sign of the input. This code then checks for an edge case for the

biggest negative number 13'b1000000000000 and setting it to the proper sign-magnitude value. For negative values, the input is inverted and incremented by one and set to the output, which positive values are simply set to the output. Below is a hand-drawn schematic of the general purpose, omitting intricate details to avoid confusion.

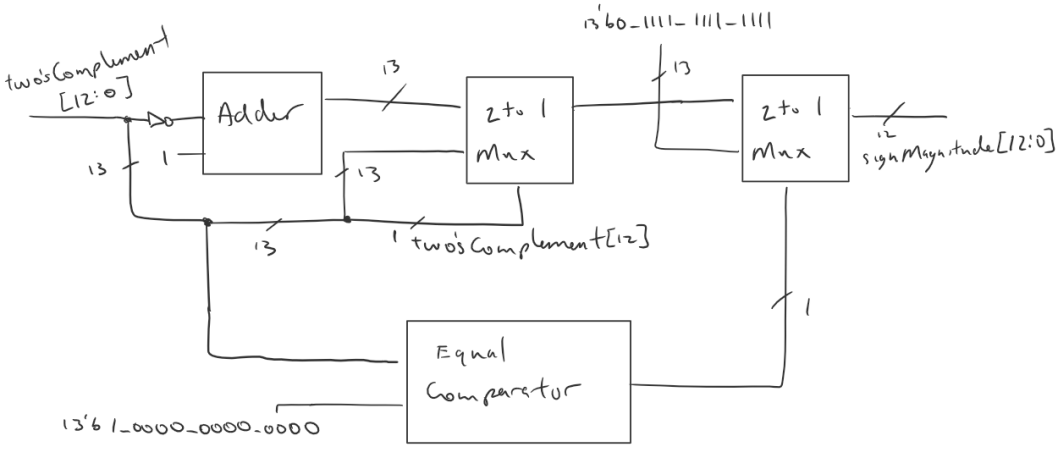

Figure 2: signMagConversion Module Schematic

2. **Sub-Module 2:** bitExtraction

   This module take the output from signMagConversion and does basic FP conversion, extracting the exponent, significand and the "6th bit" to be used the following module, rounding. The exponent and significand output is based on the number of leading zeroes.

   To do this in Verilog, I take a [12:0] signMagnitude input from signMagConversion and outputs a [2:0] exp, [4:0] significand , and sixthBit. Using a priority queue, which is implemented with an always block surrounding a block of if else statements that checked which bit position was the first nonzero bit, I extract the exponent based on the number of leading zeroes. Afterwards, the next 5 bits (start-

ing from the first nonzero bit, or the 5 least significant bits if required) are set to the significand. The sixth bit would be used for rounding, which is simply the bit following the significand, or 0 if none exists.

Below is a hand-drawn schematic of the general purpose, omitting intricate details to avoid confusion.

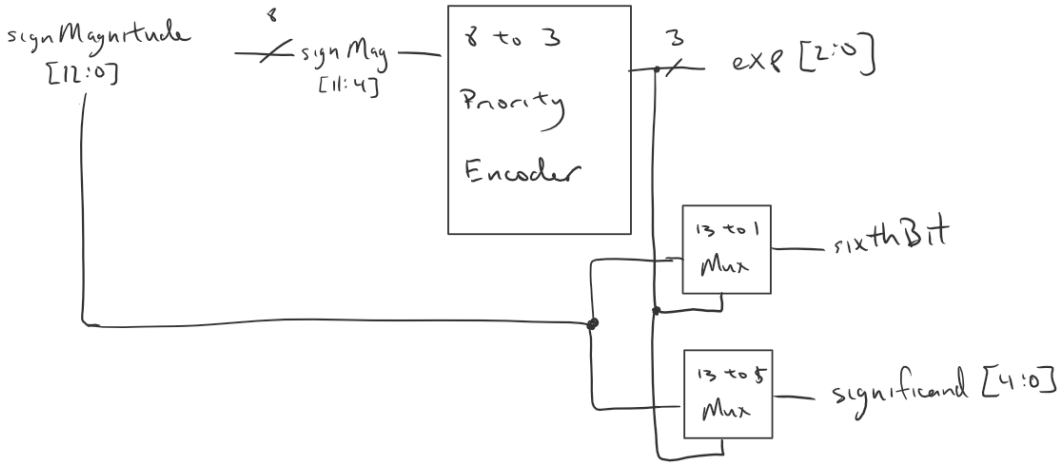

Figure 3: bitExtraction Module Schematic

3. **Sub-Module 3:** rounding

   This module take the output from bitExtraction and performs rounding on the FP representation. The rounding is based on the sixthBit from bitExtraction and if sixthBit = 1 then the significand is rounded up. If the significand overflows, we increment exp and right shift by 1 and increment by 1 on the significand.

   To do this in Verilog, rounding takes a [2:0] exp, [4:0] significand , and sixthBit as the input and outputs [2:0] newExp and [2:0] newSig. Utilizing an always block and if statements, I check for edge cases and deal with overflow of the significand and/or exponent and deal with them accordingly, and then have a

general execution of code for normal cases.

Below is a hand-drawn schematic of the general purpose, omitting intricate details to avoid confusion.

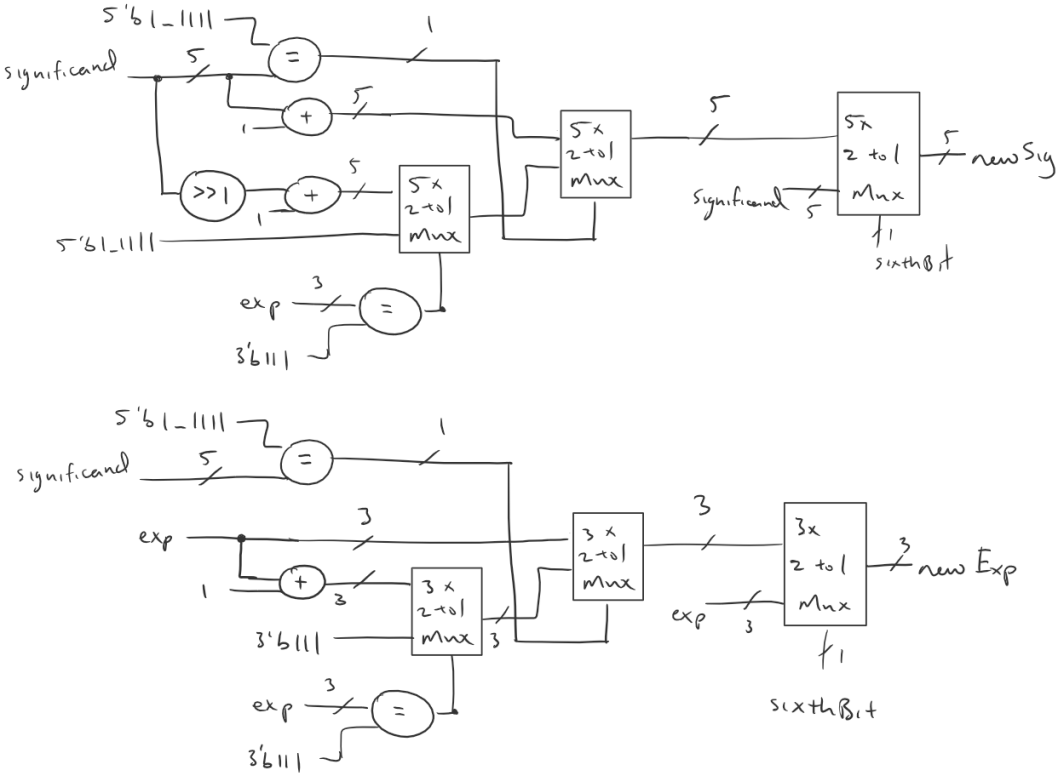

Figure 4: rounding Module Schematic

3 Test-bench Simulation

To test my modules, I tested my main module FPCVT and ran a series of tests with varying inputs of D to ensure the conversion works properly, observing how the inputs S, E, F are affected. Below is a snippet of the waveform from the test bench:

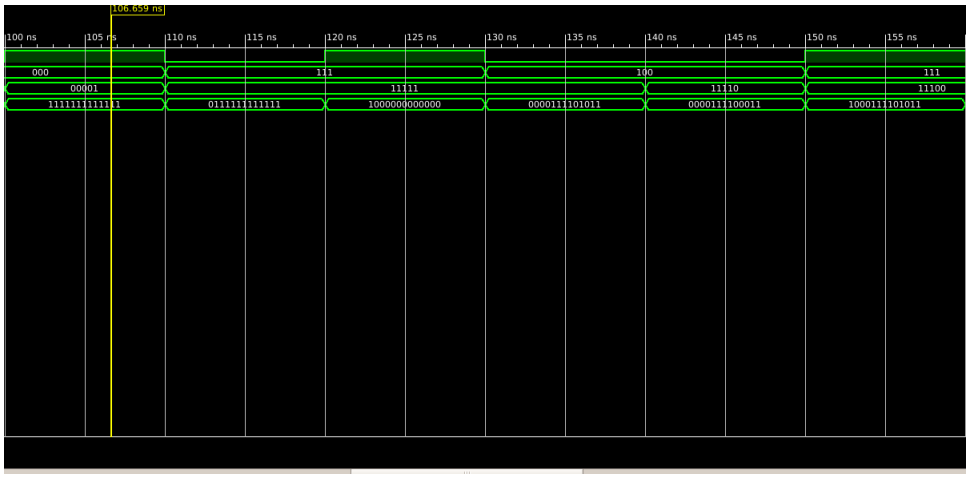

Figure 5: FPCVT Simulation Waveform Snippet

From top to bottom, the waves shown are S, E, F, D. To describe one of the inputs, we will look at 130 ns. The input for D is 13'b0000111101011 and the output is as follows: S is 0 E is 3'b100 and F is 5'b11111. To test if that is correct, since the input is positive, the sign-magnitude value is equal to the input. Counting the number of leading zeroes, we get 4. This means that the exponent should be 4, which is equal to 3'b100. For the significand, starting from the first nonzero bit, we get 5'b11110. In addition, we can see that the sixthBit is equal to 1, so we must round up, leaving us with 5'b11111 as the significand. As we can see, our calculations are equivalent to the output of the module and in-depth examination of all the different outputs would show that the module works as intended.

A bug I found was that having a 100 wait time was too long for the alotted test bench

time, so decreasing it to 10 allowed for all of my tests to run. In addition, in creating my wires and assigning them, I initially added/assigned them as needed, but it implementation didn't work properly so I attempted to put them all at the beginning of the module and it worked properly from there on.

4 Reports

4.1 ISE Design Overview Summary Report

FPCVT Project Status			
Project File:	Lab1.xise	**Parser Errors:**	No Errors
Module Name:	FPCVT	**Implementation State:**	Synthesized
Target Device:	xc6slx16-3csg324	**• Errors:**	No Errors
Product Version:	ISE 14.7	**• Warnings:**	1 Warning (1 new)
Design Goal:	Balanced	**• Routing Results:**	
Design Strategy:	Xilinx Default (unlocked)	**• Timing Constraints:**	
Environment:	System Settings	**• Final Timing Score:**	

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice LUTs	61	9112	0%
Number of fully used LUT-FF pairs	0	61	0%
Number of bonded IOBs	22	232	9%

Detailed Reports					[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Sun Apr 18 21:02:09 2021	0	1 Warning (1 new)	1 Info (1 new)
Translation Report	Out of Date	Sun Apr 18 20:49:44 2021	0	0	0
Map Report	Out of Date	Sun Apr 18 20:50:14 2021	0	0	6 Infos (0 new)
Place and Route Report	Out of Date	Sun Apr 18 20:50:39 2021	0	0	2 Infos (0 new)
Power Report					
Post-PAR Static Timing Report	Out of Date	Sun Apr 18 20:50:56 2021	0	0	4 Infos (0 new)

Figure 6: Design Summary

Above is the ISE Design Overview Summary Report. As indicated, there are no errors and only one warning. This warning is negligible and is simply informing me of a port that is useless to my implementation.

4.2 Synthesis Report

```
Release 14.7 - xst P.20131013 (lin64)
Copyright (c) 1995-2013 Xilinx, Inc.  All rights reserved.
-->
Parameter TMPDIR set to xst/projnav.tmp


Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.16 secs

-->
Parameter xsthdpdir set to xst


Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.16 secs

-->
Reading design: FPCVT.prj

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=========================================================================
*                      Synthesis Options Summary                        *
=========================================================================
---- Source Parameters
Input File Name                    : "FPCVT.prj"
Ignore Synthesis Constraint File   : NO
```

```
---- Target Parameters
Output File Name                   : "FPCVT"
Output Format                      : NGC
Target Device                      : xc6slx16-3-csg324

---- Source Options
Top Module Name                    : FPCVT
Automatic FSM Extraction           : YES
FSM Encoding Algorithm             : Auto
Safe Implementation                : No
FSM Style                          : LUT
RAM Extraction                     : Yes
RAM Style                          : Auto
ROM Extraction                     : Yes
Shift Register Extraction          : YES
ROM Style                          : Auto
Resource Sharing                   : YES
Asynchronous To Synchronous        : NO
Shift Register Minimum Size        : 2
Use DSP Block                      : Auto
Automatic Register Balancing       : No

---- Target Options
LUT Combining                      : Auto
Reduce Control Sets                : Auto
Add IO Buffers                     : YES
Global Maximum Fanout              : 100000
Add Generic Clock Buffer(BUFG)     : 16
Register Duplication               : YES
Optimize Instantiated Primitives   : NO
Use Clock Enable                   : Auto
Use Synchronous Set                : Auto
Use Synchronous Reset              : Auto
Pack IO Registers into IOBs        : Auto
Equivalent register Removal        : YES

---- General Options
Optimization Goal                  : Speed
Optimization Effort                : 1
Power Reduction                    : NO
Keep Hierarchy                     : No
Netlist Hierarchy                  : As_Optimized
RTL Output                         : Yes
Global Optimization                : AllClockNets
Read Cores                         : YES
Write Timing Constraints           : NO
Cross Clock Analysis               : NO
```

```
Hierarchy Separator                 : /
Bus Delimiter                       : <>
Case Specifier                      : Maintain
Slice Utilization Ratio             : 100
BRAM Utilization Ratio              : 100
DSP48 Utilization Ratio             : 100
Auto BRAM Packing                   : NO
Slice Utilization Ratio Delta       : 5

=========================================================================


=========================================================================
*                            HDL Parsing                                *
=========================================================================
Analyzing Verilog file "/home/ise/Xillinx_host/Lab1/FPCVT.v" into library work
Parsing module <signMagConversion>.
Parsing module <bitExtraction>.
Parsing module <rounding>.
Parsing module <FPCVT>.

=========================================================================
*                             HDL Elaboration                           *
=========================================================================

Elaborating module <FPCVT>.

Elaborating module <signMagConversion>.

Elaborating module <bitExtraction>.

Elaborating module <rounding>.

=========================================================================
*                            HDL Synthesis                              *
=========================================================================

Synthesizing Unit <FPCVT>.
    Related source file is "/home/ise/Xillinx_host/Lab1/FPCVT.v".
    Summary:
        no macro.
Unit <FPCVT> synthesized.

Synthesizing Unit <signMagConversion>.
    Related source file is "/home/ise/Xillinx_host/Lab1/FPCVT.v".
    Found 13-bit adder for signal <twosComplement[12]_GND_2_o_add_3_OUT> create
    Summary:
        inferred   1 Adder/Subtractor(s).
```

```
        inferred   2 Multiplexer(s).
Unit <signMagConversion> synthesized.

Synthesizing Unit <bitExtraction>.
    Related source file is "/home/ise/Xillinx_host/Lab1/FPCVT.v".
WARNING:Xst:647 - Input <signMagnitude<12:12>> is never used. This port will be preserved
    Summary:
        inferred  20 Multiplexer(s).
Unit <bitExtraction> synthesized.

Synthesizing Unit <rounding>.
    Related source file is "/home/ise/Xillinx_host/Lab1/FPCVT.v".
    Found 3-bit adder for signal <exp[2]_GND_4_o_add_3_OUT> created at line 121.
    Found 5-bit adder for signal <n0024> created at line 122.
    Found 5-bit adder for signal <significand[4]_GND_4_o_add_7_OUT> created at line 128.
    Summary:
        inferred   2 Adder/Subtractor(s).
        inferred   8 Multiplexer(s).
Unit <rounding> synthesized.

=========================================================================
HDL Synthesis Report

Macro Statistics
# Adders/Subtractors                                   : 3
 13-bit adder                                          : 1
 3-bit adder                                           : 1
 5-bit adder                                           : 1
# Multiplexers                                         : 30
 1-bit 2-to-1 multiplexer                              : 7
 13-bit 2-to-1 multiplexer                             : 2
 3-bit 2-to-1 multiplexer                              : 9
 5-bit 2-to-1 multiplexer                              : 12

=========================================================================
INFO:Xst:1767 - HDL ADVISOR - Resource sharing has identified that some arithmetic operati

=========================================================================
*                      Advanced HDL Synthesis                           *
=========================================================================


=========================================================================
Advanced HDL Synthesis Report

Macro Statistics
# Adders/Subtractors                                   : 3
 13-bit adder                                          : 1
```

```
 13-bit adder                                          : 1
 3-bit adder                                           : 1
 5-bit adder                                           : 1
# Multiplexers                                         : 30
 1-bit 2-to-1 multiplexer                              : 7
 13-bit 2-to-1 multiplexer                             : 2
 3-bit 2-to-1 multiplexer                              : 9
 5-bit 2-to-1 multiplexer                              : 12

=========================================================================

=========================================================================
*                            Low Level Synthesis                        *
=========================================================================

Optimizing unit <FPCVT> ...

Optimizing unit <signMagConversion> ...

Optimizing unit <rounding> ...

Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block FPCVT, actual ratio is 1.

Final Macro Processing ...

=========================================================================
Final Register Report

Found no macro
=========================================================================

=========================================================================
*                             Partition Report                          *
=========================================================================

Partition Implementation Status
-------------------------------

  No Partitions were found in this design.

-------------------------------

=========================================================================
*                              Design Summary                           *
=========================================================================
```

```
Top Level Output File Name         : FPCVT.ngc

Primitive and Black Box Usage:
------------------------------
# BELS                             : 86
#      GND                         : 1
#      INV                         : 11
#      LUT1                        : 1
#      LUT4                        : 6
#      LUT5                        : 8
#      LUT6                        : 35
#      MUXCY                       : 11
#      VCC                         : 1
#      XORCY                       : 12
# IO Buffers                       : 22
#      IBUF                        : 13
#      OBUF                        : 9

Device utilization summary:
---------------------------

Selected Device : 6slx16csg324-3


Slice Logic Utilization:
 Number of Slice LUTs:                   61  out of   9112     0%
    Number used as Logic:                61  out of   9112     0%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:     61
   Number with an unused Flip Flop:      61  out of     61   100%
   Number with an unused LUT:             0  out of     61     0%
   Number of fully used LUT-FF pairs:     0  out of     61     0%
   Number of unique control sets:         0

IO Utilization:
 Number of IOs:                          22
 Number of bonded IOBs:                  22  out of    232     9%

Specific Feature Utilization:

---------------------------
Partition Resource Summary:
---------------------------

  No Partitions were found in this design.
```

```
--------------------------


=========================================================================
Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
------------------
No clock signals found in this design

Asynchronous Control Signals Information:
----------------------------------------
No asynchronous control signals found in this design

Timing Summary:
---------------
Speed Grade: -3

   Minimum period: No path found
   Minimum input arrival time before clock: No path found
   Maximum output required time after clock: No path found
   Maximum combinational path delay: 14.450ns

Timing Details:
---------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default path analysis
  Total number of paths / destination ports: 26837 / 9
-------------------------------------------------------------------------
Delay:               14.450ns (Levels of Logic = 10)
  Source:            D<12> (PAD)
  Destination:       F<4> (PAD)

  Data Path: D<12> to F<4>
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             15   1.222   1.086  D_12_IBUF (D_12_IBUF)
     LUT6:I4->O            13   0.203   1.277  smg/twosComplement[12]_PWR_2_o_equal_1_o1
     LUT6:I1->O            17   0.203   1.372  smg/Mmux_signMagnitude121 (tempSignMag<8>)
     LUT6:I1->O             1   0.203   0.944  b_ext/Mmux_significand82 (b_ext/Mmux_signi
```

```
================================================================================
Timing constraint: Default path analysis
  Total number of paths / destination ports: 26837 / 9
--------------------------------------------------------------------------------
Delay:               14.450ns (Levels of Logic = 10)
  Source:            D<12> (PAD)
  Destination:       F<4> (PAD)

  Data Path: D<12> to F<4>
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             15   1.222   1.086  D_12_IBUF (D_12_IBUF)
     LUT6:I4->O            13   0.203   1.277  smg/twosComplement[12]_PWR_2_o_equal_
     LUT6:I1->O            17   0.203   1.372  smg/Mmux_signMagnitude121 (tempSignMa
     LUT6:I1->O             1   0.203   0.944  b_ext/Mmux_significand82 (b_ext/Mmux_
     LUT6:I0->O             1   0.203   0.808  b_ext/Mmux_significand85_SW0 (N10)
     LUT6:I3->O             5   0.205   0.962  b_ext/Mmux_significand85 (tempSignifi
     LUT4:I0->O             1   0.203   0.944  rnd/Mmux_significand[4]_BUS_0002_mux_
     LUT6:I0->O             5   0.203   1.059  rnd/Mmux_significand[4]_BUS_0002_mux_
     LUT6:I1->O             1   0.203   0.579  rnd/Mmux_newSignificand41 (F_3_OBUF)
     OBUF:I->O                  2.571          F_3_OBUF (F<3>)
    ----------------------------------------
    Total                      14.450ns (5.419ns logic, 9.031ns route)
                                        (37.5% logic, 62.5% route)

================================================================================

Cross Clock Domains Report:
--------------------------

================================================================================


Total REAL time to Xst completion: 20.00 secs
Total CPU time to Xst completion: 18.04 secs

-->


Total memory usage is 377712 kilobytes

Number of errors   :    0 (   0 filtered)
Number of warnings :    1 (   0 filtered)
Number of infos    :    1 (   0 filtered)
```

4.3 Map Report

```
Release 14.7 Map P.20131013 (lin64)
Xilinx Mapping Report File for Design 'FPCVT'

Design Information
------------------
Command Line   : map -intstyle ise -p xc6slx16-csg324-3 -w -logic_opt off -ol
high -t 1 -xt 0 -register_duplication off -r 4 -global_opt off -mt off -ir off
-pr off -lc off -power off -o FPCVT_map.ncd FPCVT.ngd FPCVT.pcf
Target Device  : xc6slx16
Target Package : csg324
Target Speed   : -3
Mapper Version : spartan6 -- $Revision: 1.55 $
Mapped Date    : Sun Apr 18 20:49:47 2021

Design Summary
--------------
Number of errors:      0
Number of warnings:    0
Slice Logic Utilization:
  Number of Slice Registers:                     0 out of  18,224    0%
  Number of Slice LUTs:                         59 out of   9,112    1%
    Number used as logic:                       58 out of   9,112    1%
      Number using O6 output only:              45
      Number using O5 output only:              11
      Number using O5 and O6:                    2
      Number used as ROM:                        0
    Number used as Memory:                       0 out of   2,176    0%
    Number used exclusively as route-thrus:      1
      Number with same-slice register load:      0
      Number with same-slice carry load:         1
      Number with other load:                    0

Slice Logic Distribution:
  Number of occupied Slices:                    19 out of   2,278    1%
  Number of MUXCYs used:                        12 out of   4,556    1%
  Number of LUT Flip Flop pairs used:           59
    Number with an unused Flip Flop:            59 out of      59  100%
    Number with an unused LUT:                   0 out of      59    0%
```

```
    Number of fully used LUT-FF pairs:           0 out of      59    0%
    Number of slice register sites lost
      to control set restrictions:               0 out of  18,224    0%

  A LUT Flip Flop pair for this architecture represents one LUT paired with
  one Flip Flop within a slice.  A control set is a unique combination of
  clock, reset, set, and enable signals for a registered element.
  The Slice Logic Distribution report is not meaningful if the design is
  over-mapped for a non-slice resource or if Placement fails.

IO Utilization:
  Number of bonded IOBs:                      22 out of     232    9%

Specific Feature Utilization:
  Number of RAMB16BWERs:                       0 out of      32    0%
  Number of RAMB8BWERs:                        0 out of      64    0%
  Number of BUFIO2/BUFIO2_2CLKs:               0 out of      32    0%
  Number of BUFIO2FB/BUFIO2FB_2CLKs:           0 out of      32    0%
  Number of BUFG/BUFGMUXs:                     0 out of      16    0%
  Number of DCM/DCM_CLKGENs:                   0 out of       4    0%
  Number of ILOGIC2/ISERDES2s:                 0 out of     248    0%
  Number of IODELAY2/IODRP2/IODRP2_MCBs:       0 out of     248    0%
  Number of OLOGIC2/OSERDES2s:                 0 out of     248    0%
  Number of BSCANs:                            0 out of       4    0%
  Number of BUFHs:                             0 out of     128    0%
  Number of BUFPLLs:                           0 out of       8    0%
  Number of BUFPLL_MCBs:                       0 out of       4    0%
  Number of DSP48A1s:                          0 out of      32    0%
  Number of ICAPs:                             0 out of       1    0%
  Number of MCBs:                              0 out of       2    0%
  Number of PCILOGICSEs:                       0 out of       2    0%
  Number of PLL_ADVs:                          0 out of       2    0%
  Number of PMVs:                              0 out of       1    0%
  Number of STARTUPs:                          0 out of       1    0%
  Number of SUSPEND_SYNCs:                     0 out of       1    0%

Average Fanout of Non-Clock Nets:              3.79
```

```
Peak Memory Usage:  665 MB
Total REAL time to MAP completion:  25 secs
Total CPU time to MAP completion:   23 secs

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Section 1 - Errors
------------------

Section 2 - Warnings
--------------------
WARNING:Security:42 - Your software subscription period has lapsed.
version of Xilinx tools will continue to function, but you no longe
Xilinx software updates or new releases.

Section 3 - Informational
-------------------------
INFO:Security:54 - 'xc6slx16' is a WebPack part.
INFO:MapLib:562 - No environment variables are currently set.
INFO:LIT:244 - All of the single ended outputs in this design are u
   rate limited output drivers. The delay on speed critical single
   can be dramatically reduced by designating them as fast outputs.
INFO:Pack:1716 - Initializing temperature to 85.000 Celsius. (defau
```

```
   0.000 to 85.000 Celsius)
INFO:Pack:1720 - Initializing voltage to 1.140 Volts. (default - Range: 1.140 to
   1.260 Volts)
INFO:Map:215 - The Interim Design Summary has been generated in the MAP Report
   (.mrp).
INFO:Pack:1650 - Map created a placed design.

Section 4 - Removed Logic Summary
---------------------------------
   2 block(s) optimized away

Section 5 - Removed Logic
-------------------------

Optimized Block(s):
TYPE            BLOCK
GND             XST_GND
VCC             XST_VCC

To enable printing of redundant blocks removed and signals merged, set the
detailed map report option and rerun map.

Section 6 - IOB Properties
--------------------------

+-----------------------------------------------------------------------------------------
| IOB Name                           | Type             | Direction | IO Standard
|                                    |                  |           |
+-----------------------------------------------------------------------------------------
| D<0>                               | IOB              | INPUT     | LVCMOS25
| D<1>                               | IOB              | INPUT     | LVCMOS25
| D<2>                               | IOB              | INPUT     | LVCMOS25
| D<3>                               | IOB              | INPUT     | LVCMOS25
| D<4>                               | IOB              | INPUT     | LVCMOS25
| D<5>                               | IOB              | INPUT     | LVCMOS25
| D<6>                               | IOB              | INPUT     | LVCMOS25
| D<7>                               | IOB              | INPUT     | LVCMOS25
| D<8>                               | IOB              | INPUT     | LVCMOS25
```

D<10>	IOB	INPUT	LVCMOS25
D<11>	IOB	INPUT	LVCMOS25
D<12>	IOB	INPUT	LVCMOS25
E<0>	IOB	OUTPUT	LVCMOS25
E<1>	IOB	OUTPUT	LVCMOS25
E<2>	IOB	OUTPUT	LVCMOS25
F<0>	IOB	OUTPUT	LVCMOS25
F<1>	IOB	OUTPUT	LVCMOS25
F<2>	IOB	OUTPUT	LVCMOS25
F<3>	IOB	OUTPUT	LVCMOS25
F<4>	IOB	OUTPUT	LVCMOS25
S	IOB	OUTPUT	LVCMOS25

Section 7 - RPMs

Section 8 - Guide Report

Guide not run on this design.

Section 9 - Area Group and Partition Summary

Partition Implementation Status

  No Partitions were found in this design.

Area Group Information

  No area groups were found in this design.

```
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  No Partitions were found in this design.

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Area Group Information
----------------------

  No area groups were found in this design.

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Section 10 - Timing Report
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A logic-level (pre-route) timing report can be generated by using Xilinx static
timing analysis tools, Timing Analyzer (GUI) or TRCE (command line), with the
mapped NCD and PCF files. Please note that this timing report will be generated
using estimated delay information. For accurate numbers, please generate a
timing report with the post Place and Route NCD file.

For more information about the Timing Analyzer, consult the Xilinx Timing
Analyzer Reference Manual; for more information about TRCE, consult the Xilinx
Command Line Tools User Guide "TRACE" chapter.

Section 11 - Configuration String Details
-----------------------------------------
Use the "-detail" map option to print out Configuration Strings

Section 12 - Control Set Information
------------------------------------
Use the "-detail" map option to print out Control Set Information.

Section 13 - Utilization by Hierarchy
-------------------------------------
Use the "-detail" map option to print out the Utilization by Hierarchy section.
```

5 Conclusion

In this lab, I made a floating point converter that converted a 13-bit linear encoding into a 9-bit FP representation. I took advantage of the slides and recordings during lectures to implemented it. The slides and recordings were extremely helpful especially with setup and syntax because it was my first time using Verilog. In addition, specifically with syntax, I used the internet a ton to figure out the small details.

Some difficulties I ran into included not knowing what should be a wire vs a register, but with the slides, I believe I figured it out and use the assumption that if it is not going to change, I can use a wire. In addition, I had some difficulties figuring out why my simulation method was ModelSim instead of ISim, but looking back at the slides helped me figure out that my settings were incorrect. Lastly, with respect to the implementation, figuring out the edge cases and the proper way to deal with them was tough, for example, an input of all 1's, as well as drawing the schematics for the modules were extremely difficult.