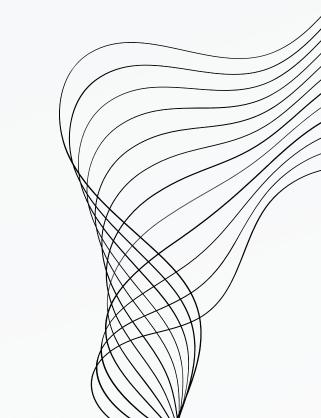
3º BIMESTRE FLIP FLOP

Eduardo Evangelista - 149382 Pedro Edom - 149349



CONTENT

01

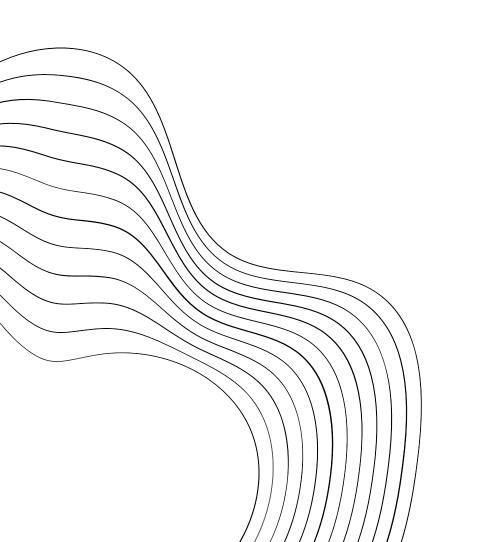
ESTRUTURA DO TRABALHO

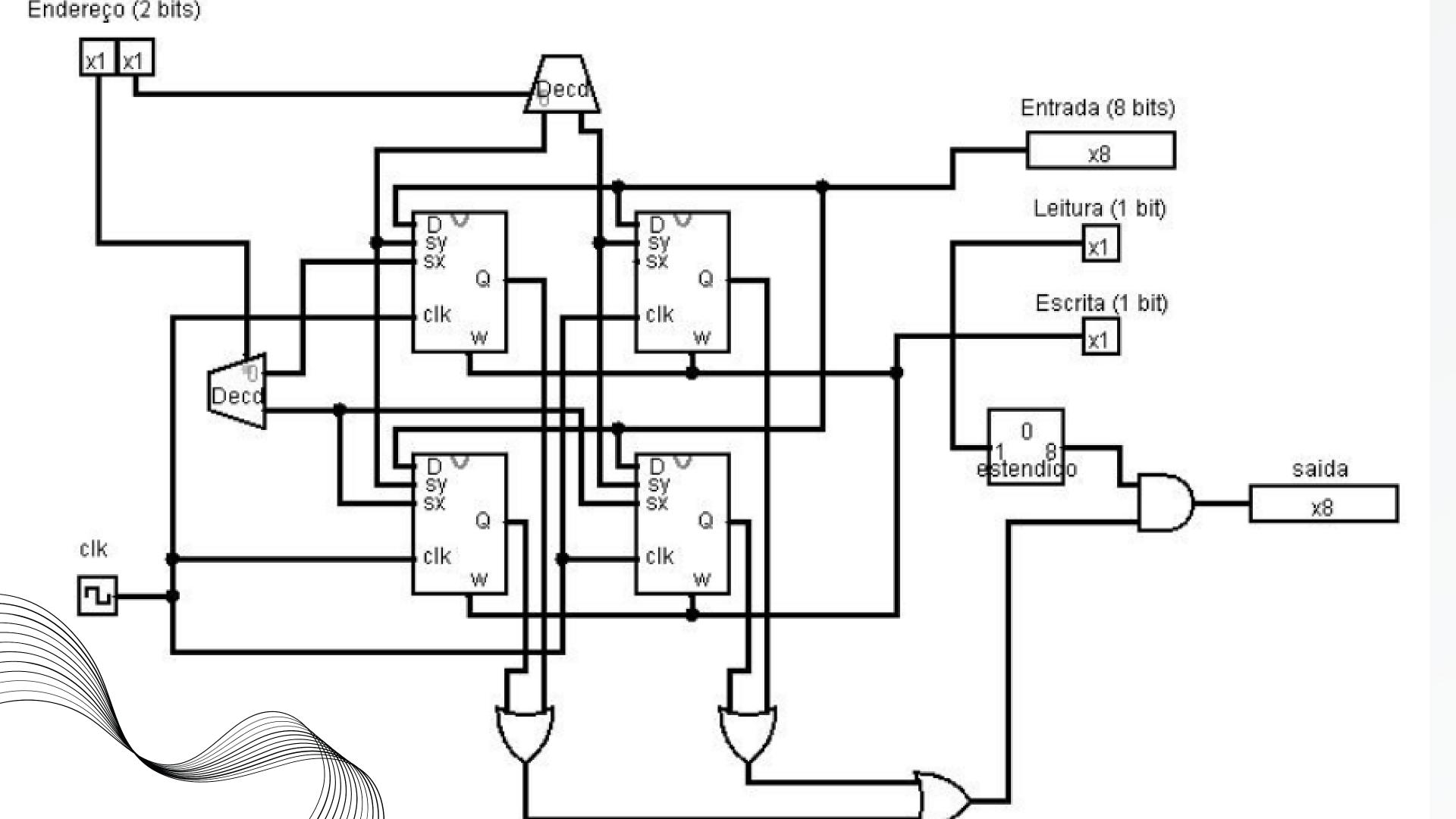
02

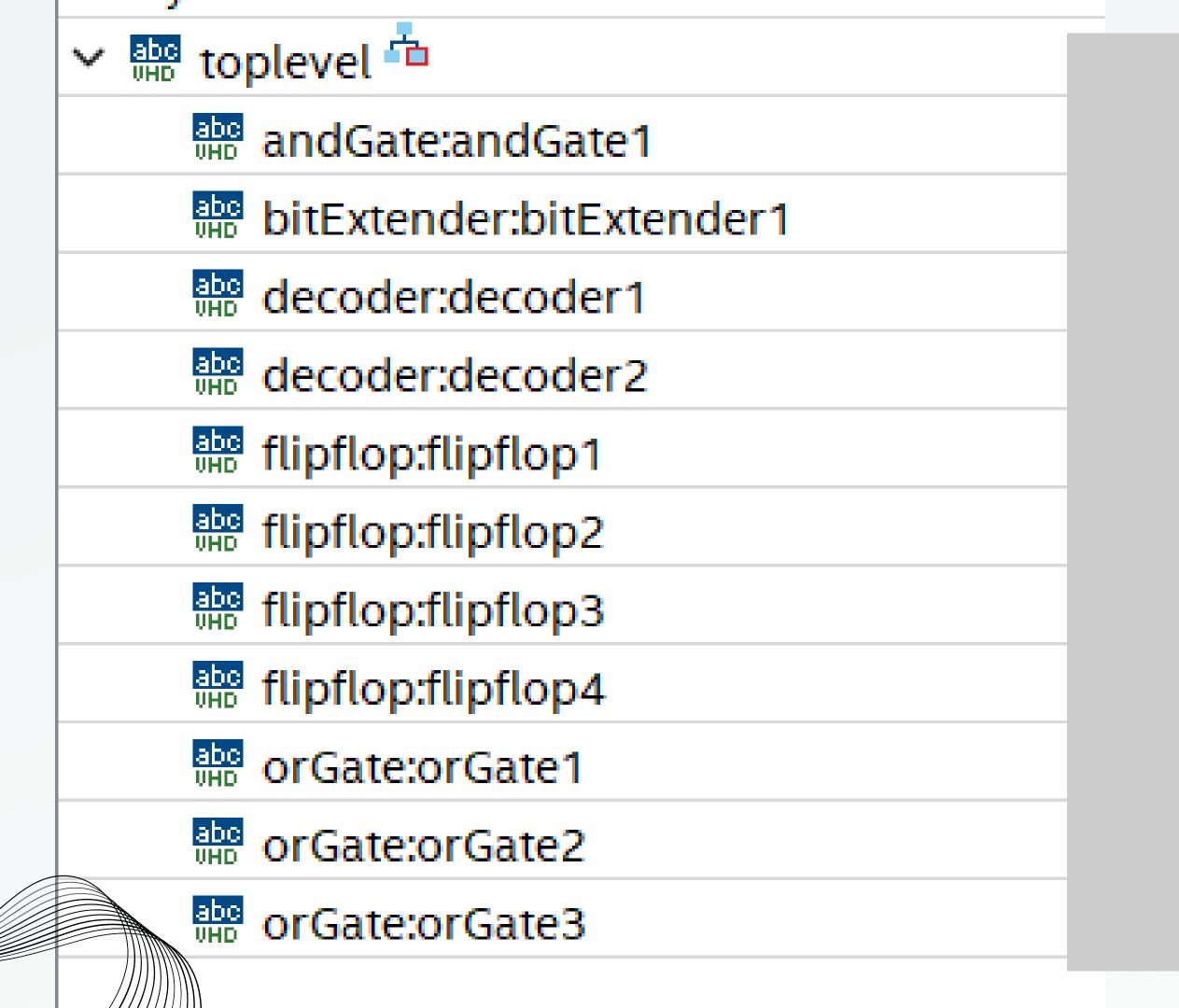
RTL VIEW

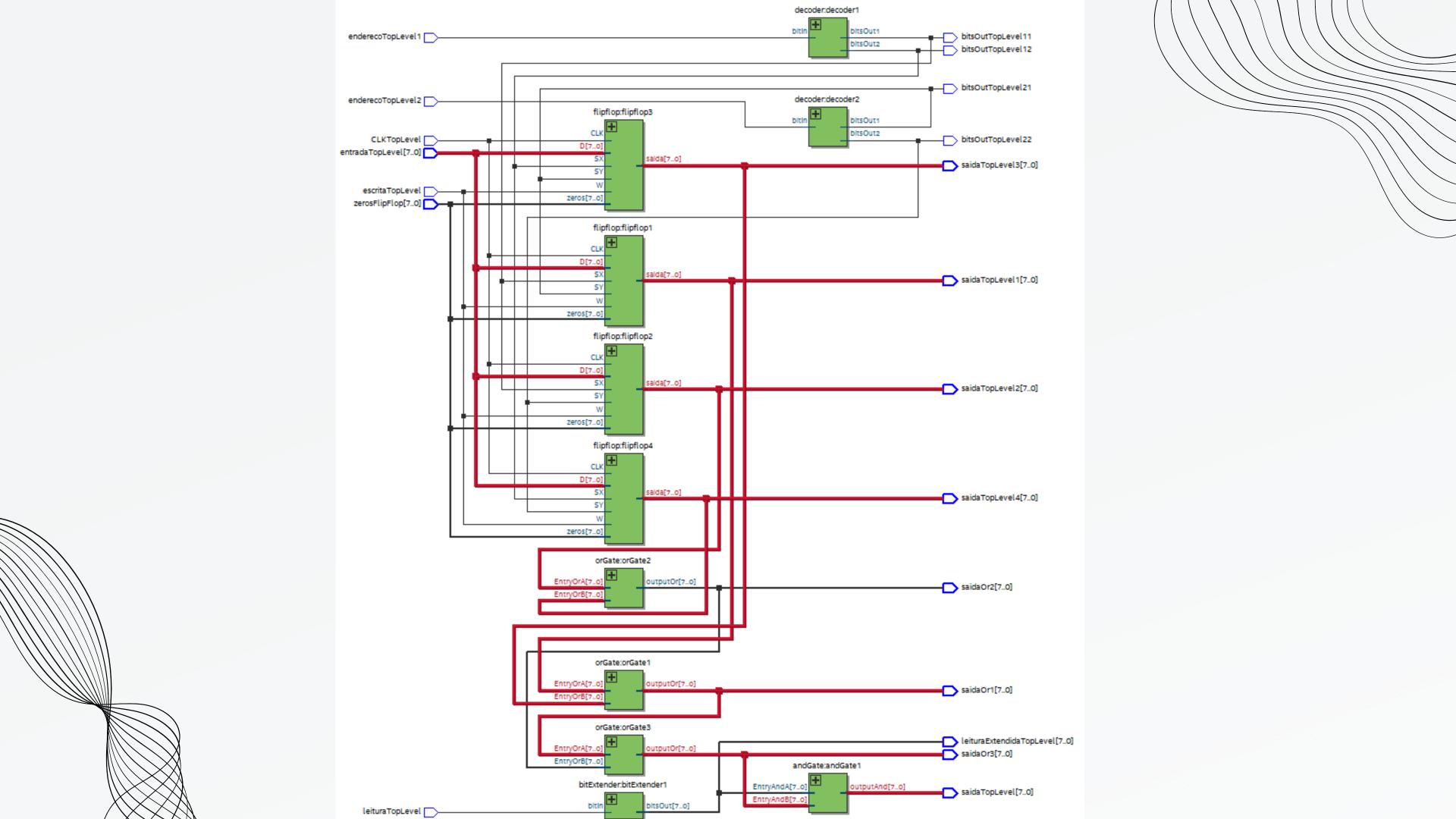
03

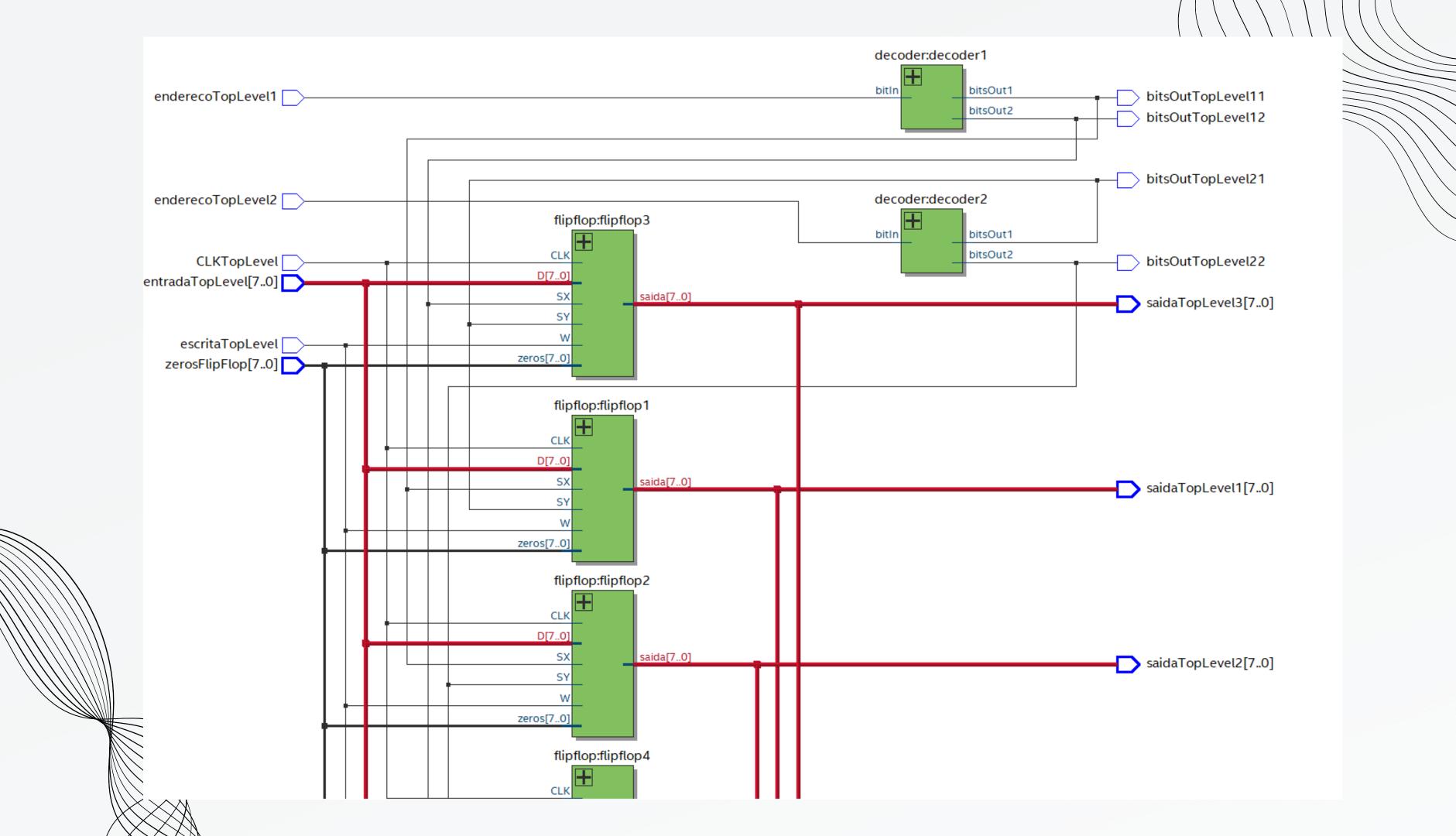
CÓDIGO FLIPFLOP

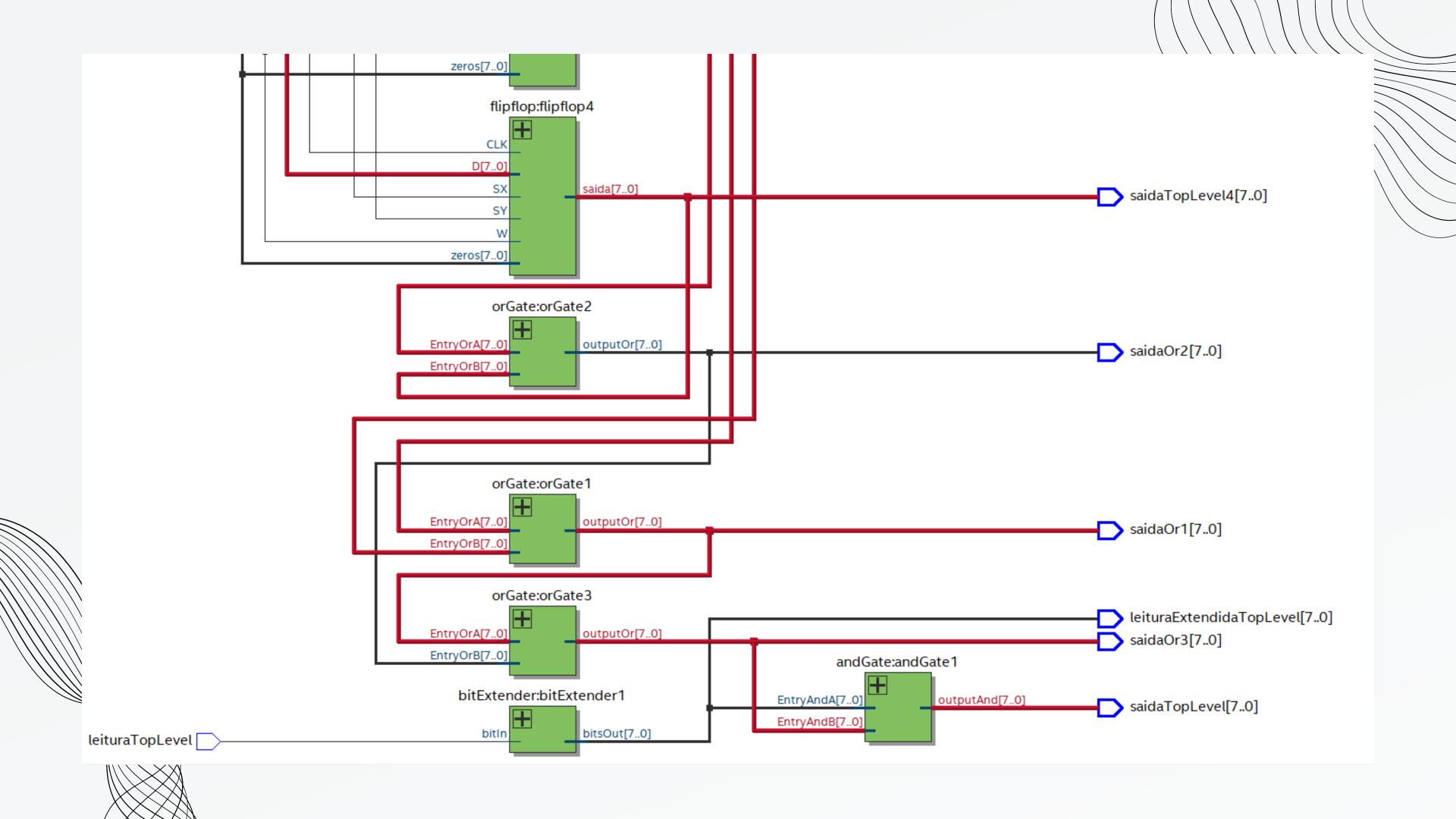


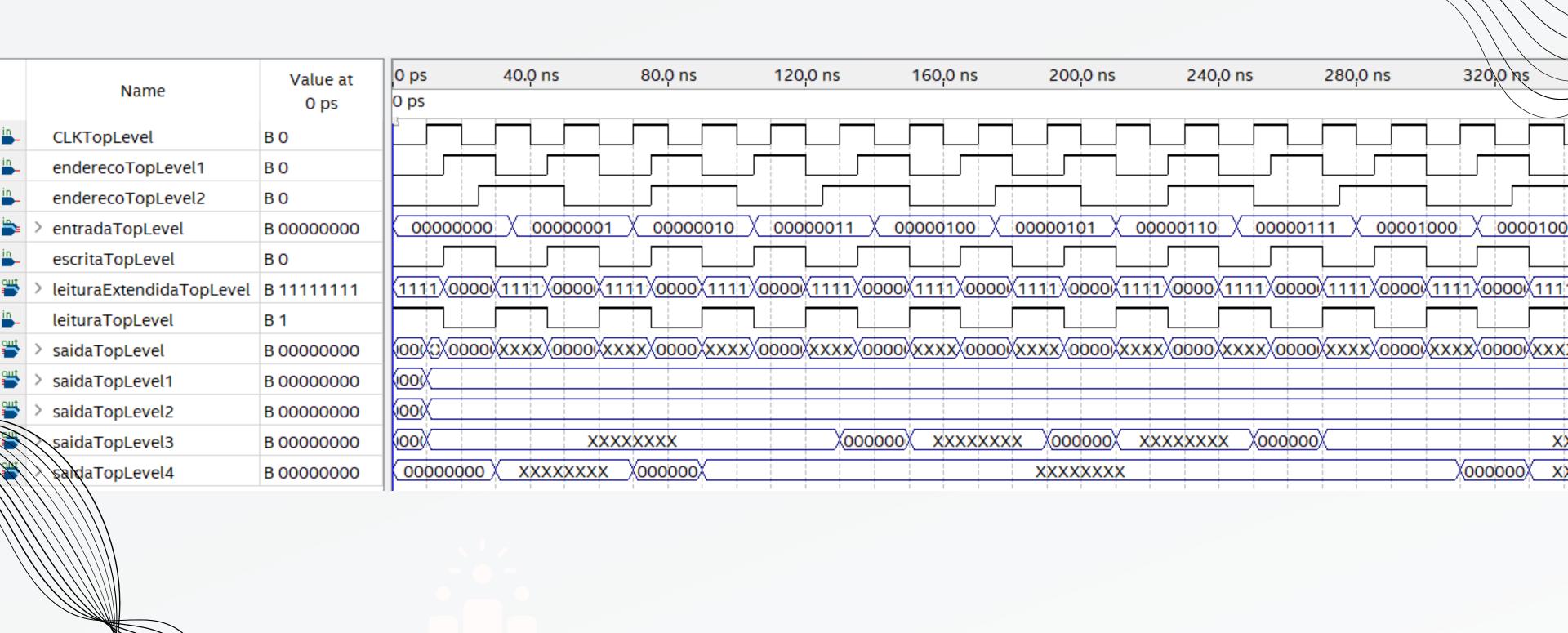












```
⊟begin
⊟process (CLK)
 begin
    if(rising_edge(CLK)) then
       if (W = '1') and SX = '1' and SY = '1') then
          Q \leq D;
       elsif((W = '0') and (SX = '1') and (SY = '1')) then
           saida \leq Q;
       else
           saida <= zeros;
       end if:
    end if;
 end process;
 end comportamento;
```

```
-- definir a entidade
⊟entity toplevel is
      port (
          -- Entrada
          entradaTopLevel,zerosFlipFlop: in std_logic_vector(7 downto 0)
          leituraTopLevel: in std_logic;
          escritaTopLevel: in std_logic;
saidaTopLevel: out std_logic_vector(7 downto 0);
leituraExtendidaTopLevel: buffer std_logic_vector(7 downto 0);
          -- Enderecos
          enderecoTopLevel1: in std_logic;
          enderecoTopLevel2: in std_logic;
          -- clock
          CLKTopLevel: in std_logic;
          -- Decoder 1
          bitsOutTopLevel11: buffer std_logic;
          bitsOutTopLevel12: buffer std_logic;
          -- Decoder 2
          bitsOutTopLevel21: buffer std_logic;
          bitsOutTopLevel22: buffer std_logic;
          -- Flipflop1
          saidaTopLevel1: buffer std_logic_vector(7 downto 0);
          -- Flipflop2
          saidaTopLevel2: buffer std_logic_vector(7 downto 0);
          -- Flipflop3
          saidaTopLevel3: buffer std_logic_vector(7 downto 0);
          -- Flipflop4
          saidaTopLevel4: buffer std_logic_vector(7 downto 0);
          -- OR
```

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35 36 37

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```
-- OR
saidaOr1: buffer std_logic_vector(7 downto 0);
saidaOr2: buffer std_logic_vector(7 downto 0);
saidaOr3: buffer std_logic_vector(7 downto 0);
saidaOr3: buffer std_logic_vector(7 downto 0)

7 downto 0)
47 definition of the control of the cont
```

OBRIGADO!

