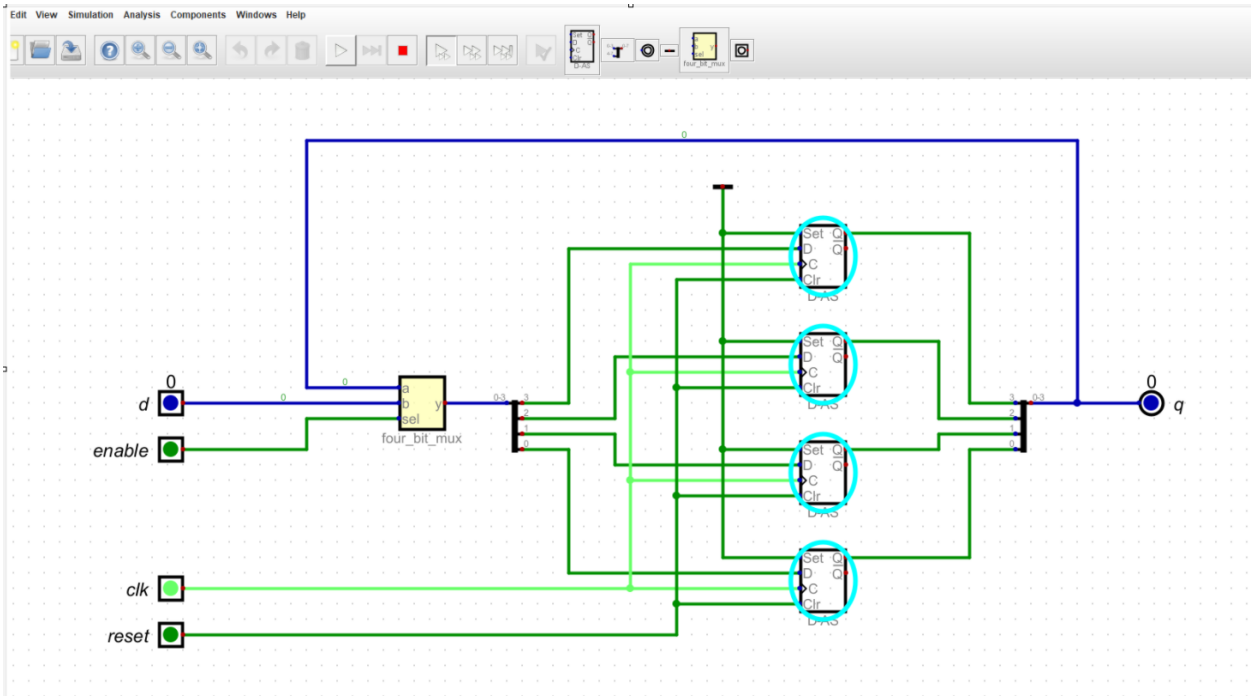
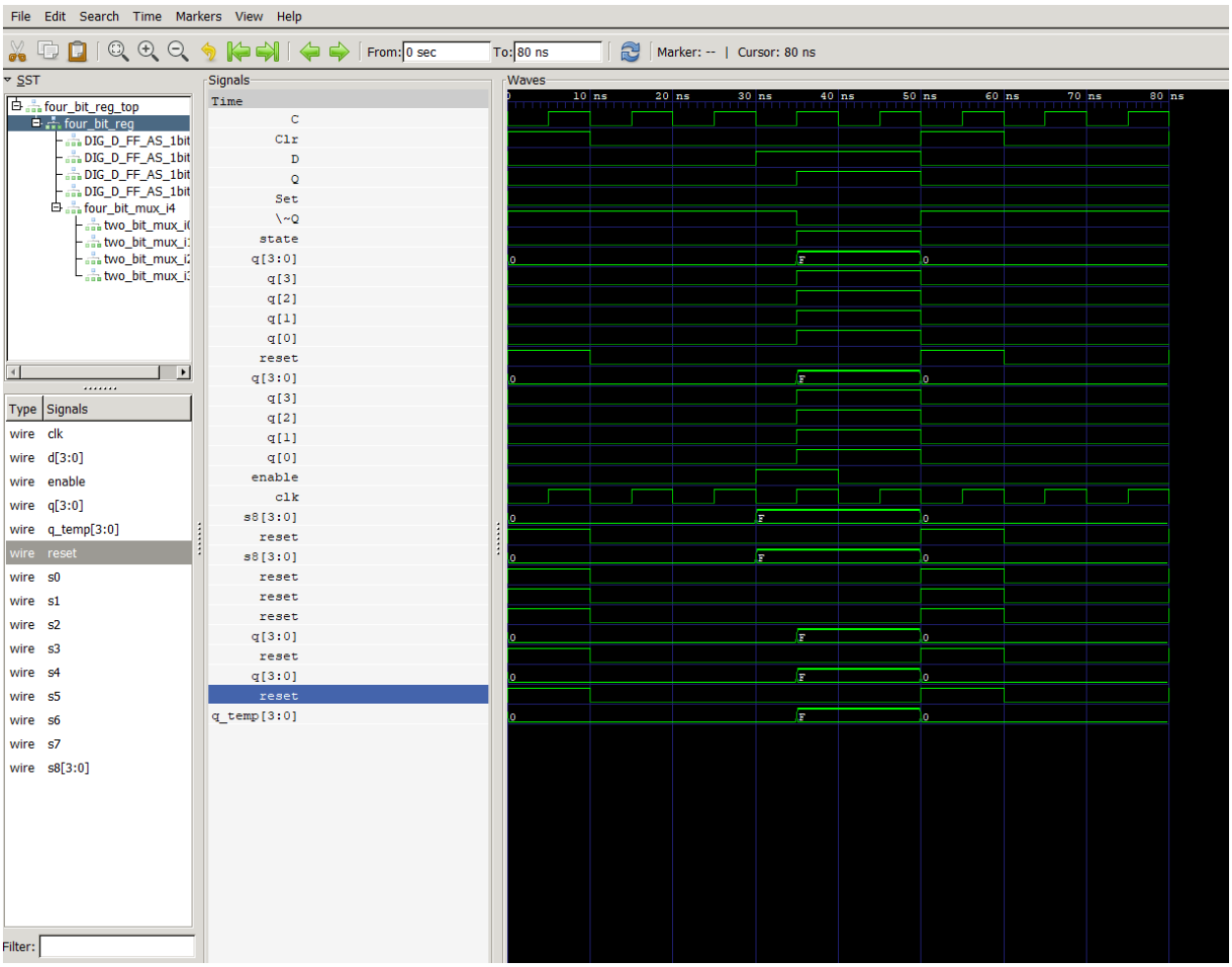
Objectives:

By the end of this lab, you will be able to:

- Build and test a **4-bit D register** with enable.
- 

- Construct a **4-bit up counter**.
- Create a **16-word, 4-bit RAM**.
- Build and simulate a **"Brainless CPU"**, which lacks a controller.
- Act as the **controller** for the CPU by manually manipulating signals.
- Testing the circuit is shown below. You are showing the electrical signal, traveling through the circuit, to then reach the intended point and affect it with the electricity flowing through the circuit.

- 

Task 3-1: 4-Bit D Register with Enable

- **Design** a **4-bit register** using **D flip-flops** with an **enable** signal.
- **Simulate** it in **Digital**, ensuring it loads values correctly.
- **Export** it to Verilog and modify **four_bit_reg_stim.v** to run 8 tests.
- **Run** Verilog simulation using **Icarus Verilog (iverilog)** and analyze waveforms using **GTKWave**.

Task 3-2: 4-Bit Program Counter

- **Build** a **4-bit counter** that increments from **0 to 15** using the **4-bit register** and a **4-bit incrementer**.
- The counter **stops counting** when **enable = 0**.
- **Simulate and test** in **Digital**, ensuring correct functionality.

Task 3-3: 4-Bit RAM with 16 Words

- **Design a RAM module** with:
    - **4-bit words** and **16 memory locations**.
    - A **4-bit address bus**.
    - A **write-enable signal**.
- **Initialize** RAM with **ram_vals.hex** in **Digital**.
- **Simulate and verify** correct read/write operations.

Task 3-4: Assemble the "Brainless CPU"

- **Combine previous circuits** (ALU, Register, RAM, Multiplexers) to create a **basic CPU**.
- **Manually control** operations by setting control signals.
- **Test it** by performing an **addition operation (3 + 5 = 8)** and verifying the result.

Task 3-5: Verilog Simulation of the CPU

- **Export** the brainless CPU to **Verilog** and modify it to initialize RAM.
- **Run simulation** in **Icarus Verilog** and view waveforms in **GTKWave**.
- **Verify the 3+5 addition operation** in Verilog.

Task 3-6: Additional Tests

- Create **three new test cases**:
    1. **External RAM Write**: Store a value from **data_in** into RAM.
    2. **Internal RAM Write**: Store a value from **Accumulator** into RAM.
    3. **Additional ALU Operations**: Demonstrate two new ALU functions.
- **Modify test stimulus files** and verify results.

Task 3-7: (Optional) Video Presentation

- Create a **video demonstration** explaining the design and showing simulations.

Final Submission:

- Submit a **zip file** of the **Lab3 directory**.
- Submit a **PDF report** with screenshots of circuit schematics and waveforms.

Key Takeaways:

- You built essential **digital circuits** like **registers, counters, RAM, and a CPU**.
- You learned to **manually control** a CPU before implementing an **automated controller** in Lab 4.
- You practiced **Verilog simulation**, **GTKWave analysis**, and **Digital software usage**.