Computer Architecture and Networks

Computer Function and Interconnection

Section A

1) The buses that connect different parts of the processor can be hierarchical to improve the performance (True)

2) Instead of hard-wiring units, software is used to interpret and execute instructions in a general purpose system (True)

3) The program counter stores the address of the next instruction to be executed (True)

4) The fetched instructions are stored in the Accumulator register (False)
5) Interrupts are part of the program that can cause the processor to stop (True)

6) All interrupts are handled by the interrupt handler (True)

7) Multiple interrupts cannot be handled by the processor (True)

8) I/O modules can have direct access to the memory (False)

9) If a module needs to transmit data, the data is sent through the buses immediately (False)
10) Data transfer between modules/units cannot be controlled (False)

11) The PCI bus is used for high speed I/O transfers (True)

12) Interrupt request is a PCI command (True)

Section B

1) **How are data and instructions stored in the Von Neumann architecture?**
   Unified read-write memory

2) **Which are the main stages of an instruction cycle?**
   Fetch and execute cycle

3) **Where is the fetched instruction stored?**
   Instruction buffer register

4) **Which of the following is a type of interrupt?**
All (program interrupt, hardware/power failure, I/O interrupt)

5) **Which of the following approaches is used to handle multiple interrupts?**
Parallel interrupt processing

6) **Which of these interconnection wires is not in the bus structure?**
Instruction lines

7) **Which of the following is a bus arbitration scheme?**
All (Priority, round-robin, first come first serve)