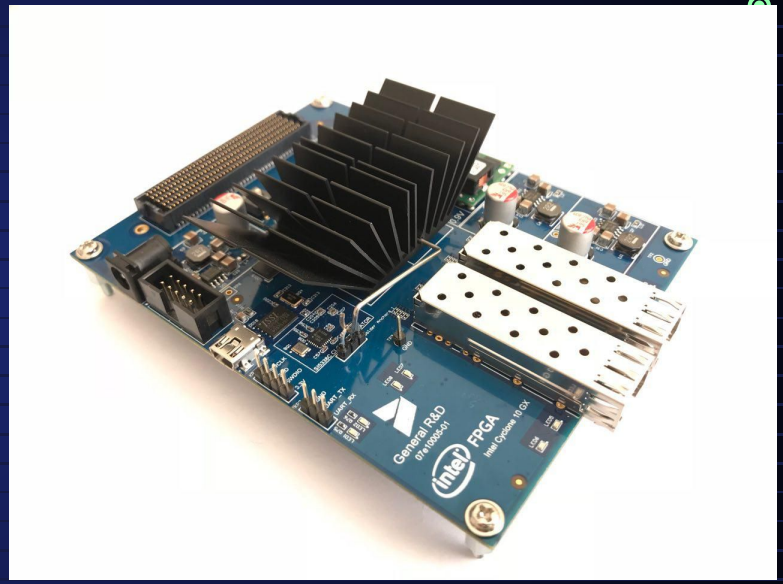
Intel Cyclone X: A High-Speed PCB Design

By Edreese Basharyar and Benjamin Molina

Overall Design

Key Aspects of Design include:

- Transmitter IC:
  - Intel Cyclone 10 GX Series
  - Submodel (10CX105)
- Receiver IC:
  - Differential Receiver
  - Comparator to sense high-speed changes in voltage
  - D-Flip Flops using 1 GHz clock signal
  - Buffers to eliminate noise in output waveforms
- Specialized Standards
  - LVDS (Low Voltage Differential Signaling)
  - Uses differential voltage to transmit high-speed data with low power consumption



Transmitter Specifications

Package Plan Specifications

- UBGA (Ultra FineLine Ball Grid Array)
- Total of 484-pins
- 188 GPIOs, 70 LVDS pairs, 6 Transceiver IOs, 220 gnd/pwr IOs
- Nominal Ball Pitch = 0.80 mm
- Minimum Ball Diameter (worst-case) = 0.45 mm
- Maximum Ball Diameter = .55 mm

Signaling Rate Specifications

- Maximum data rate of 1.434 Gbps per channel
- Design will use data rate of 1Gbps per channel
- Minimum rise/fall time = 20 ps
- Maximum rise/fall time = 130 ps

LVDS Specifications

- Bi-directional (can function as both transmitter & receiver)
- Nominal common-mode output voltage = 1.25 V
- Output common-mode voltage between 1.125 V and 1.375V
- Receiver input voltage between 1.0 V and 1.6 V
- Differential output voltage of .247 V and 0.6 V
- Measured assuming data rates > 700 Mbps

Package Outline Dimension Table

Symbol	Millimeters		
	Min.	Nom.	Max.
A	2.85	3.05	3.25
A1	0.35	0.40	0.45
A2	2.40	2.65	2.90
A3	1.45	1.50	1.55
D		19.00 BSC	
E		19.00 BSC	
b	0.45	0.50	0.55
e		0.80 BSC	

Figure 2: U484 Package Outline Specifications

Differential I/O Standards Specifications

Table 17. Differential I/O Standards Specifications for Intel Cyclone 10 GX Devices

Differential inputs are powered by V_{CCPT} which requires 1.8 V.

I/O Standard	V_{CCIO} (V)			V_{ID} (mV) (23)			$V_{ICM(DC)}$ (V)			V_{OD} (V) (24)			V_{OCM} (V) (24)		
	Min	Typ	Max	Min	Condition	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
LVDS (25)	1.71	1.8	1.89	100	V_{CM} = 1.25 V	—	0	D_{MAX} ≤700 Mbps	1.85	0.247	—	0.6	1.125	1.25	1.375
							1	D_{MAX} >700 Mbps	1.6						
RSDS (26)	1.71	1.8	1.89	100	V_{CM} = 1.25 V	—	0.3	—	1.4	0.1	0.2	0.6	0.5	1.2	1.4
Mini-LVDS (27)	1.71	1.8	1.89	200	—	600	0.4	—	1.325	0.25	—	0.6	1	1.2	1.4
LVPECL (28)	1.71	1.8	1.89	300	—	—	0.6	D_{MAX} ≤700 Mbps	1.7	—	—	—	—	—	—
							1	D_{MAX} >700 Mbps	1.6						

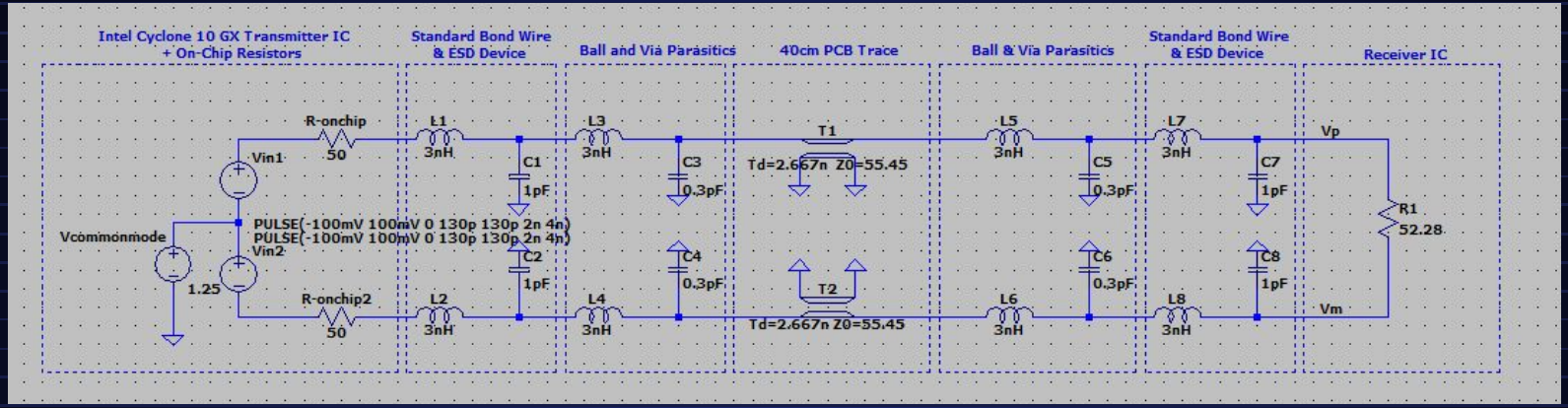
Figure 3: Differential I/O Standards for Intel Cyclone 10 GX Series

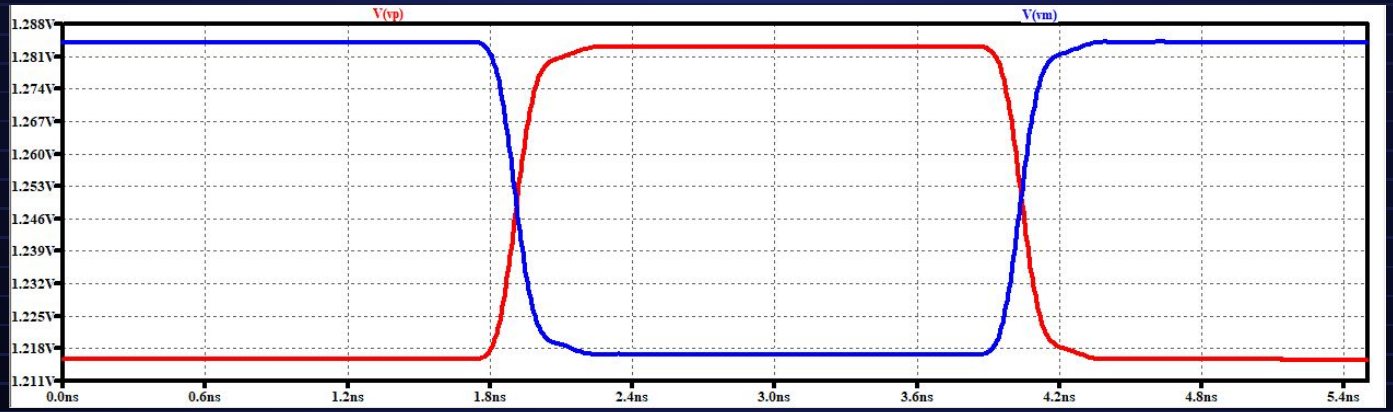
Design Calculations

The table on the right encompasses all the primary design calculations necessary for our high-speed system, with emphasis on the forward crosstalk coefficient (kfx), which is specified as zero due to the earlier design of the PCB layer stack-up ensuring a homogeneous medium for the signal layers.

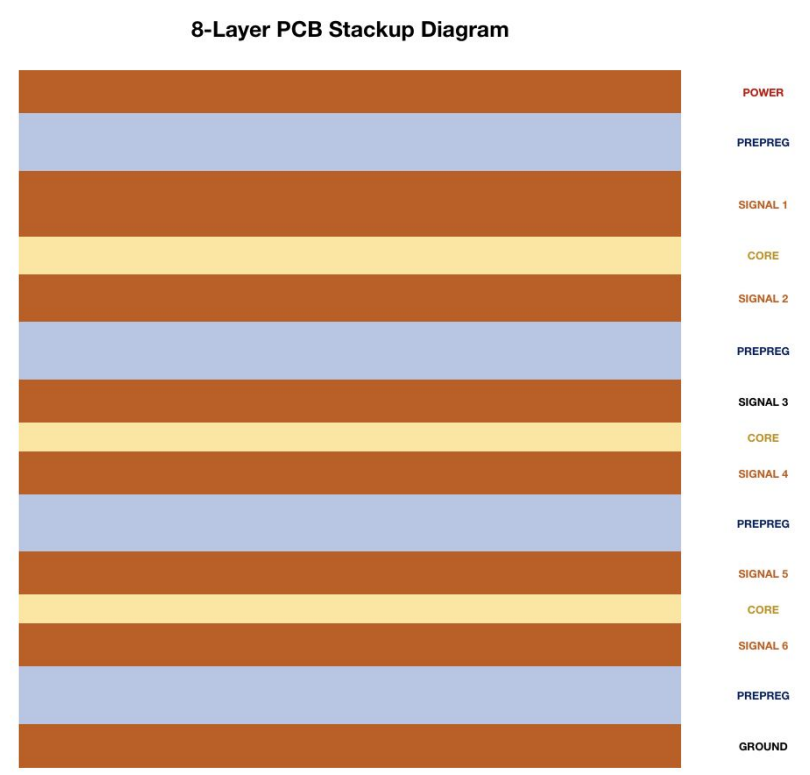
Hand Calculations of System	Value	Units
Capacitance for Parallel Lines in Same Layer	7.08	pF/m
Capacitance for Parallel Lines in Above Layer	14.16	pF/m
Capacitance to Ground Plane (worst-case)	91.95	pF/m
Differential Capacitance (Cd)	113.19	pF/m
Stray Capacitance (Cc)	7.08	pF/m
Total Capacitance of Line (C)	120.27	pF/m
Inductance of Line (L)	369.87	nH/m
Mutual Inductance (M)	21.77	nH/m
Odd-Mode Line Impedance (Zodd)	52.28	Ω
Impedance of Line (Zo)	55.45	Ω
Velocity of Signal on Line (v)	0.15	m/ns
Delay of Line (td)	2.667	ns
Resistance of Line (R)	2.24	Ω/m
Capactive Crosstalk Coefficient (kcx)	0.0588	
Inductive Crosstalk Coefficient (klx)	0.0588	
Forward Crosstalk Coefficient (kfx)	0	
Reverse Crosstalk Coefficient (krx)	0.0294	

Schematic and Simulations





Board Specifications



PCB Stackup Details:

- Utilizes 8 Layers
- Consists of 8 1oz. Copper Layers, 4 FR-4 7628 Prepreg Layers, and 3 Core Layers
- Thickness of Copper Layer = 1.4 mil
- Thickness of Prepreg Layer = 7 mil
- Thickness of Core Layer = 7.6 mil
- Overall PCB Thickness = 62 mil
- Designed for Homogenous Medium
- Forward Crosstalk is eliminated
- Reduces need for Crosstalk Control / Equalization

8 Layer PCB Stackup

Colors	Layers	Total Count	Total Length
	1oz Copper Layer (.0014")	8	0.0112"
	Prepreg Layer (.007")	4	0.028"
	Core Layer (.0076")	3	0.0228"
		15	0.062"

Timing and Synchronization

- Design will consist on mesochronous clock signals
  - Matching bit-rate and frequency for transmitter and receiver
  - Periodic clock signals with oscillation frequency of 1GHz
  - Closed-Loop Timing per line to address size and variation of the differential receiver
  - Two-level (binary) voltage system for inputs fed into comparator

Cost Analysis

The table below provides an approximate cost breakdown for the components intended for our high-speed design, with potential for future enhancements based on the extent to which we aim to optimize the overall design.

Cost Analysis	Price
Intel Cyclone 10 GX Series (10CX105)	$177.78
Cost of 8-Layer PCB Stackup	$.75/in^2
PCB Board	$50
Receiver IC	$40
Termination Resistor	$5
BGA-484 Adapter	$60

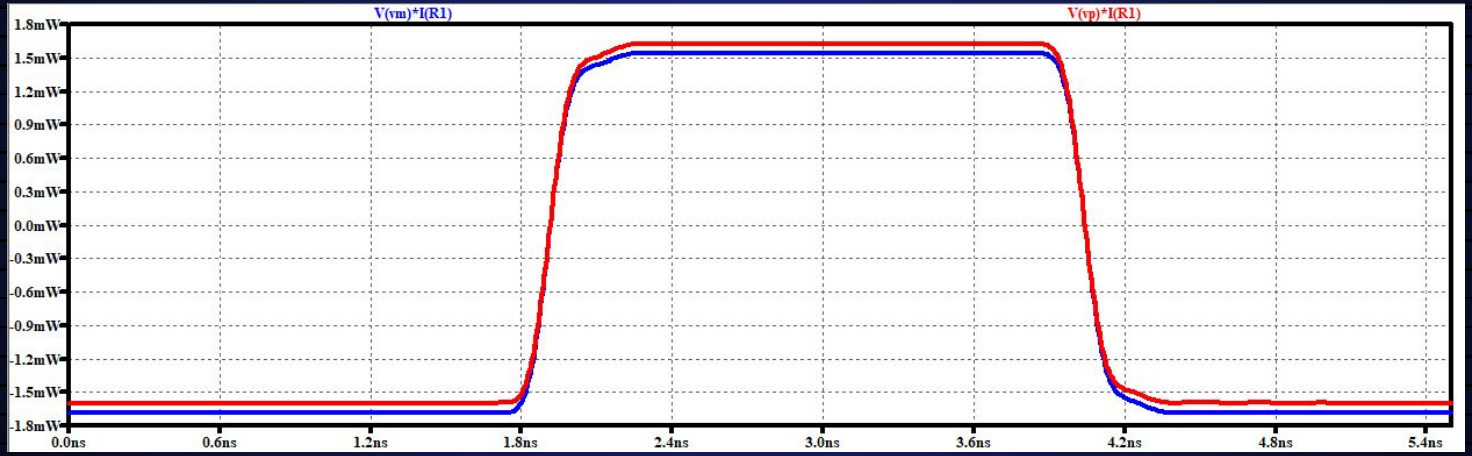
Noise Budget

The table below consists all the values involved in the noise budget in our design. Our final calculations for some of the values haven't been met to our standards, so we have decided to omit the values until the final design has been made.

Noise Budget	Values
Voltage Swing	800mV
Gross Margin	400mV
Net Margin	-
Reverse Crosstalk Coefficient	-0.0588-
Forward Crosstalk Coefficient	-
Receiver Offset	40mV
Transmitter Offset	10mV
Gaussian Noise	5mV
Power Supply Noise	0mV
VSNR	0mV
BER	-
MTBF	-
Kn	-

Power Analysis

The power consumption for the inputs before the differential receiver (comparator) based on the waveform shows a peak value for ~1.5mW for Vm & Vp, taking the current of the odd-mode termination resistor.



THANK YOU!