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# ECG 722: Mixed-Signal Circuit Design

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# Continuous Time K-Delta-1-Sigma (KD1S) ADC Design

## Project Objectives:

In this report, we will describe the design and implementation of the K-Delta-1-Sigma (KD1S) modulator as a replacement for the ADC seen in Figure 9.32 of the *CMOS Mixed-Signal Design* textbook. This approach utilizes a continuous-time topology, omitting the need for any switched-capacitors and non-overlapping clock signals. Each section of the report provides a comprehensive explanation of the components within the KD1S modulator. We constructed both first order and second-order topologies to observe the performances relative to the original ADC. The design is implemented with the C5 process, using a minimum transistor length of 600 nm, and a supply voltage of VDD = 5V. Out of the two designs, the first-order KD1S topology consists of 8 paths while our second-order KD1S topology consists of 4 paths and an additional amplifier.

## Overview of Design Performances:

| | 1st Order 8-Path KD1S Project Performance (1MHz) | | | | | |
|---|---|---|---|---|---|---|
| **OSR** | **64** | | **128** | | **256** | |
| **Mode** | **Serial** | **Parallel** | **Serial** | **Parallel** | **Serial** | **Parallel** |
| **$F_{s,new}$** | **807MHz** | **101MHz** | **807MHz** | **101MHz** | **807MHz** | **101MHz** |
| **SNR** | **39.72 dB** | **30.76 dB** | **46.12 dB** | **44.33 dB** | **48.17 dB** | **48.08 dB** |
| **$N_{eff}$** | **6.30 Bits** | **4.81 Bits** | **7.36 Bits** | **7.07 Bits** | **7.71 Bits** | **7.69 Bits** |
| **Bandwidth** | **6.30 MHz** | **6.30 MHz** | **3.15 MHz** | **3.15MHz** | **1.58MHz** | **1.57MHz** |
| **$P_{avg}$** | **50.94 mW** | | | | | |

*Table 1: 1st Order 8-Path KD1S Project Performance at 1MHz*

| | 2nd Order 4-Path KD1S Project Performance (1MHz) | | | | | |
|---|---|---|---|---|---|---|
| **OSR** | **32** | | **64** | | **128** | |
| **Mode** | **Serial** | **Parallel** | **Serial** | **Parallel** | **Serial** | **Parallel** |
| **$F_{s,new}$** | **403MHz** | **101MHz** | **403MHz** | **101MHz** | **403MHz** | **101MHz** |
| **SNR** | **43.41 dB** | **34.86 dB** | **53.92 dB** | **44.99 dB** | **60.14 dB** | **55.11 dB** |
| **$N_{eff}$** | **6.92 Bits** | **5.49 Bits** | **8.66 Bits** | **7.18 Bits** | **9.69 Bits** | **8.86 Bits** |
| **Bandwidth** | **6.29 MHz** | **6.29 MHz** | **3.15 MHz** | **3.14MHz** | **1.57MHz** | **1.57MHz** |
| **$P_{avg}$** | **78.52 mW** | | | | | |

*Table 2: 2nd Order 4-Path KD1S Project Performance at 1MHz*

# Analysis & Design of Main Components

## I. Differential Ring Oscillator (Clock Generator)

One of the fundamental components in the design of KD1S modulators is the generation of precise clock signals. In this design, the objective was to employ a ring oscillator capable of generating eight equally spaced clock edges, ensuring proper timing for the K-paths in the KD1S modulator. Unlike single-ended ring oscillators, which inherently produce an odd number of clock phases in their topology, the ring oscillator below can generate an even number of clock edges, which aligns with the requirement needed for the 8-path 1st order and 4-path 2nd order topologies to operate successfully.

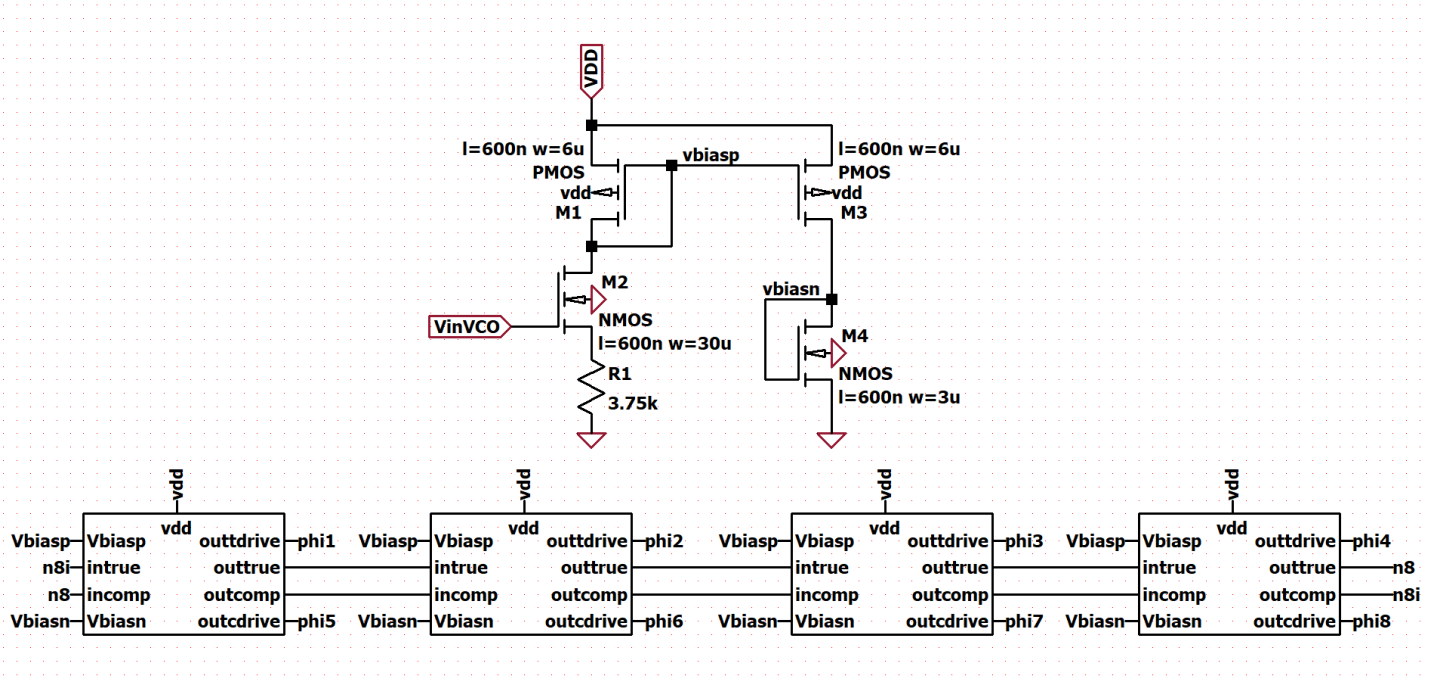



***Figure 1: Self-Biased Differential Ring Oscillator (Clock Generator) Topology***

Figure 1 illustrates the schematic of the ring oscillator topology, also denoted as the clock generator, used for generating K = 8 clock signals. The design of the clock generator is based on a chain of delay blocks, each responsible for introducing a precise phase shift between successive clock signals. The final delay stage is fed back into the first stage to create the intended oscillation. The internal architecture of the delay block, as seen in Figure 2, consists of an initial NAND gate stage followed by a cascade of current-starved and CMOS inverters. The current-starved inverters are significant in the design of the delay block, as they allow precise control of the delay introduced in each block. The control comes from the biasing voltages $V_{biasp}$ and $V_{biasn}$, as seen in Figure 1, which is affected by the input control voltage of the oscillator topology, VinVCO. As the biasing voltages increase, the current of the inverter increases with it, causing the oscillation frequency to increase due to the reduction of charge times. Since the oscillation frequency of the clock generator is a function of VinVCO (in other words, the oscillator is voltage-controlled), the design provides a wide range of oscillation frequencies that can be adjusted based on preference. This tunability allows the clock generator to adapt to varying operating conditions rather than being limited to a fixed frequency range. In this design, the resistor was fine-tuned so that the oscillation frequency of the clock generator is at 100MHz, and the period of the clock signals are 10ns with a DC voltage input of 5V.

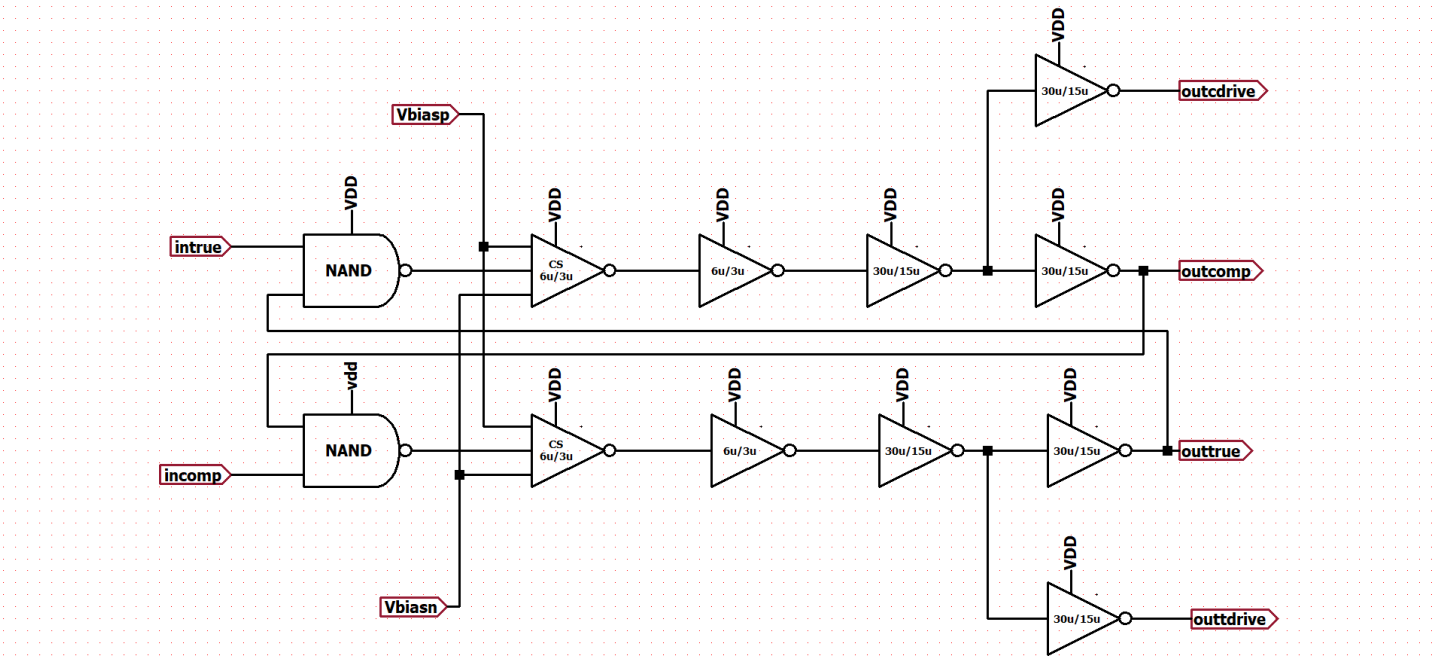



*Figure 2: Delay Block used in Differential Ring Oscillator (Clock Generator) Topology*

The symbol-view of the clock generator topology is illustrated in Figure 3. In this configuration, a slow ramp input voltage is applied to the clock generator to analyze the range of oscillation frequencies achievable across the entire supply voltage range.

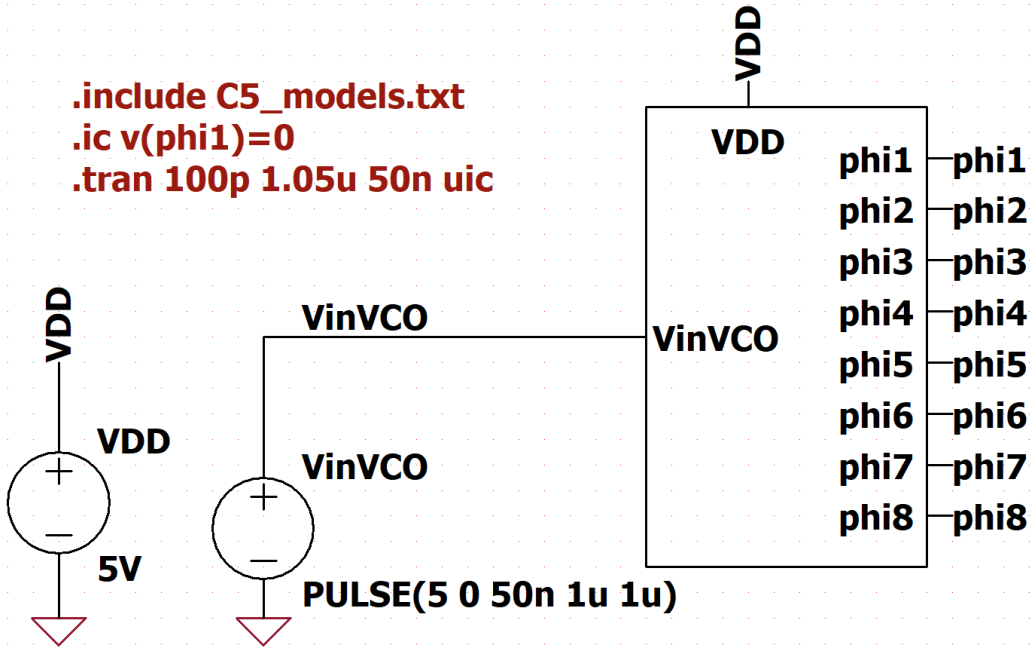



*Figure 3: Top-Level Symbol of Clock Generator with Simulation Test Schematic*

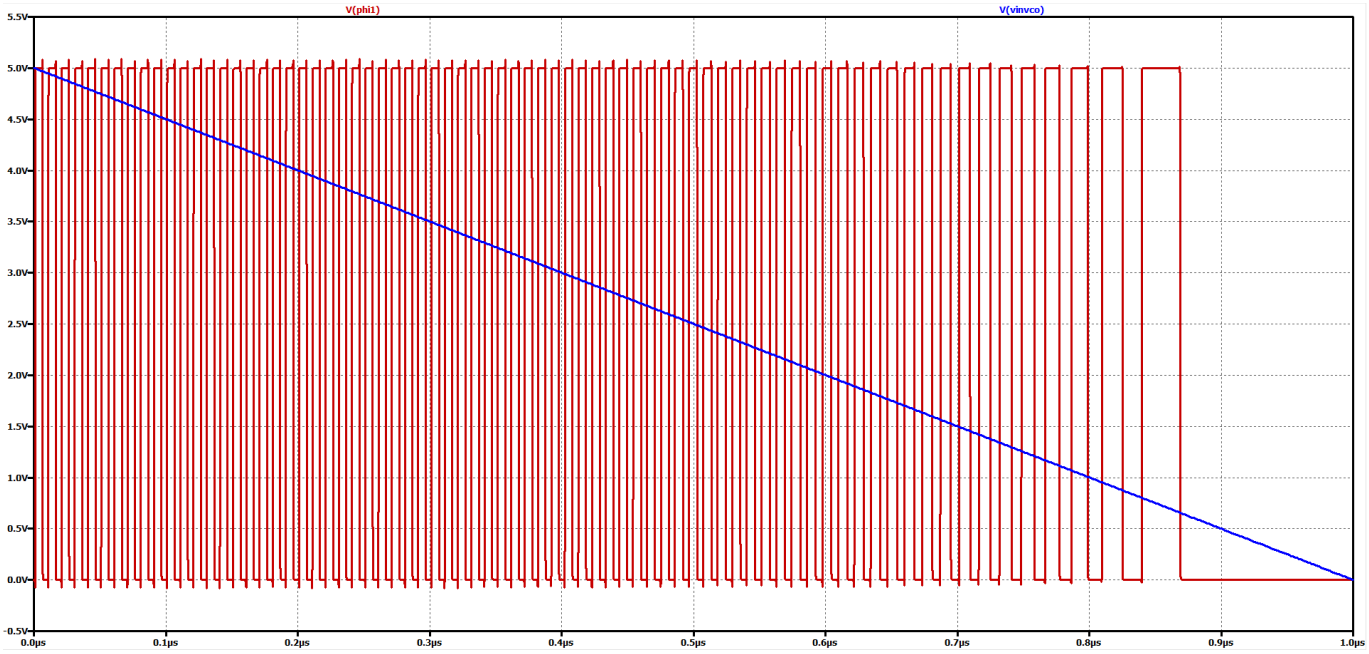



***Figure 4: Simulation Results of Sweeping DC Voltage & Range of Oscillation Frequencies***

Figure 4 shows the behavior of the clock generator when the input voltage is swept from 5V down to 0V. The waveforms show that the oscillation frequency is highest when the input voltage is at its peak. As the input voltage decrease, the oscillation frequency gradually reduces due to the reduced current-driving capability of the transistors inside the delay stages. Eventually, when the input voltage falls below the threshold voltage of the transistors, the devices cease to function as they will shut off, so it is important to take this into the design consideration. Practically, the circuit should be operating at a sufficient voltage above the threshold voltage for proper functionality.

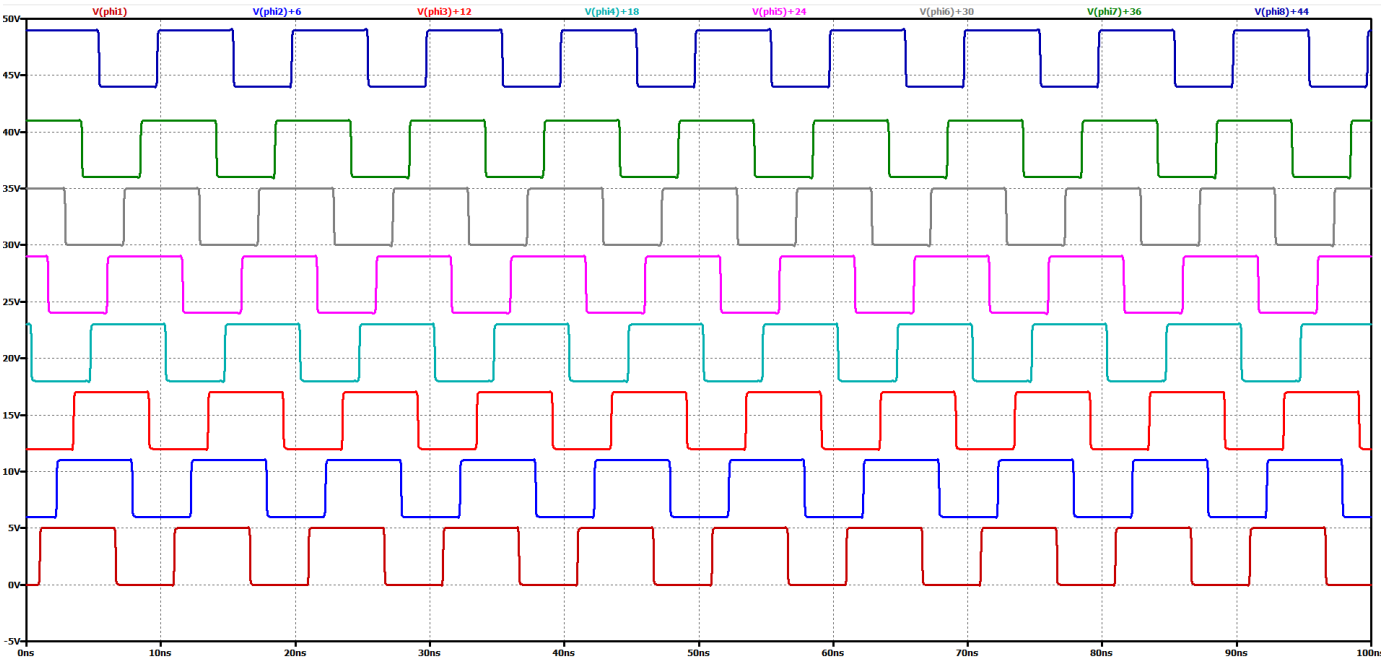



***Figure 5: Simulation Results of Generated Clock Signals for 1st Order Topology, K=8***

Therefore, our design sets the input control voltage VinVCO to 5V, as the clock generator topology has been carefully fine-tuned to achieve a 10ns sampling period for all clock phases, corresponding to an oscillation frequency of 100MHz, which is depicted in Figure 5 along with the waveforms of the eight clock signals. These selections ensure that the circuit remains within a stable operating region of the transistors while minimizing variations due to PVT conditions.

Accurate timing is critical for optimizing the performance of the KD1S modulator, particularly in ensuring proper operation of the feedback paths with the current clock signal configuration. Figure 6 shows the circuitry of the first two feedback paths within the 8-path KD1S 1st order topology, with the remaining circuitry omitted for visual clarity. In the first feedback path, $phi_1$ clocks the comparator, while $phi_2$ & $phi_7$ serve as the inputs to the transmission gates. Similarly, in the second feedback path, $phi_2$ clocks the comparator, while $phi_3$ & $phi_8$ feed into the two transmission gate inputs.

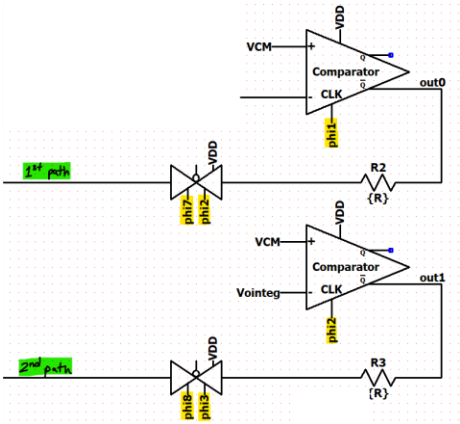



***Figure 6: Configuration of First Two Feedback Paths within the 1st order Topology, K=8***

Figure 7 provides an accurate representation of the clock signals associated with the two feedback paths. The lower half corresponds to the clock signals for the first feedback path, while the upper half corresponds to the second feedback path. The region highlighted in green represents the period during which the comparator feeds values through the transmission gates and back into the negative input of the integrator. Ideally, the clock signal during this time window for the subsequent feedback path should only activate after the first feedback path completes its operation (when $phi_7$ goes low). In the current setup below, $phi_7$ (highlighted in green) is active during the first feedback path. However, during this time window, $phi_3$ (highlighted in red), becomes active during this timing window. Having both feedback paths on ruins the overall performance of the circuit. The root issue is due to the clock cycles having a duty cycle greater than 50%. Therefore, in terms of design consideration, the only way to ensure a duty cycle of 50% for the clock signals to remove this problem would be to generate the complementary counterparts using inverters. This approach eliminates the present timing conflicts without adding components or increasing the complexity of the existing KD1S layout and would be implemented in future designs.

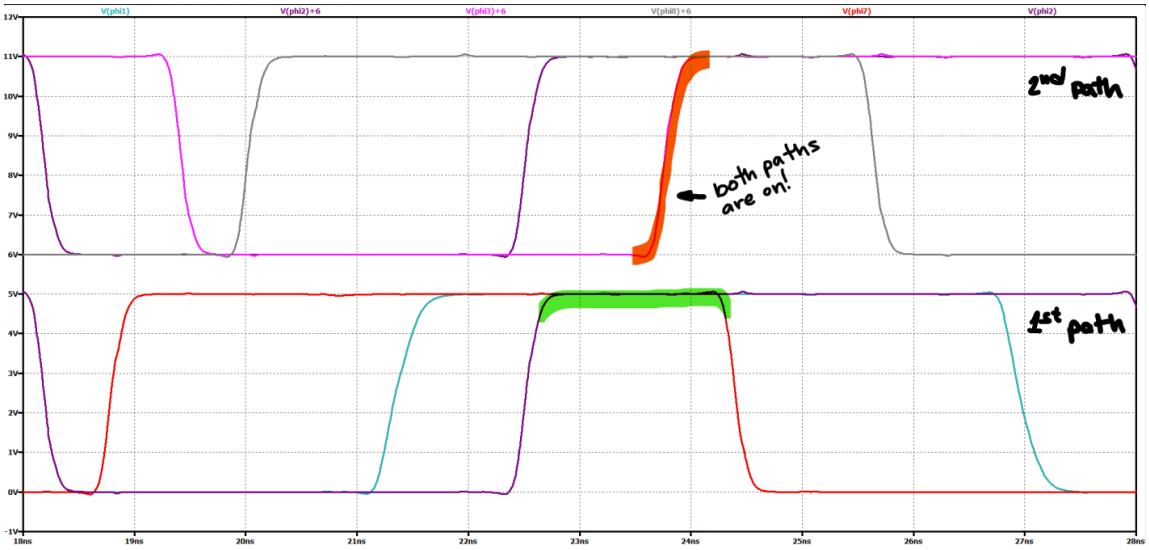



***Figure 7: Observing Timing Window Flaw in Active Feedback Paths***

# II. Amplifier

Another critical component of the KD1S modulator is the amplifier, which functions as the equivalent of the integrator in the typical KD1S topology. The amplifier's role here is to perform the essential task of averaging the signal during each clock cycle. The current design is based off a simple differential amplifier topology, as depicted in Figure 8, to achieve this functionality.

To evaluate the performance of the amplifier, the positive input of the amplifier is swept from 0 to VDD, while the negative input of the amplifier is kept at the common mode voltage VCM, which is half of the supply voltage.

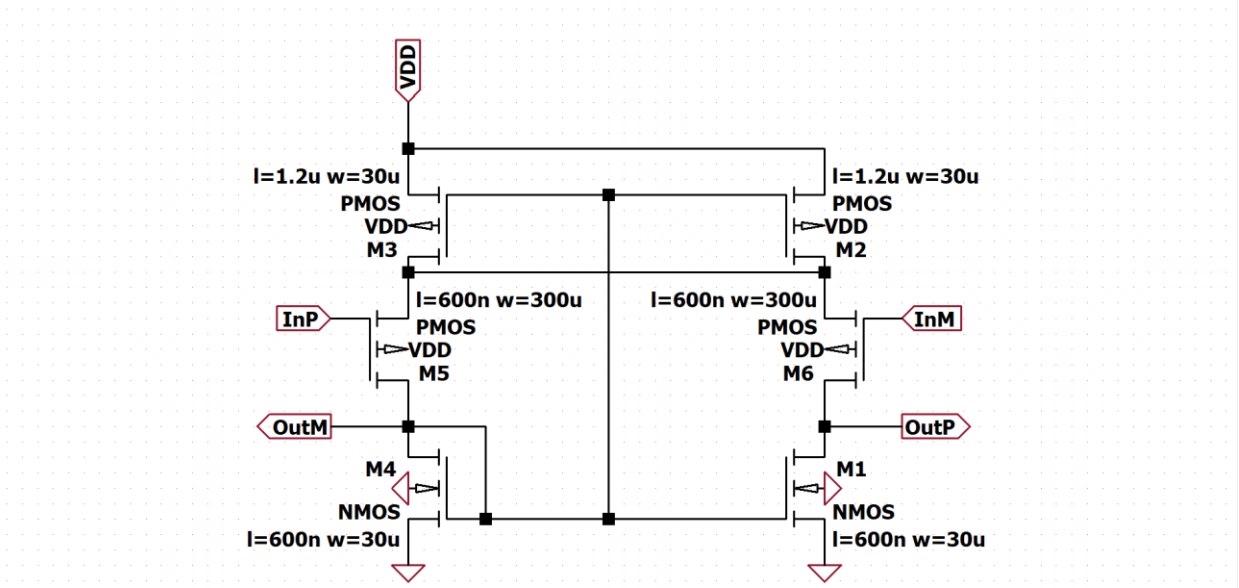



*Figure 8: Self-Biasing Differential Amplifier Topology used in Integrator*

To quantify the gain of the amplifier, the derivative of the output voltage is plotted in Figure 9, and the peak value of this derivative was observed. From the waveform, the gain was measured to be twenty-six. To improve the gain slightly without introducing complexity of the topology, the lengths of transistors M3 and M2 in the differential pair were doubled from the standard C5 minimum length. While higher-gain designs could reduce the overall gain error, the returns are diminishing as the overall design increases in complexity and power consumption increases. Therefore, this amplifier has sufficient gain to maintain optimal operation while also being simple in its design.

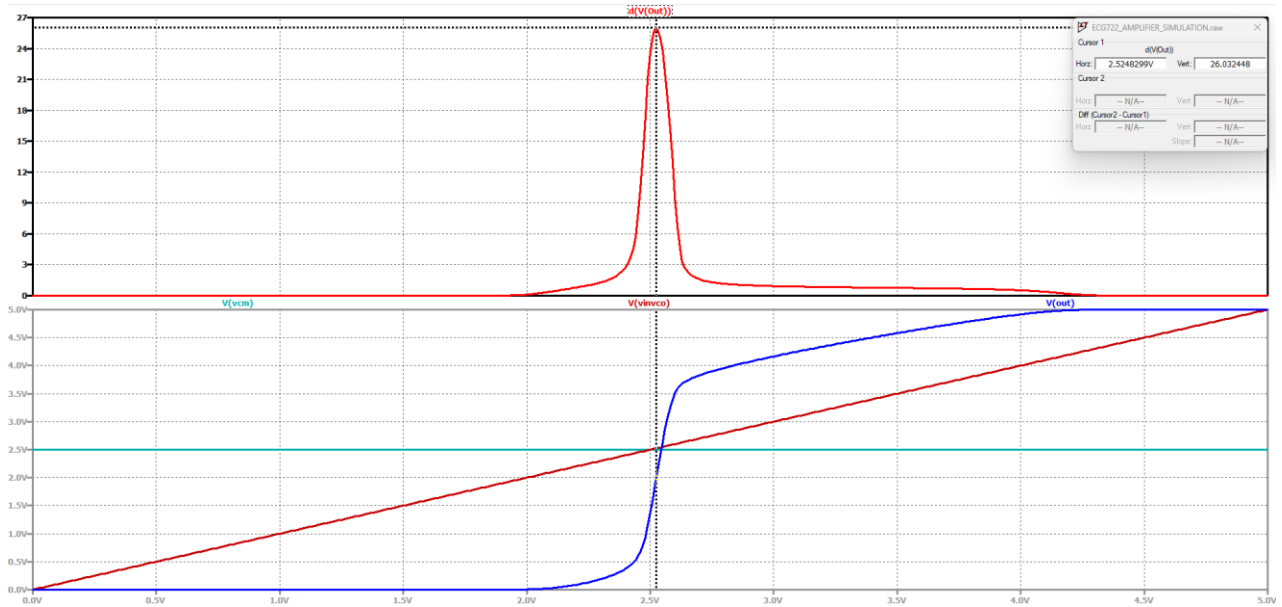



*Figure 9: Measuring Inputs, Outputs, & Gain Values of Differential Amplifier*

# III. Comparator

The comparator is another vital component within the KD1S modulator, as it must be able to make quick and accurate decisions when the clock signals transition from high to low. The symbol-view of the clocked comparator topology is illustrated in Figure 10.

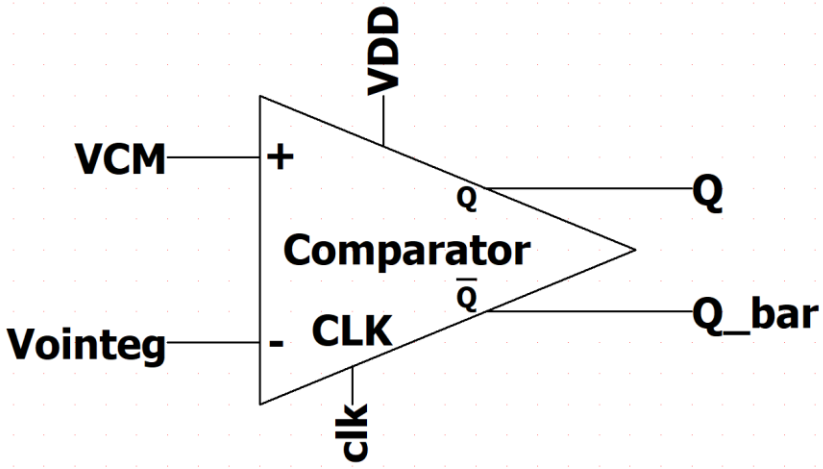



*Figure 10: Top-Level Symbol of Comparator*

Inside the top-level symbol is the comparator topology denoted for the KD1S modulator, as seen in Figure 11. Due to the number of K-paths in the KD1S modulator, there should be K-comparators, designating one for each feedback path. This configuration gives us the ability to make decisions eight times faster than the sampling frequency. Any fluctuations and errors that flow through the feedback paths get averaged out over the path, but it is more important to reduce the amount of noise and inaccuracy without relying on the inherent nature of the comparator. This specific comparator focuses on low power and high speed, while also minimizing kickback noise with the isolation of the outputs from the clock. In Figure 11, the shows the topology of the compactor, along the addition of a cross-coupled inverter NAND SR latch, and buffed input/output drivers to fully drive the input signals as well as the output of the comparator.

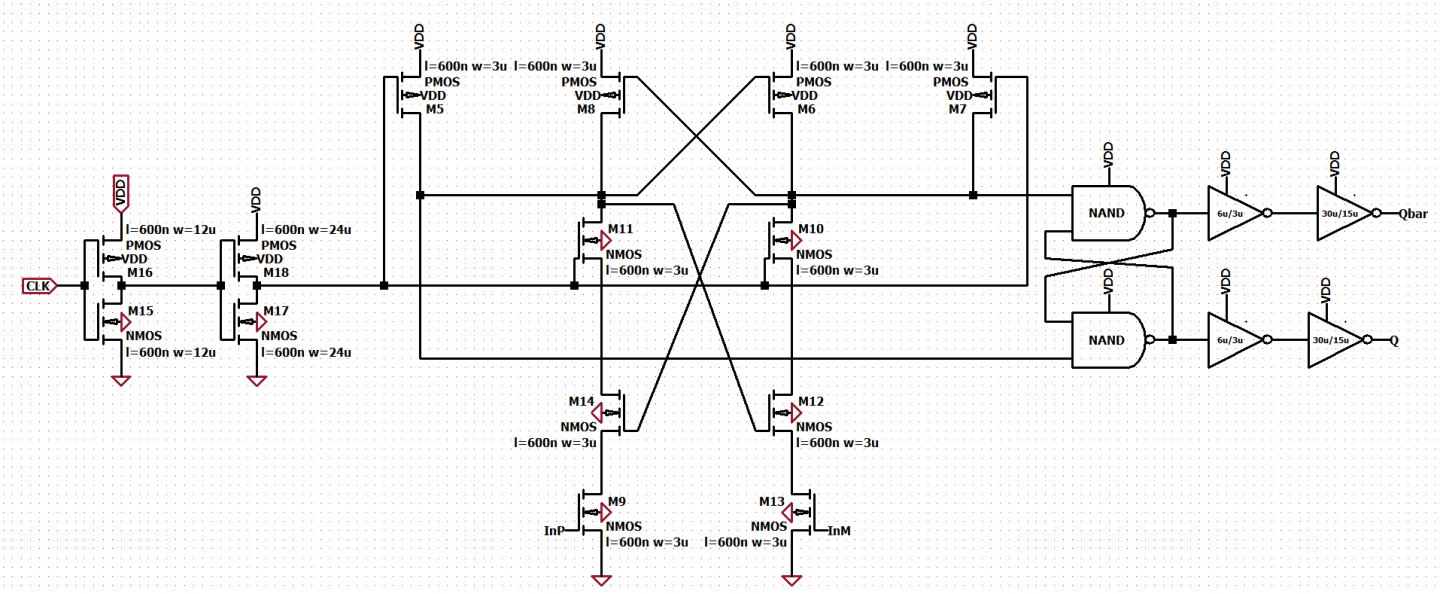



*Figure 11: Clocked Comparator Topology with Buffed Input & Output Drivers and Cross-Coupled NAND SR Latch*

A critical aspect of the comparator design is the switching point, as minimizing delay is essential for efficient and accurate decision-making. The schematic of the comparator is shown in Figure 12, setting up the rising and falling edges of the output.

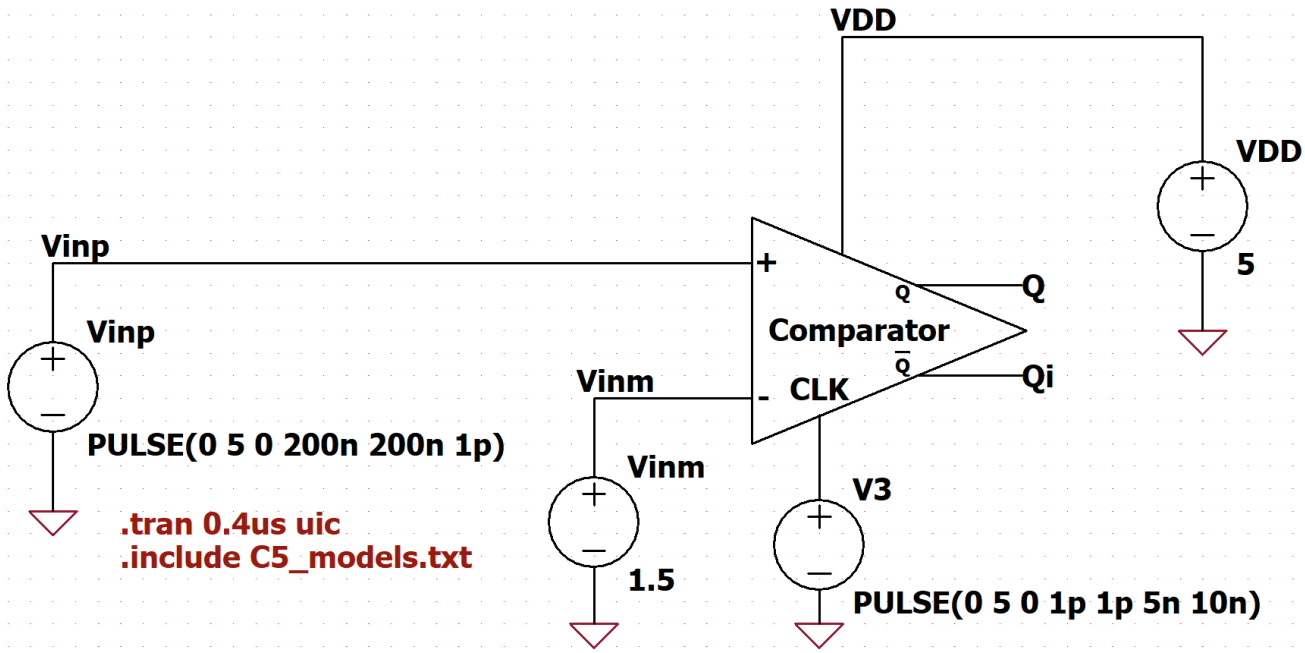



*Figure 12: Top-Level Symbol of Clocked Comparator Topology with Simulation Test Schematic*

In this configuration, the pulse source is applied to the positive input, generating a triangular waveform that ramps up to the supply voltage and back. On the other hand, the negative input is held at a constant DC voltage of 1.5V. Once the positive input passes the threshold voltage of 1.5V, the comparator output transitions to the supply voltage, and it returns to ground once the positive input drops below the threshold voltage. The results of the comparator output can be seen in Figure 13, where a delay of 11.3ns is seen in the rising edge and 1.34ns on the falling edge. While the falling edge demonstrates a much faster response compared to the rising edge, both offsets are sufficient for the requirements of the KD1S modulator to operate efficiently.

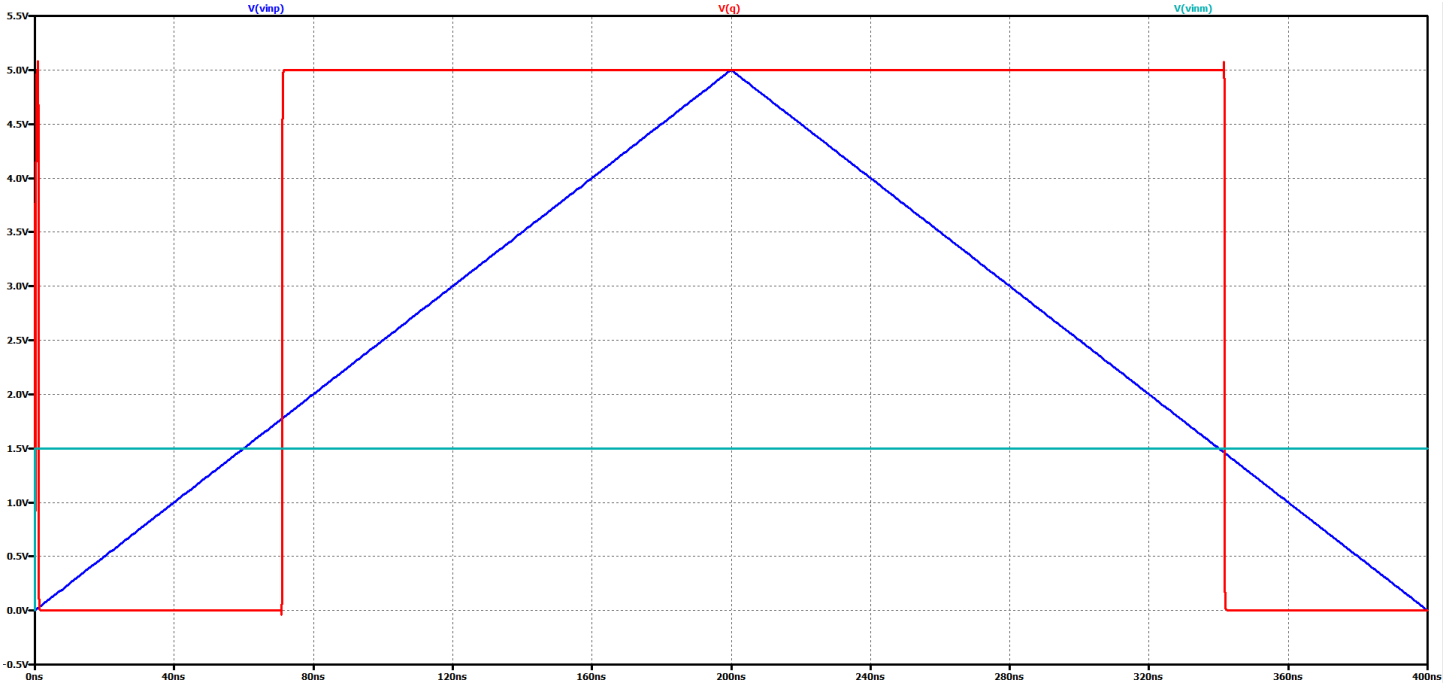



*Figure 13: Measuring the Rising Edge & Falling Edge of the Comparator*

# IV. Transmission Gates

The last critical design component of the KD1S modulator involves feedback signal control and logic. The transmission gate is one of the key elements implemented in the feedback paths of the circuitry, with each transmission gate symbol placed in each path. For simplicity, two transmission gates are combined into a single block, as represented by the top-level symbol in Figure 14.1.

Inside the transmission gate schematic as seen in Figure 14.2, the clock signals are fed into the gate of the NMOS transistor, while the inverter generates the complementary clock signal to drive the PMOS transistor. This configuration ensures that when the NMOS gate is high, the PMOS gate is simultaneously low, which allows both transistors to turn on and pass the input signal through. In contrast, if the NMOS gate is low, the PMOS gate is high, this makes both transistors turn off, effectively blocking the signal from going through. For each feedback path, different clock phases are assigned to the transmission gates depending on the feedback path to ensure the proper operation of the KD1S modulator. This allows precise control over how the signal flows inside the feedback paths. Inverters are used so that input for the PMOS directly uses the complementary clock signal that is being fed into the input.

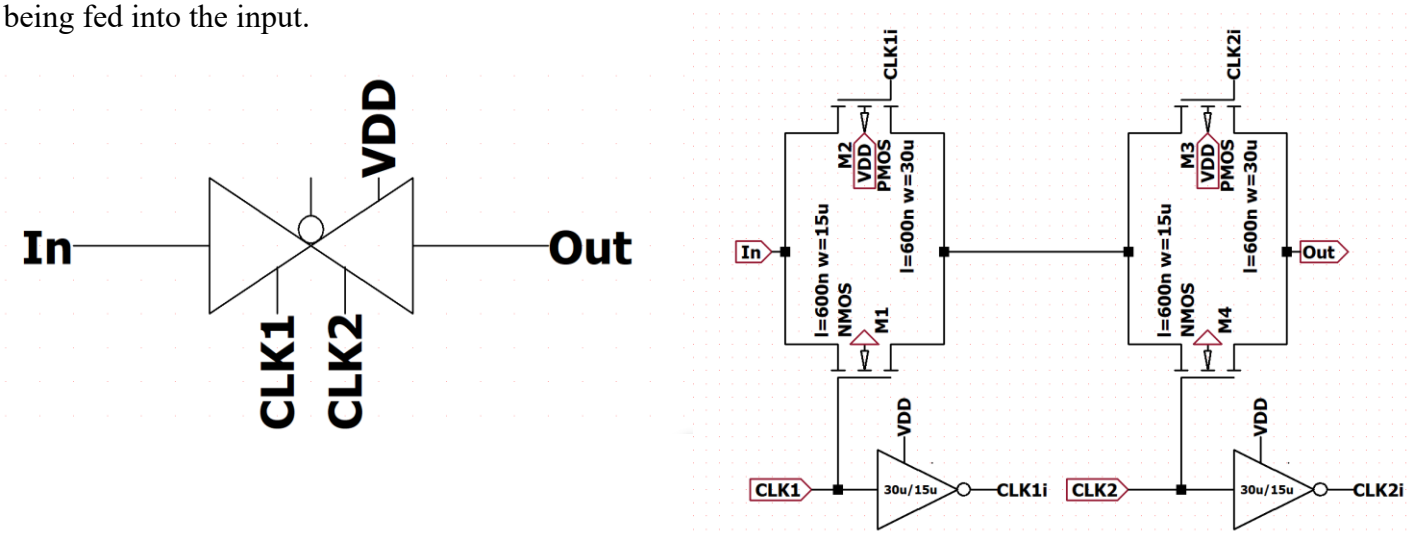



*Figure 14: Transmission Gate Top-Level Symbol (14.1) & Schematic (14.2)*

# V. Hand Calculations: Ideal SNR Values

Recalling the $SNR_{ideal}$ formula for a 1st order NS topology:

$$SNR_{ideal} = 6.02N + 1.76 - 5.17 + 30\log(K)$$

Using the following parameters used in the first-order topology:

$$\boldsymbol{K = 64}, \qquad \boldsymbol{N = 1}$$

Our ideal SNR value at K = 64 is:

$$SNR_{ideal} = 6.02 + 1.76 - 5.17 + 30\log(64)$$

$$SNR_{ideal} = 6.02 + 1.76 - 5.17 + 54.18$$

$$SNR_{ideal} = 56.79\ dB$$

Our ideal SNR value at K = 128 is:

$$SNR_{ideal} = 6.02 + 1.76 - 5.17 + 63.21$$

$$SNR_{ideal} = 65.83\ dB$$

Our ideal SNR value at K = 256 is:

$$SNR_{ideal} = 6.02 + 1.76 - 19.15 + 72.24$$

$$SNR_{ideal} = 74.86\ dB$$

Now, let us calculate the formula for a 2nd order NS topology:

$$SNR_{ideal} = 6.02N + 1.76 - 12.9 + 50\log(K)$$

Using the following parameters used in the second-order topology:

$$\boldsymbol{K = 32}, \qquad \boldsymbol{N = 1}$$

$$SNR_{ideal} = 6.02 + 1.76 - 12.9 + 75.25$$

Our ideal SNR value at K = 32 is:

$$SNR_{ideal} = 70.14\ dB$$

Our ideal SNR value at K = 64 is:

$$SNR_{ideal} = 6.02 + 1.76 - 12.9 + 90.31$$

$$SNR_{ideal} = 85.19\ dB$$

Our ideal SNR value at K = 128 is:

$$SNR_{ideal} = 6.02 + 1.76 - 21.82 + 105.36$$

$$SNR_{ideal} = 100.2\ dB$$

# V. Hand Calculations: Effective Number of Bits

Recalling the $N_{eff}$ formula for a 1st order NS topology:

$$N_{eff} = \frac{SNR_{ideal} - 1.76}{6.02}$$

Therefore, for an OSR of 64, and using the calculated SNR values we found above:

$$N_{eff} = \frac{56.79 - 1.76}{6.02} = 9.14\ Bits$$

Our ideal effective number of bits at K = 128 is:

$$N_{eff} = \frac{65.83 - 1.76}{6.02} = 10.64\ Bits$$

Our ideal effective number of bits at K = 256 is:

$$N_{eff} = \frac{74.86 - 1.76}{6.02} = 12.14\ Bits$$

Now, let us calculate the $N_{eff}$ formula for a 2nd order NS topology:

$$N_{eff} = \frac{SNR_{ideal} - 1.76}{6.02}$$

Notice that the formula for the 1st and 2nd order topologies are the same, the difference being the $SNR_{ideal}$ values. Now, for an OSR of 32 and using the calculated SNR values we found above:

$$N_{eff} = \frac{70.14 - 1.76}{6.02} = 11.36\ Bits$$

Our ideal effective number of bits at K = 64 is:

$$N_{eff} = \frac{85.19 - 1.76}{6.02} = 13.86\ Bits$$

Our ideal effective number of bits at K = 128 is:

$$N_{eff} = \frac{100.2 - 1.76}{6.02} = 16.35\ Bits$$

# Final Design Topologies & Simulation Results

## I. The Continuous Time KD1S 1st Order 8-Path Topology

With all the components above combined, Figure 15 shows the final proposed design of the 1st Order 8-Path Continuous Time (CT) KD1S to replace the ADC in Fig. 9.32 of the *CMOS Mixed-Signal Design* textbook. In this specific configuration, we are using an input amplitude of 2V and an input frequency of 1MHz.

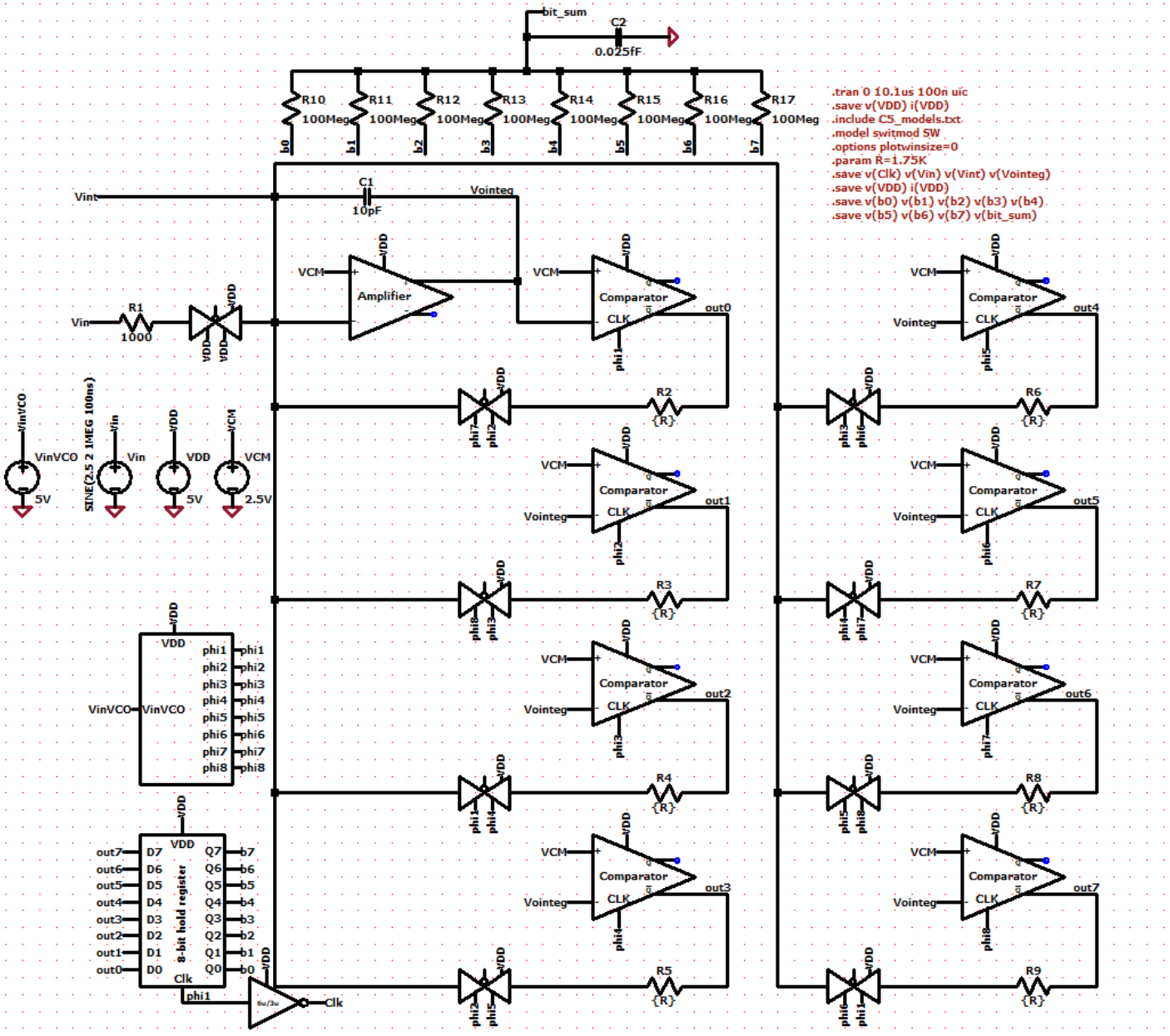



*Figure 15: 1st Order 8-Path CT KD1S Top-Level Schematic*

As seen in Figure 16, the output is the average of 8-bit outputs and is summed together inside the *bitsum* node, with the use of 100 MEG resistors for each of the bits. The *bitsum* waveform tracks the input signal well, but the waveform is not perfect as there are small areas where dead zones occur as well as transient spikes that can potentially be cleaned up in future design improvements.

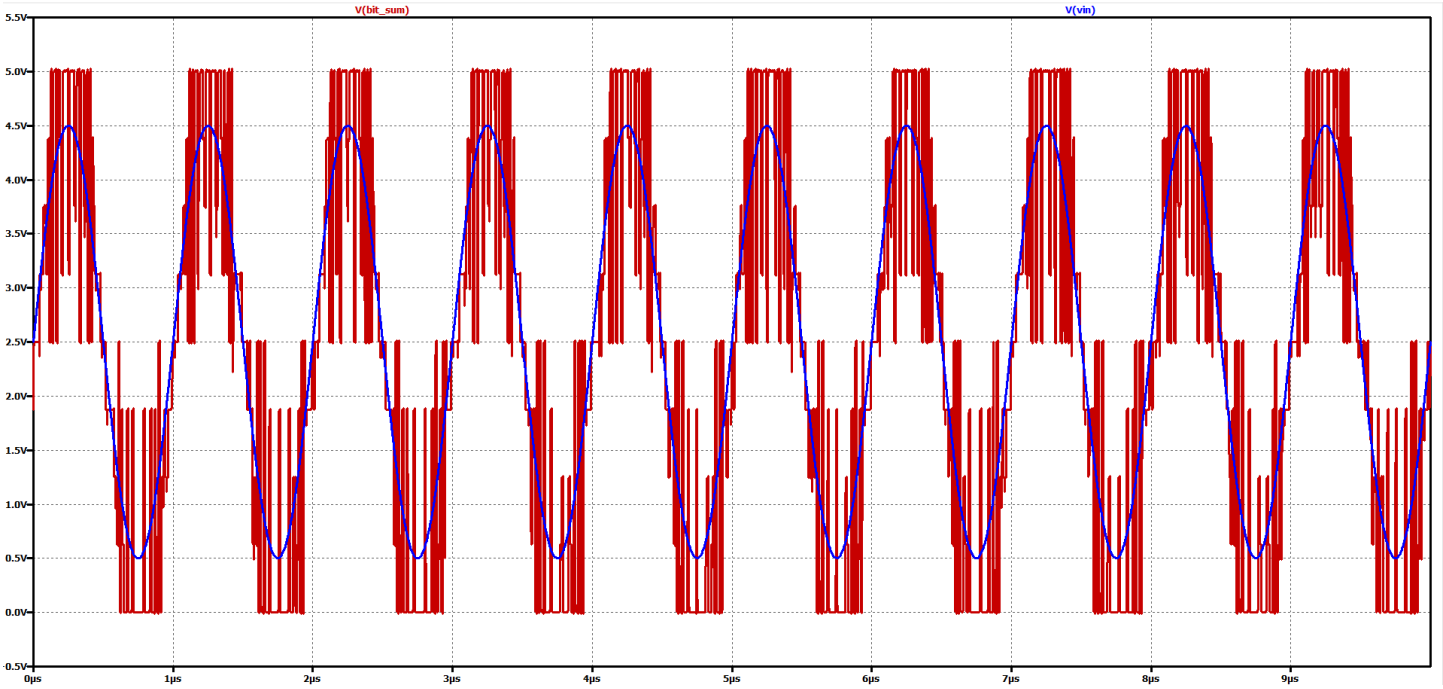



***Figure 16: Input and Output Waveforms of the 1st Order 8-Path CT KD1S Topology***

With the use of MATLAB, the data for both serial and parallel modes can be observed and compared against the hand calculations that we solved previously. Based on the results from the graphs, we can see that we did not reach our ideal SNR values as well as our $N_{eff}$ values due to the non-ideality of the circuit and other effects that externally decrease the total amount of SNR that we are able to obtain and cannot be applied to in the formula. The effective sampling rate here is around 807 MHz, which is eight times the original sampling frequency (~100-101MHz).The data from LTspice is based on 10 full cycles, which is sufficient for the results to be accurate when extracting them to MATLAB. For the first-order topology, OSR values of 64, 128, and 256 were calculated below in Figures 17-19.

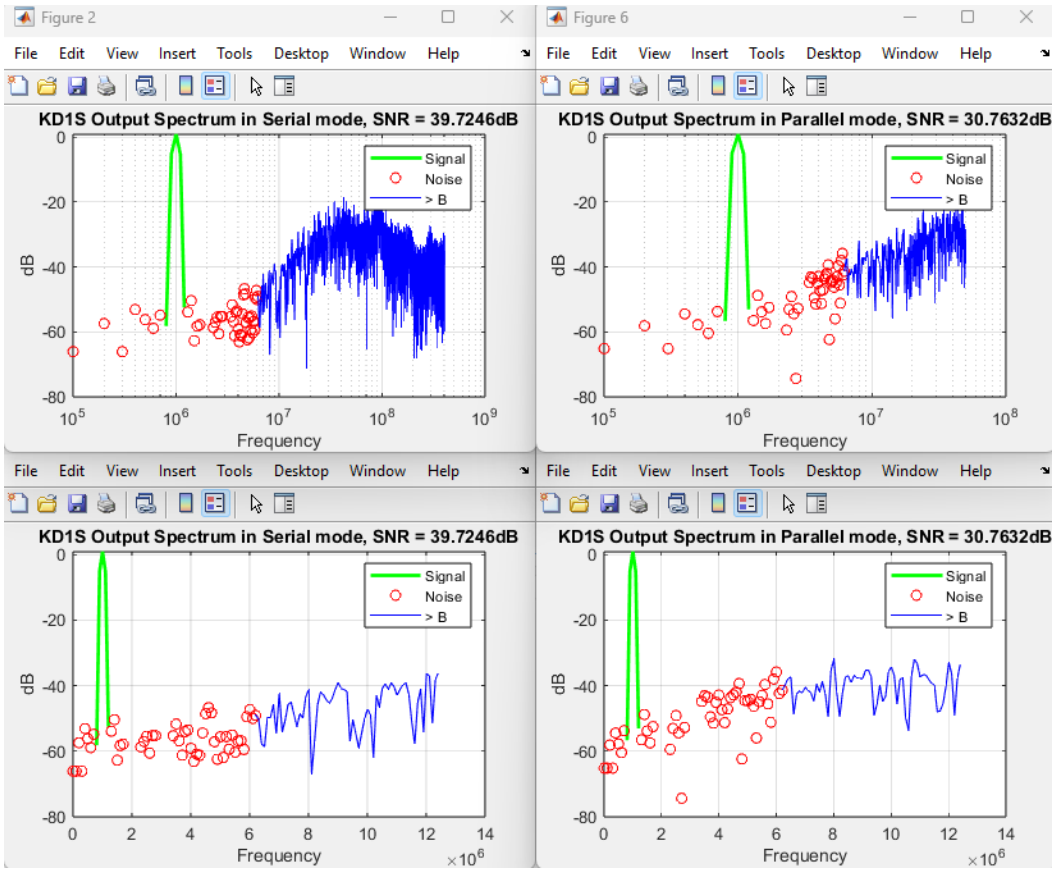



*Figure 17: SNR in Serial/Parallel Mode for 1st Order 8-Path KD1S, OSR = 64*

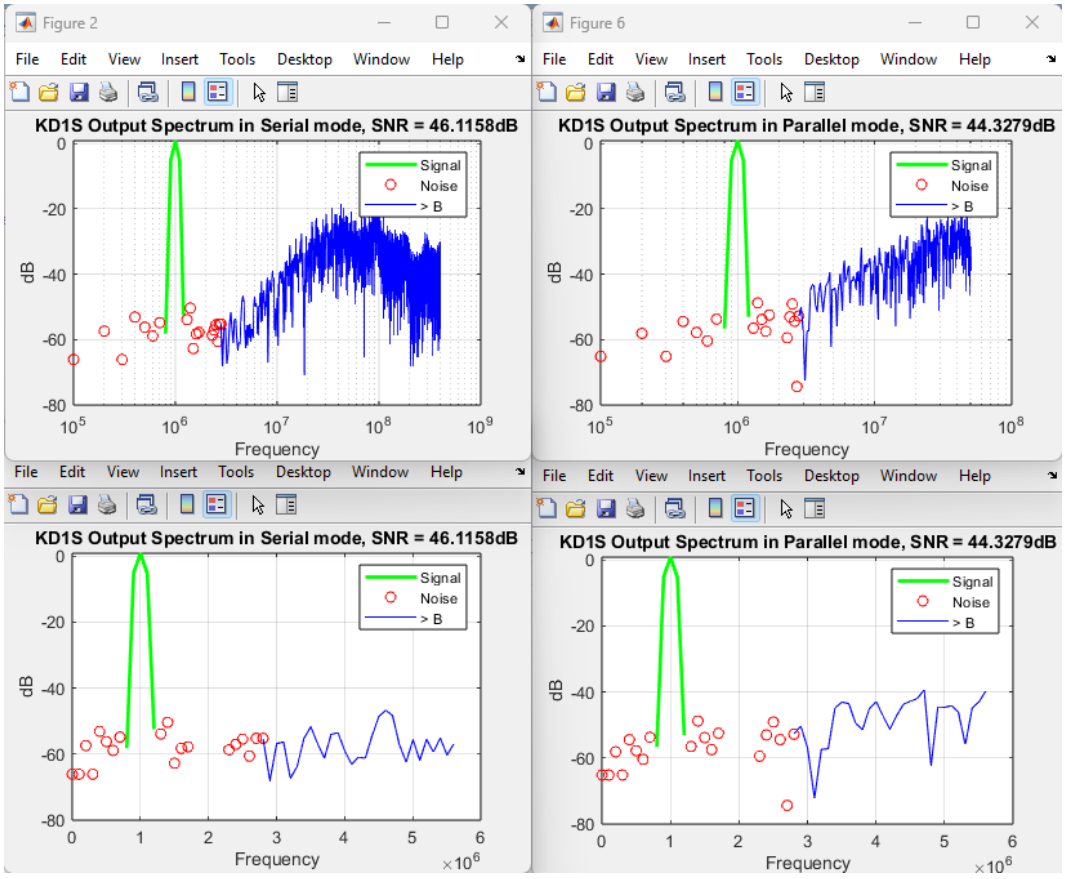



*Figure 18: SNR in Serial/Parallel Mode for 1st Order 8-Path KD1S, OSR = 128*

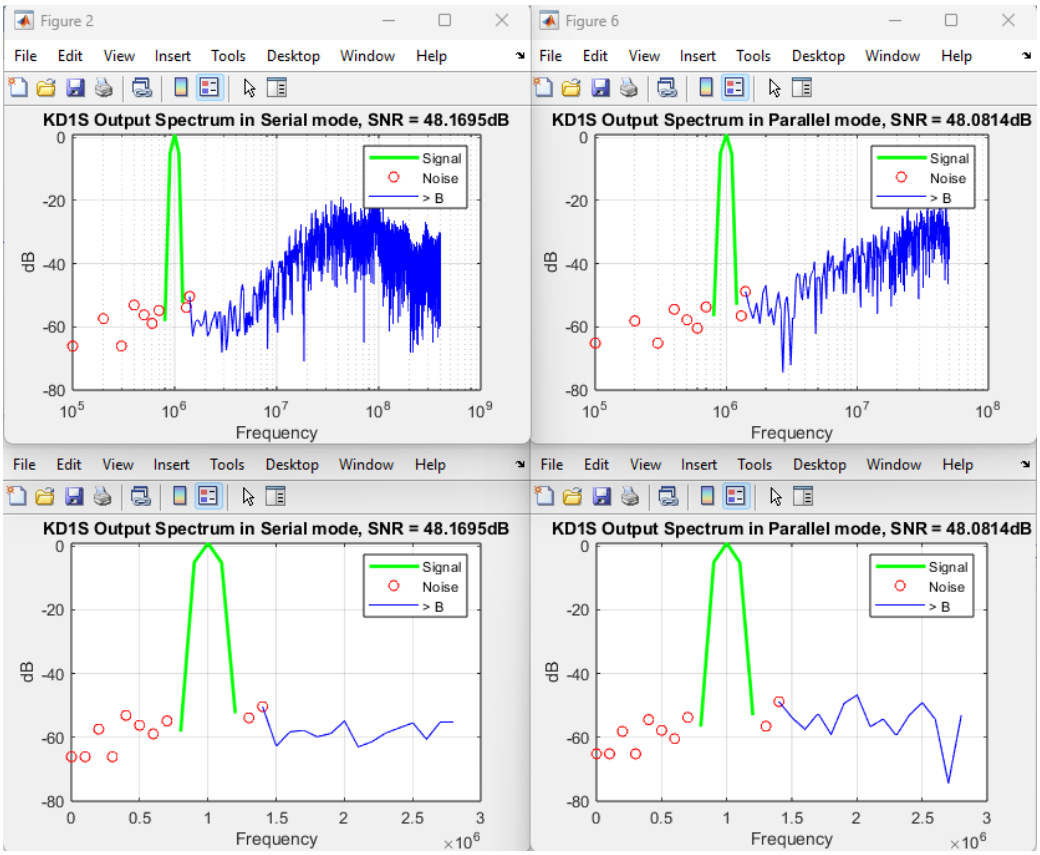



***Figure 19: SNR in Serial/Parallel Mode for 1st Order 8-Path KD1S, OSR = 256***

The results below show the SNR, $N_{eff}$, and Bandwidth values at OSR values of 64, 128, and 256 in both serial and parallel modes, verifying the waveforms above:

```
Kpath = 8 OSR = 64
For 1-bit output (serial mode) at Kpath*fs = 807 MHz
SNR = 39.72, Neff = 6.30, B = 6.30 MHz
For Kpath-bits output (parallel mode) at fs = 101 MHz
SNR = 30.76, Neff = 4.81, B = 6.30 MHz>> Fig9_33_Matlab

Kpath = 8 OSR = 128
For 1-bit output (serial mode) at Kpath*fs = 807 MHz
SNR = 46.12, Neff = 7.36, B = 3.15 MHz
For Kpath-bits output (parallel mode) at fs = 101 MHz
SNR = 44.33, Neff = 7.07, B = 3.15 MHz>> Fig9_33_Matlab

Kpath = 8 OSR = 256
For 1-bit output (serial mode) at Kpath*fs = 807 MHz
SNR = 48.17, Neff = 7.71, B = 1.58 MHz
For Kpath-bits output (parallel mode) at fs = 101 MHz
SNR = 48.08, Neff = 7.69, B = 1.57 MHz>> Fig9_33_Matlab
```

***Figure 20: SNR, $N_{eff}$, and Bandwidth Results in Serial/Parallel Mode for 1st Order 8-Path KD1S***

# II. The Continuous Time KD1S 2nd Order 4-Path Topology

With all the components above combined, Figure 21 shows the final proposed design of the 2nd Order 4-Path Continuous Time (CT) KD1S to replace the ADC in Fig. 9.32 of the *CMOS Mixed-Signal Design* textbook. In this specific configuration, we are also using an input amplitude of 2V and an input frequency of 1MHz. In the second-order topology, there is an additional amplifier, and the number of paths reduce from eight to four.

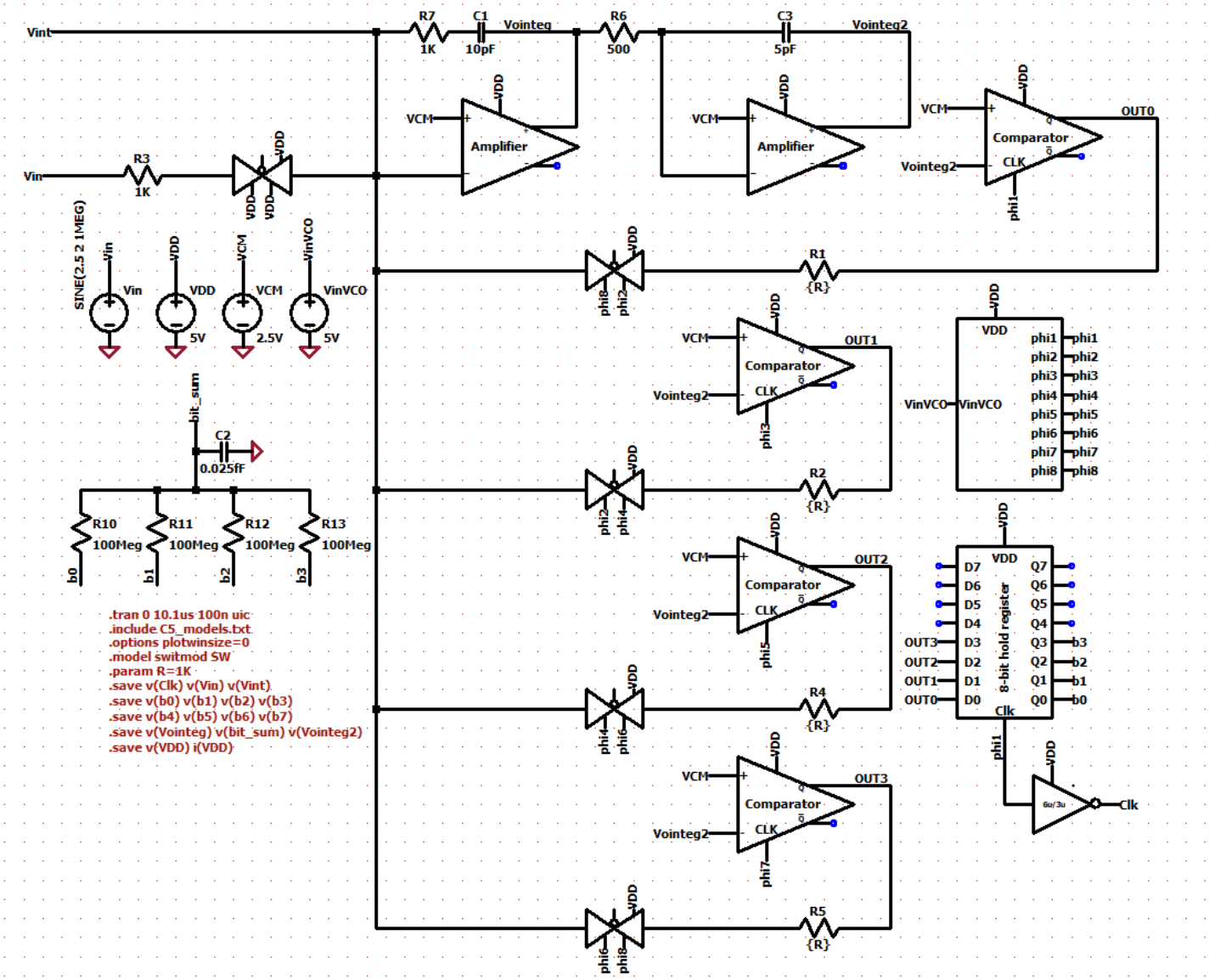



*Figure 21: 2nd Order 4-Path CT KD1S Top-Level Schematic*

As seen in Figure 22, the output is the average of 4-bit outputs and is summed together inside the *bitsum* node, with the use of 100 MEG resistors for each of the bits. The *bitsum* waveform tracks the input signal much better than 1st order topology, as the number of dead zones is minimized, but the spikes in the transient are more volatile near the troughs and peaks. The effective sampling rate here is around 807 MHz, which is eight times the original sampling frequency (~100-101MHz), which is the same as the first-order topology. Overall, this design is much more sufficient in terms of performance compared to the ADC in Figure 9.32 as well as our first-order topology when the data is extracted to MATLAB.

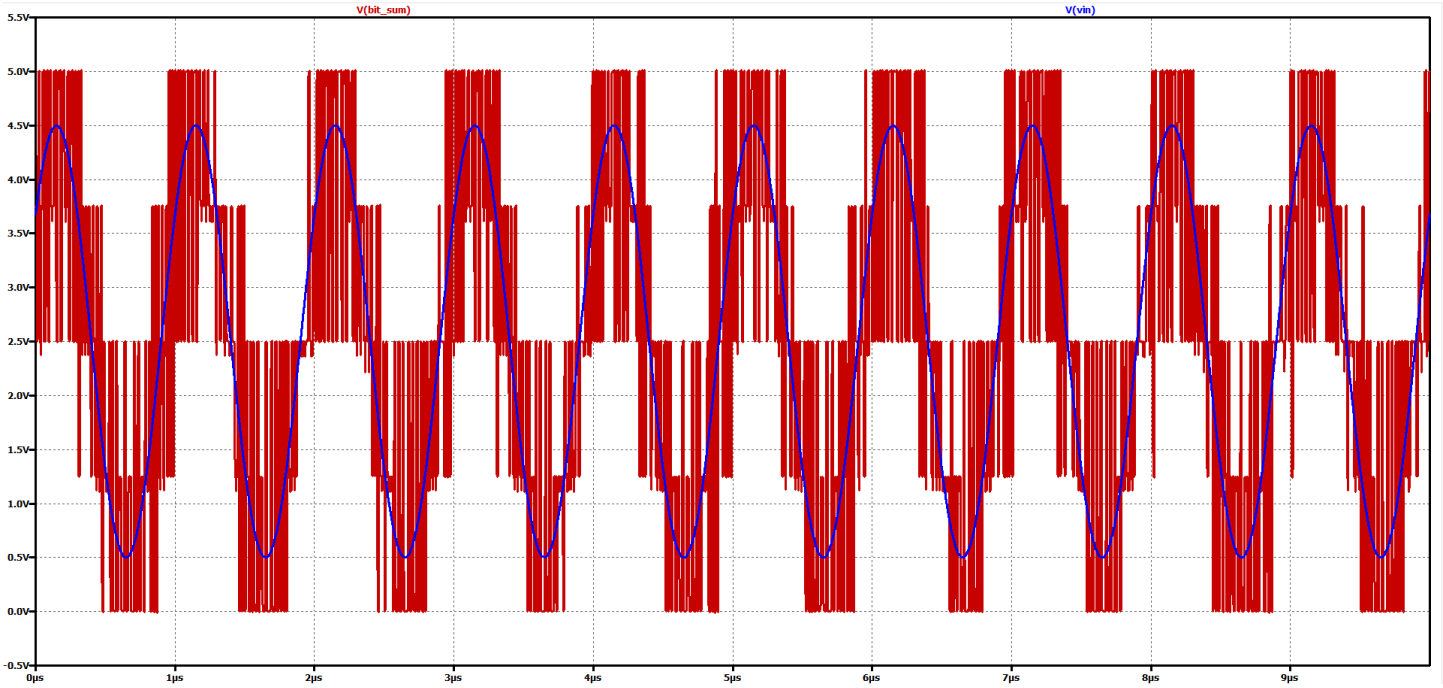



***Figure 22: Input and Output Waveforms of the 2nd Order 4-Path CT KD1S Topology***

With the use of MATLAB, the data for both serial and parallel modes can be observed and compared against the hand calculations that we solved previously. Based on the results from the graphs, we can see that we did not reach our ideal SNR values as well as our effective number of bits due to the non-ideality of the circuit and other effects that externally decrease the total amount of SNR that we are able to obtain and cannot be applied to in the formula. The data from LTspice is based on ten full cycles, which is sufficient for the results to be accurate when extracting them to MATLAB. Since this is the second-order topology, we applied OSR values of 32, 64, and 128 and the waveform results can be seen in the following Figures 23-25.

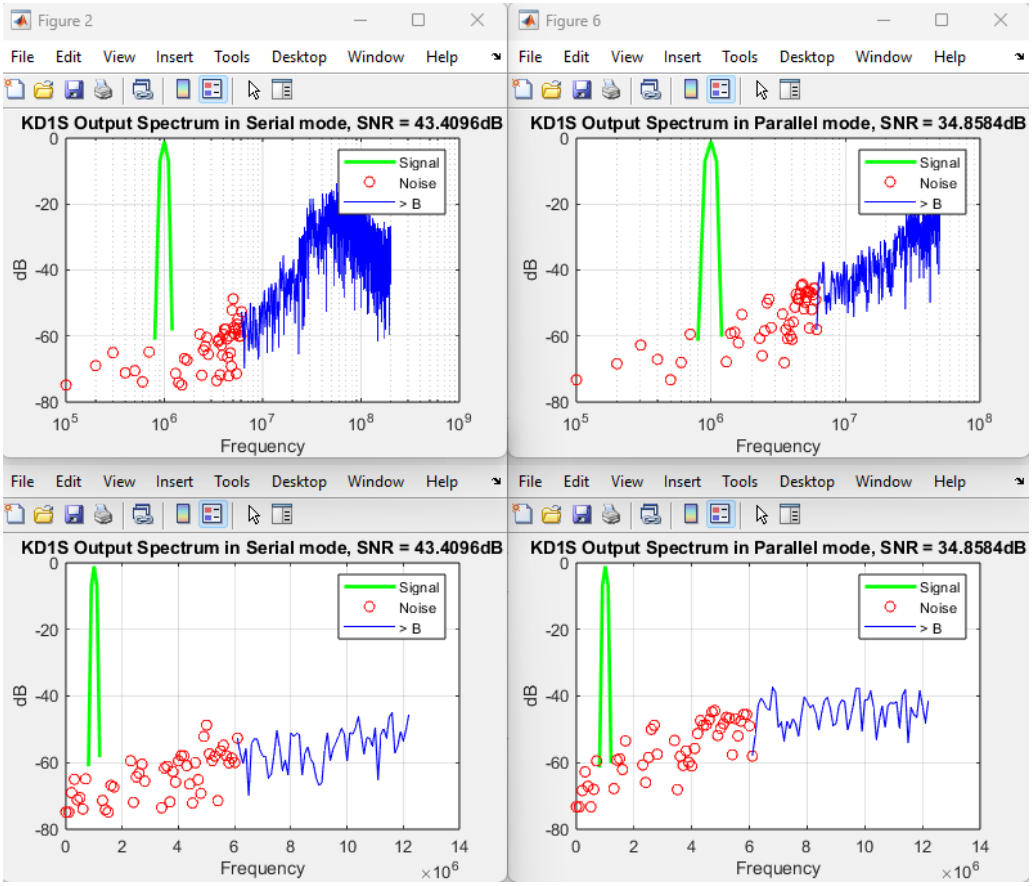



*Figure 23: SNR in Serial/Parallel Mode for 2nd Order 4-Path KD1S, OSR = 32*

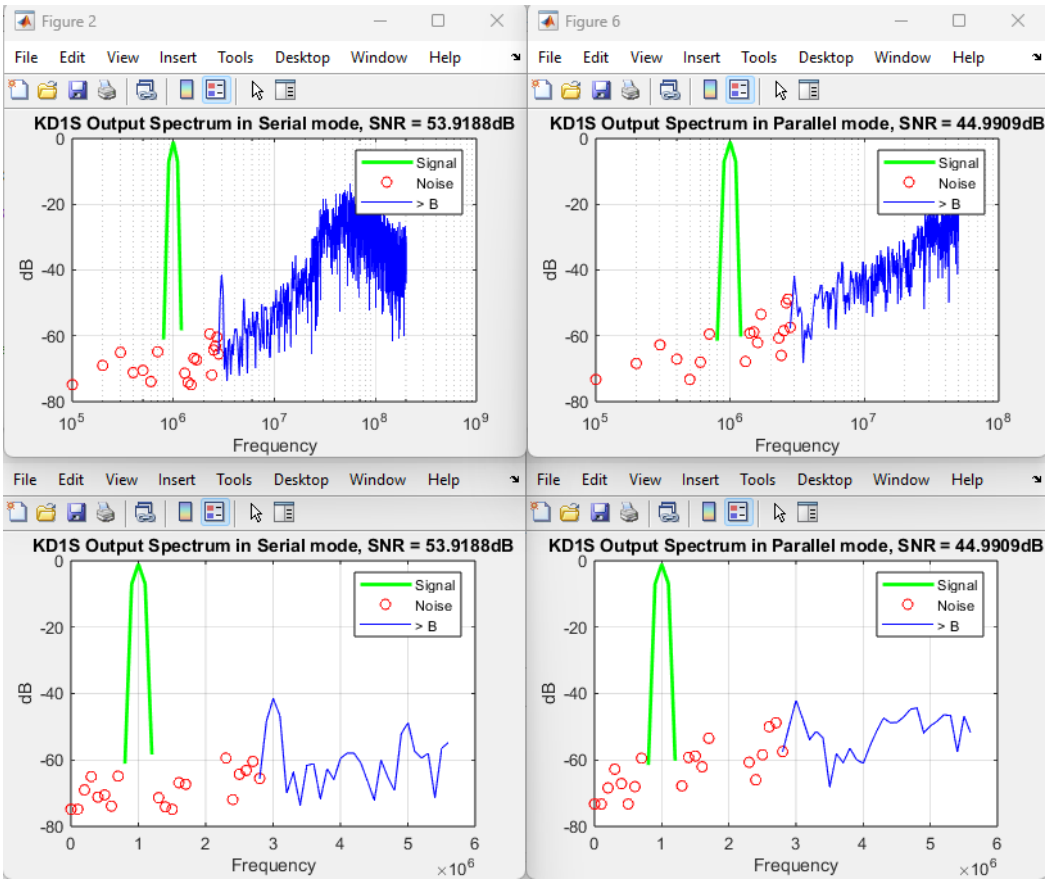



*Figure 24: SNR in Serial/Parallel Mode for 2nd Order 4-Path KD1S, OSR = 64*

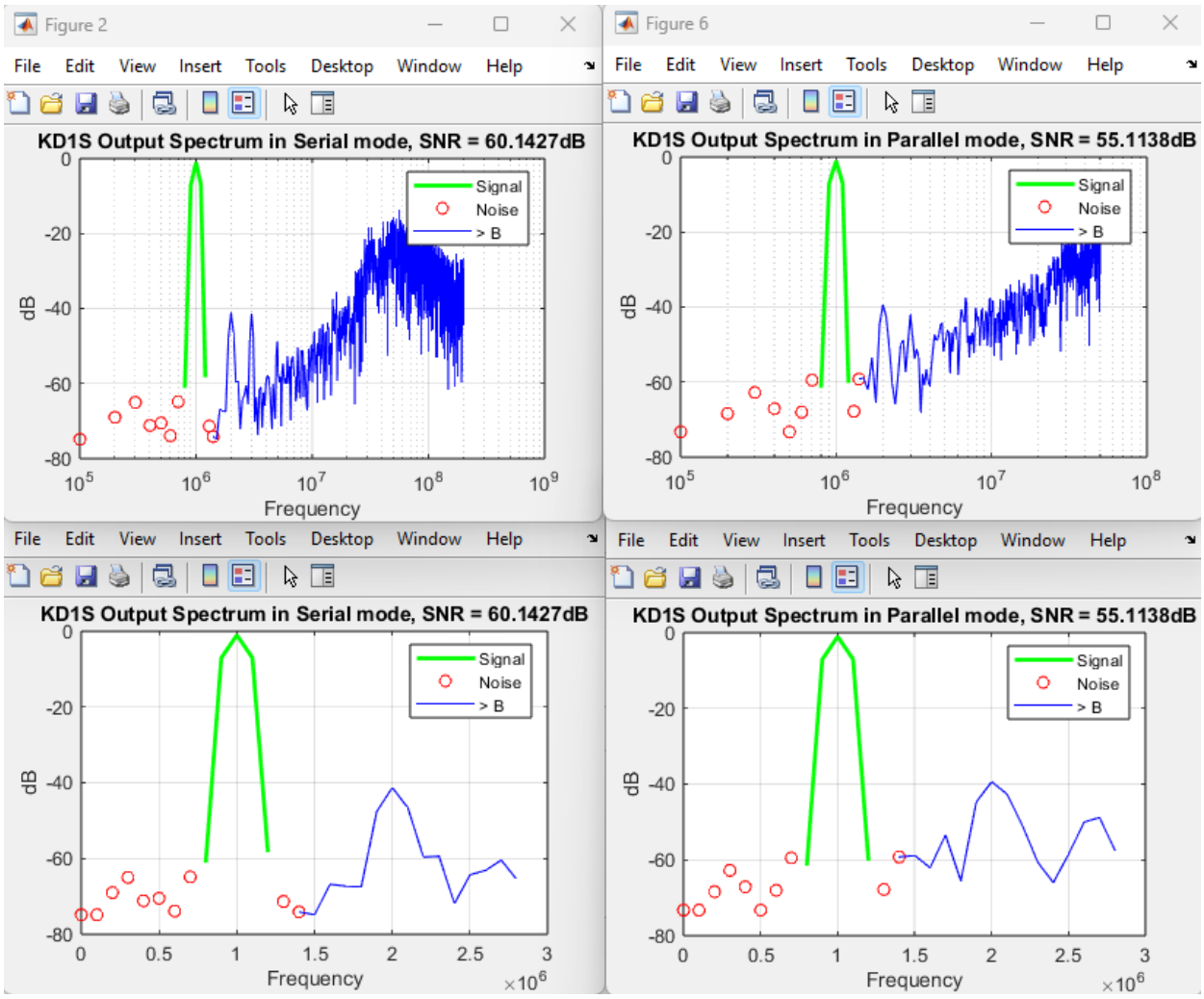



***Figure 25: SNR in Serial/Parallel Mode for 2nd Order 4-Path KD1S, OSR = 128***

The results below show the SNR, $N_{eff}$, and Bandwidth values at OSR values of 32, 64, and 128 in both serial and parallel modes, verifying the waveforms above. There is a major improvement over the board, with all the results seen in Tables 1 and 2 for both topologies.

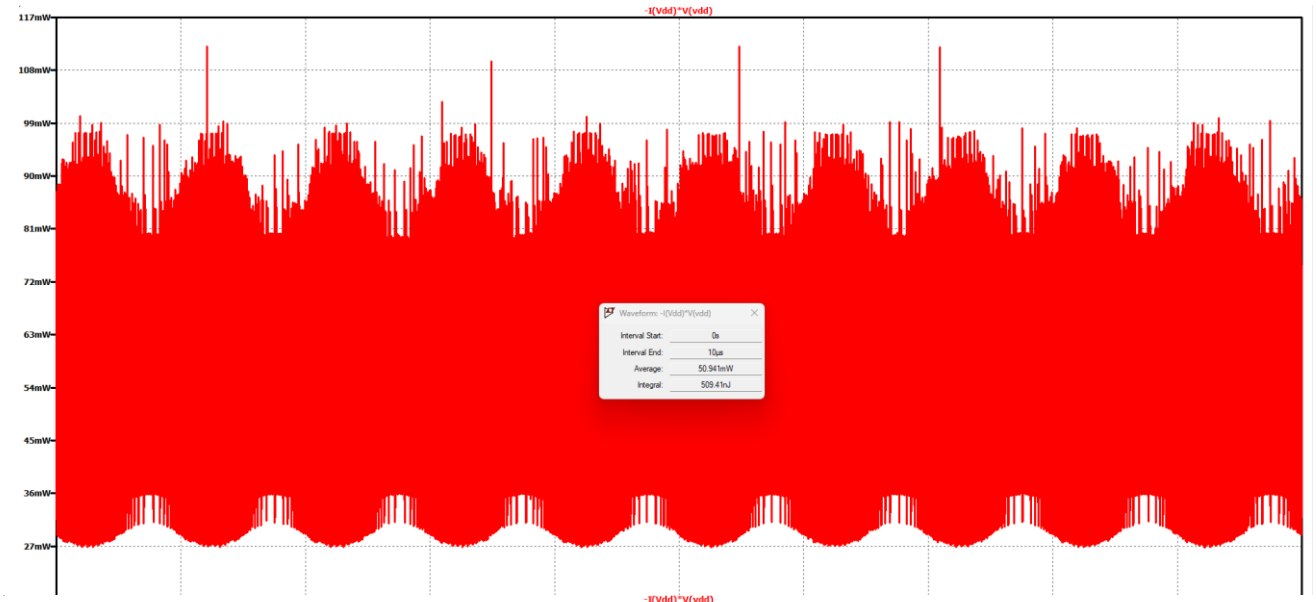
```
Kpath = 4 OSR = 32
For 1-bit output (serial mode) at Kpath*fs = 403 MHz
SNR = 43.41, Neff = 6.92, B = 6.29 MHz
For Kpath-bits output (parallel mode) at fs = 101 MHz
SNR = 34.86, Neff = 5.49, B = 6.29 MHz>> Fig9_33_2ndorder_Matlab

Kpath = 4 OSR = 64
For 1-bit output (serial mode) at Kpath*fs = 403 MHz
SNR = 53.92, Neff = 8.66, B = 3.15 MHz
For Kpath-bits output (parallel mode) at fs = 101 MHz
SNR = 44.99, Neff = 7.18, B = 3.14 MHz>> Fig9_33_2ndorder_Matlab

Kpath = 4 OSR = 128
For 1-bit output (serial mode) at Kpath*fs = 403 MHz
SNR = 60.14, Neff = 9.69, B = 1.57 MHz
For Kpath-bits output (parallel mode) at fs = 101 MHz
SNR = 55.11, Neff = 8.86, B = 1.57 MHz>> Fig9_33_Matlab
>> Fig9_33_Matlab
```

***Figure 26: SNR, $N_{eff}$, and Bandwidth Results in Serial/Parallel Mode for 2nd Order 4-Path KD1S***

# II. Power Consumption

Power consumption stands out as the most critical aspect to prioritize in the contemporary era, as it significantly influences the overall efficiency, scalability, and thermal management of KD1S in real-world applications. Using LTspice, the average power consumption of the 1st and 2nd order KD1S topologies was analyzed and plotted in Figures 27 and 28. To ensure accurate values, the waveforms were measured over ten cycles. In Figure 27, corresponding to the 1st order 8-path KD1S topology, the average power consumption is approximately 50.94 mW. Most of the power consumption comes from the differential amplifier, so this consideration is important when increasing the order of KD1S topologies, as each additional order comes requires an additional amplifier. In Figure 28, representing the 2nd order 4-path KD1S topology, the average power consumption is approximately 78.52mW. Comparing the two topologies, we can see that while the second-order topology consumes more power, it offers enhanced performance in terms of SNR and effective number of bits, providing a trade-off between efficiency and performance.

***Figure 27: Average Power Consumption of the 1st Order 8-Path KD1S***



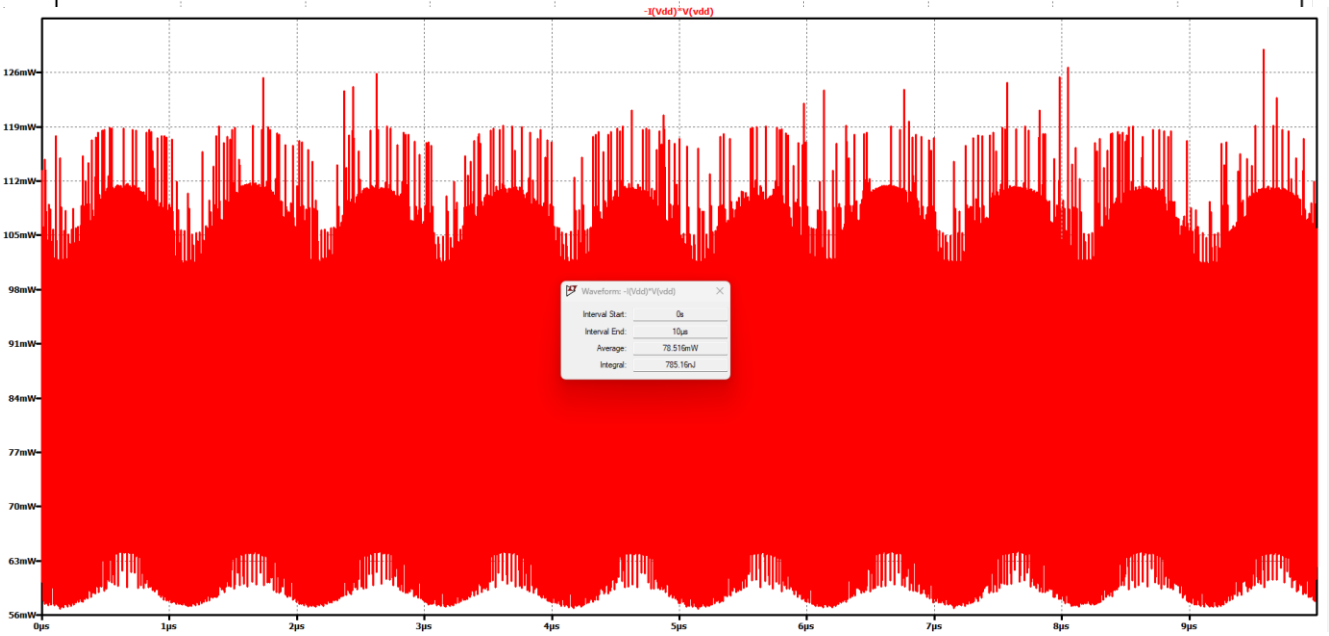




***Figure 28: Average Power Consumption of the 2nd Order 4-Path KD1S***

# III. Changing Input Frequencies (Experimental Results)

This section evaluates the performance of the 1st order and 2nd order topologies under varying input frequencies. While the original topologies were tested with an input frequency of 1MHz, the results below explore the impact of increasing the input frequency to 3MHz. This change in frequency reduces the transient duration to 3.1us, allowing ten cycles to plot for a more direct comparison towards our original results. Focusing first on the 1st order topology with an input frequency of 3MHz, the waveform behavior has many notable differences, which can be seen in Figure 29. The *bitsum* output exhibits fewer spiky transitions but introduces several dead zones throughout the waveform. In terms of average power consumption, both input frequencies range around 50-51 mW. These hardships significantly impact the overall performance, and this can be seen when extracting the output data to MATLAB for analysis. Like the previous procedure, the SNR, $N_{eff}$, and bandwidth values are measured across oversampling ratios of 64, 128, and 256, whose results can be seen in Table 3. When comparing the performance in Table 3 to Table 1, there is an overall reduction in performance across the board. However, there are exceptions in the parallel mode where the SNR increases by 5.37 dB and the $N_{eff}$ improves by 0.9 bits for an oversampling ratio of sixty-four. Therefore, it is safe to say the 1st order 8-path topology with a 1 MHz input frequency demonstrates superior overall performance compared to the 3 MHz input frequency.

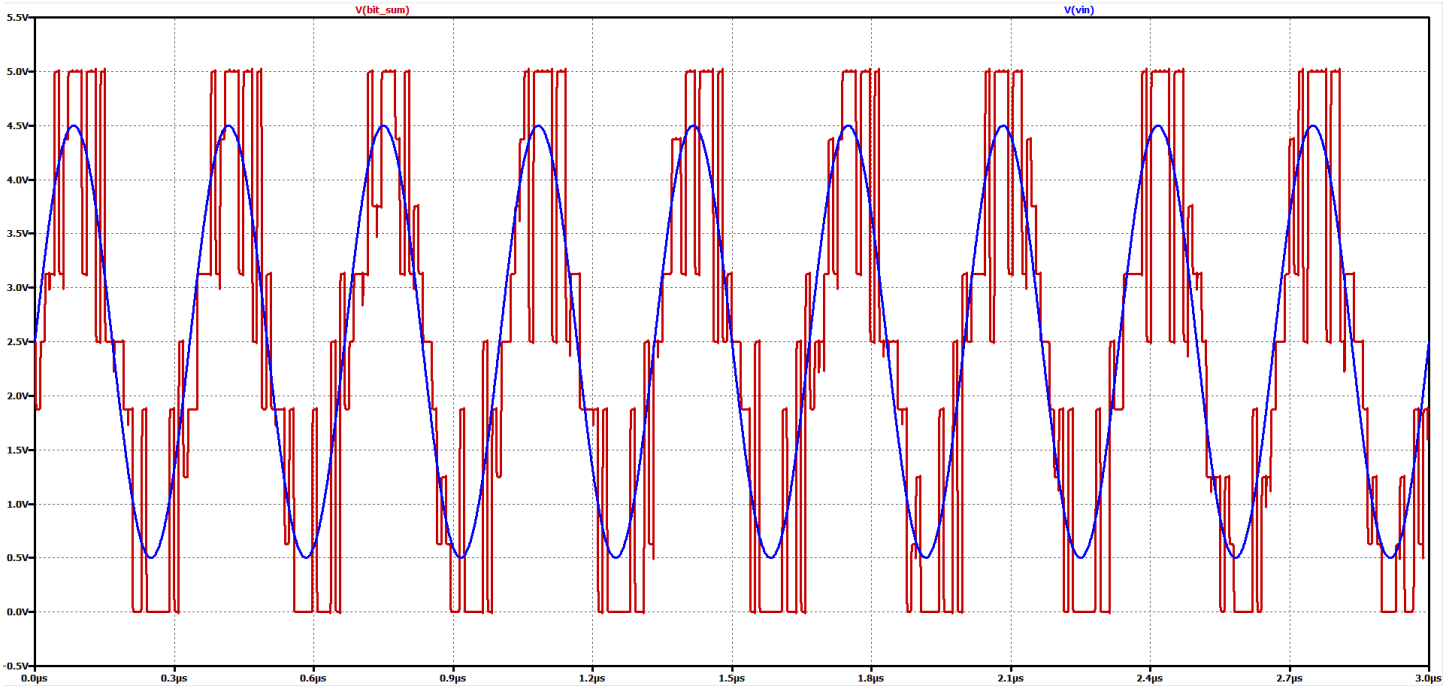



*Figure 29: Input and Output Waveforms of the 1st Order 8-Path CT KD1S Topology at 3MHz*

| | 1st Order 8-Path KD1S Project Performance (3MHz) | | | | | |
|---|---|---|---|---|---|---|
| **OSR** | **64** | | **128** | | **256** | |
| **Mode** | **Serial** | **Parallel** | **Serial** | **Parallel** | **Serial** | **Parallel** |
| **$F_{s,new}$** | **807MHz** | **101MHz** | **807MHz** | **101MHz** | **807MHz** | **101MHz** |
| **SNR** | **38.78 dB** | **36.13 dB** | **42.35 dB** | **42.72 dB** | **45.10 dB** | **45.94 dB** |
| **$N_{eff}$** | **6.15 Bits** | **5.71 Bits** | **6.74 Bits** | **6.80 Bits** | **7.20 Bits** | **7.34 Bits** |
| **Bandwidth** | **6.31 MHz** | **6.29 MHz** | **3.15 MHz** | **3.14 MHz** | **1.58 MHz** | **1.57 MHz** |
| **$P_{avg}$** | **51.04 mW** | | | | | |

*Table 3: 1st Order 8-Path KD1S Project Performance at 3MHz*

Moving on to the 2nd order topology with an input frequency of 3MHz, the input and output waveforms are depicted in Figure 30. In this scenario, the *bitsum* output shows good improvements; specifically, the dead zones are significantly minimized, the waveform spikes are more frequent, and the output tracks the input more effectively. In terms of power consumption, both input frequencies exhibit similar values of approximately 78.5 mW, rendering the difference to be negligible for comparison. To further evaluate its performance, the output is once again extracted to MATLAB, where the SNR, $N_{eff}$, and bandwidth are measured for oversampling ratios of 32, 64, and 128. These results can be seen in Table 4, where the results demonstrate an outstanding improvement across all metrics compared to Table 2. This also contrasts sharply with the performance comparisons seen in the 1st order topology, where increasing the frequency resulted in a reduction of performance. There are also no exceptions where the 1MHz input frequency outperforms the 3MHz input frequency. Therefore, this highlights that increasing the input frequency for a second-order topology can offer substantial gains, which is a strong recommendation for future design optimizations related to this specific topology.

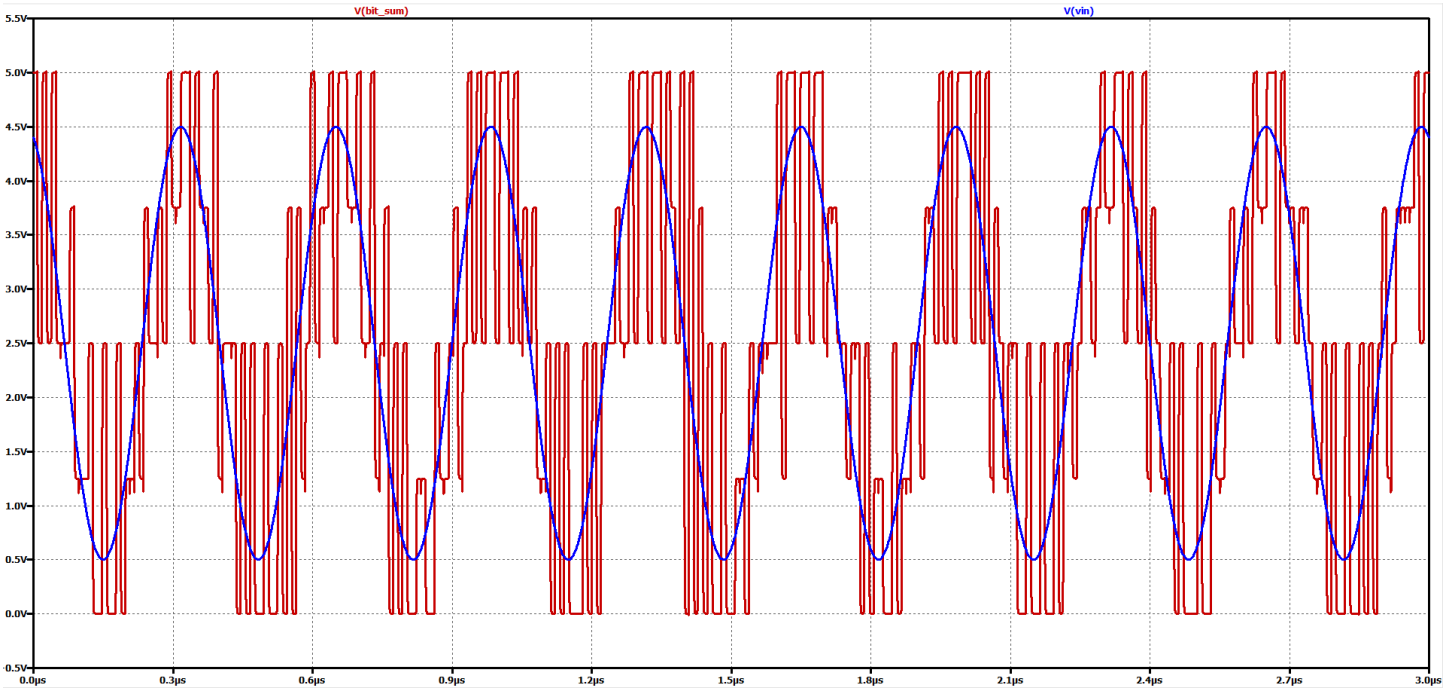



*Figure 30: Input and Output Waveforms of the 2nd Order 4-Path CT KD1S Topology at 3MHz*

| | 2nd Order 4-Path KD1S Project Performance (3MHz) | | | | | |
|---|---|---|---|---|---|---|
| **OSR** | **32** | | **64** | | **128** | |
| **Mode** | **Serial** | **Parallel** | **Serial** | **Parallel** | **Serial** | **Parallel** |
| **$F_{s,new}$** | **403MHz** | **101MHz** | **403MHz** | **101MHz** | **403MHz** | **101MHz** |
| **SNR** | **49.77 dB** | **35.27 dB** | **54.72 dB** | **50.58 dB** | **64.58 dB** | **58.65 dB** |
| **$N_{eff}$** | **7.97 Bits** | **5.56 Bits** | **8.79 Bits** | **8.11 Bits** | **10.43 Bits** | **9.45 Bits** |
| **Bandwidth** | **6.30 MHz** | **6.28 MHz** | **3.15 MHz** | **3.14 MHz** | **1.58 MHz** | **1.57 MHz** |
| **$P_{avg}$** | **78.47 mW** | | | | | |

*Table 4: 2nd Order 4-Path KD1S Project Performance at 3MHz*

# IV. Changing Input Sources (Ramp & DC) (Experimental Results)

While the previous section examined the performance of the topologies with varying input frequencies, this section focuses on analyzing the behavior under different input types, particularly transitioning from sinusoidal inputs to slow ramp and DC inputs.

Starting with the first-order topology, our input is a fixed DC voltage of 1.5V, and the waveforms are measured over a 3us period as shown in Figure 31. The results indicate that the average *bitsum* output is approximately 1.28V, which is close to the input signal.

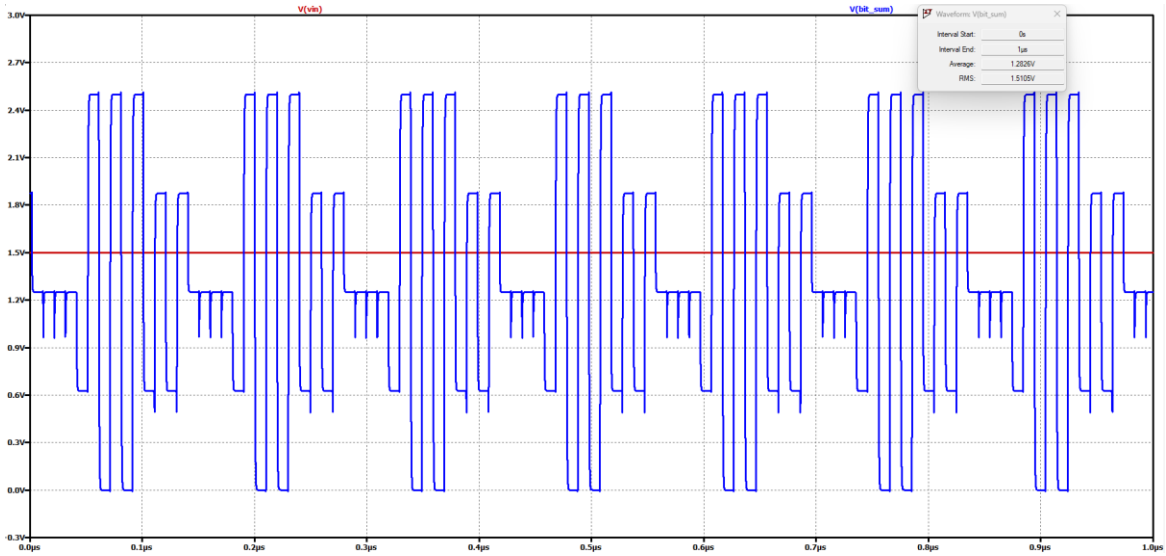



***Figure 31: Input and Output Waveforms of the 1st Order 8-Path CT KD1S Topology at DC***

For the 2nd order topology, the same test is conducted using a fixed DC input voltage of 1.5V, with waveforms measured over a 3us period to ensure a direct comparison with the 1st order topology. The input and output waveforms can be seen in Figure 32, where the *bitsum* output achieves an average value of approximately 1.62V. This is only 120mV away from the input signal, which is an improvement compared to the 220mV discrepancy from the 1st order topology. In a visual sense, the 2nd order topology is seen to have more frequent changes in the output waveform and fewer dead zones, which demonstrate its superior performance for scenarios with a fixed DC voltage input.

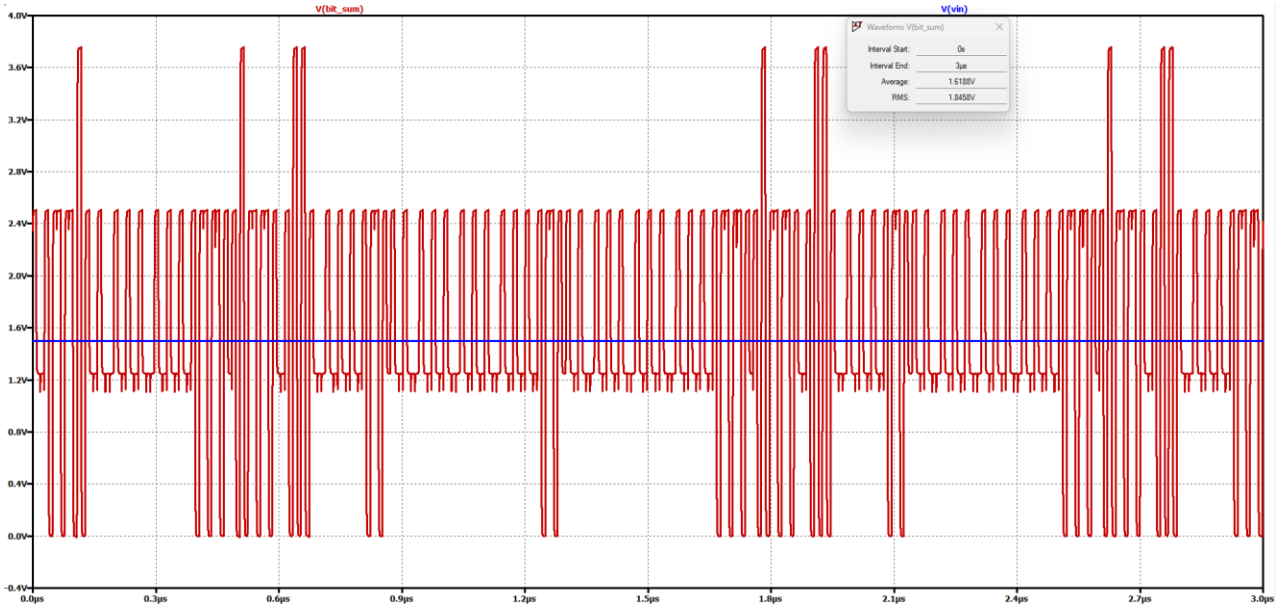



***Figure 32: Input and Output Waveforms of the 2nd Order 4-Path CT KD1S Topology at DC***

Returning to the 1st order topology, the next scenario involves analyzing the performance with a slow ramp input signal. In this configuration, a pulse source sweeps from 0 to 5V over a period of 10us, and the input and output waveforms can be seen in Figure 33. The regions highlighted in orange, with black arrows added for visual clarity, indicate prominent dead zones observed throughout the output waveform. These dead zones significantly degrade the performance of the topology, and it is most noticeable at voltages near ground and the supply voltage. This behavior stems from the input and feedback signal having equal magnitudes, causing the output code to repeat continuously until the circuit transitions out of the dead zone.

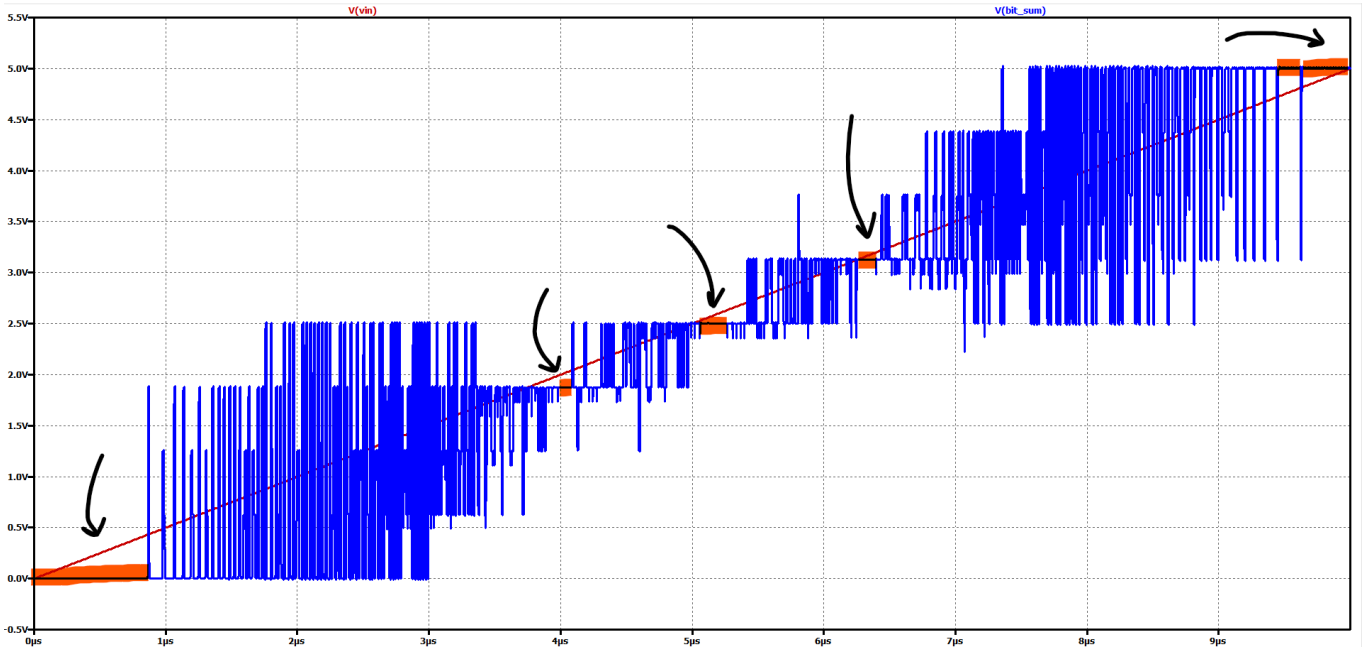



***Figure 33: Input and Output Waveforms of the 1st Order 8-Path CT KD1S Topology with a Slow Ramp Input***

The 2nd order topology is evaluated using the same configuration, with the input and *bitsum* output waveforms shown in Figure 34. Visually, the presence of dead zones is significantly reduced compared to the 1st order topology, and any dead zones that are present are very minor and have relatively little impact in terms of performance. Additionally, the dead zones that appeared near the ground and supply voltage in the 1st order topology is absent here. This improvement highlights the recommendation of the 2nd order topology in scenarios with slow ramp input signals.

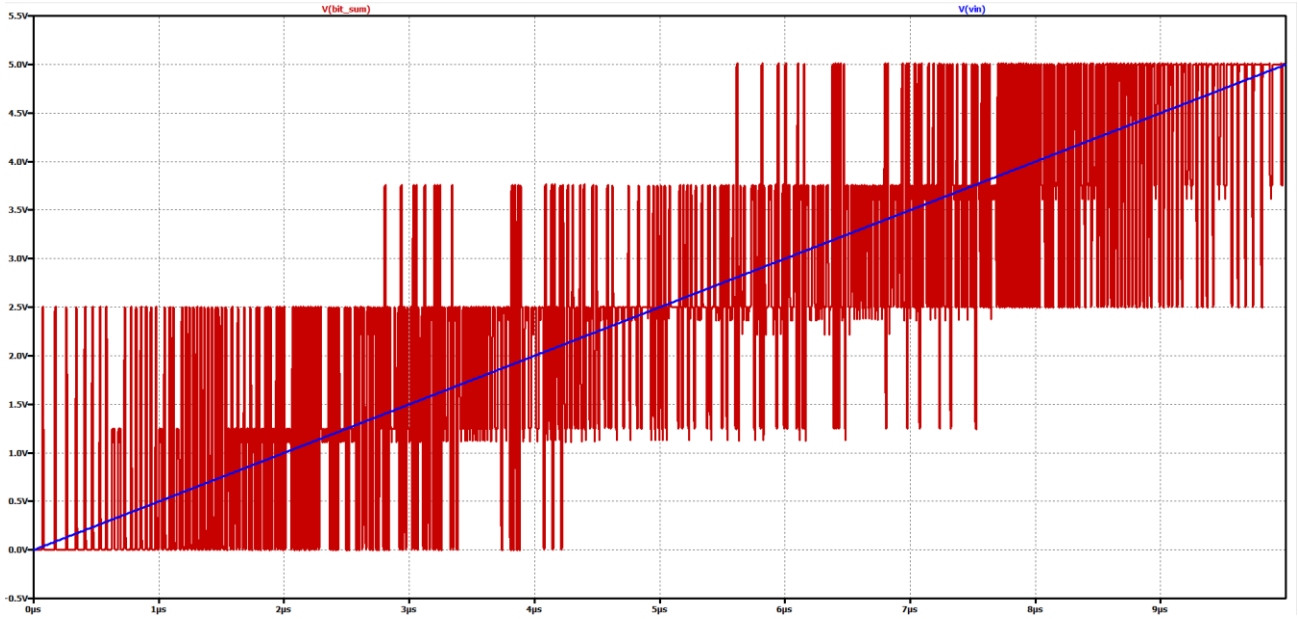



***Figure 34: Input and Output Waveforms of the 2nd Order 4-Path CT KD1S Topology with a Slow Ramp Input***

# V. Ideal Simulated Values in Figure 9.33

Figure 9.33 from the *CMOS Mixed-Signal Circuit Design* textbook provides the ideal performance metrics for the 1st-Order 8-Path KD1S topology, which serves as the baseline benchmark for evaluating and improving the contemporary designs presented in the report. The results for key performance metrics including SNR, $N_{eff}$, bandwidth, and power consumption are analyzed for OSRs of 64, 128, and 256. Table 5 presents these results for an input frequency of 1MHz, while Table 6 displays the performance for an input frequency of 3MHz. The MATLAB scripts are provided for Figure 9.33, which allows us to calculate and compare the performances between distinctive designs. While the serial and parallel modes have different frequencies compared to the designs made in Table 1 & 2, one of the most significant improvements can be seen in the reduction of the average power consumption.

| | Ideal 1st Order 8-Path KD1S Project Performance (1MHz) | | | | | |
|---|---|---|---|---|---|---|
| **OSR** | **64** | | **128** | | **256** | |
| **Mode** | **Serial** | **Parallel** | **Serial** | **Parallel** | **Serial** | **Parallel** |
| **$F_{s,new}$** | **1830MHz** | **228MHz** | **1830MHz** | **228MHz** | **1830MHz** | **228MHz** |
| **SNR** | **39.82 dB** | **36.16 dB** | **45.68 dB** | **41.72 dB** | **59.51 dB** | **60.02 dB** |
| **$N_{eff}$** | **6.32 Bits** | **5.71 Bits** | **7.29 Bits** | **6.63 Bits** | **9.59 Bits** | **9.67 Bits** |
| **Bandwidth** | **14.29 MHz** | **14.28 MHz** | **7.15 MHz** | **7.14 MHz** | **3.57 MHz** | **3.57 MHz** |
| **$P_{avg}$** | **68.55 mW** | | | | | |

*Table 5: Figure 9.33 1st Order 8-Path KD1S Project Performance at 1MHz*

| | Ideal 1st Order 8-Path KD1S Project Performance (3MHz) | | | | | |
|---|---|---|---|---|---|---|
| **OSR** | **64** | | **128** | | **256** | |
| **Mode** | **Serial** | **Parallel** | **Serial** | **Parallel** | **Serial** | **Parallel** |
| **$F_{s,new}$** | **1830MHz** | **228MHz** | **1830MHz** | **228MHz** | **1830MHz** | **228MHz** |
| **SNR** | **40.37 dB** | **37.61 dB** | **51.43 dB** | **49.89 dB** | **54.28 dB** | **53.61 dB** |
| **$N_{eff}$** | **6.41 Bits** | **5.95 Bits** | **8.25 Bits** | **7.99 Bits** | **8.72 Bits** | **8.61 Bits** |
| **Bandwidth** | **14.29 MHz** | **14.28 MHz** | **7.15 MHz** | **7.14 MHz** | **3.57 MHz** | **3.57 MHz** |
| **$P_{avg}$** | **65.61 mW** | | | | | |

*Table 6: Figure 9.33 1st Order 8-Path KD1S Project Performance at 3MHz*

# Summary & Future Improvements

The two main designs in the report include the 1st order 8-Path K-Delta-1-Sigma (KD1S) modulator and the 2nd order 4-Path KD1S modulator as a replacement for the ADC seen in Figure 9.32 of the *CMOS Mixed-Signal Design* textbook.

Despite the satisfactory performance shown by our 1st order 8-Path KD1S topology, the 2nd order 4-path KD1S topology outperforms significantly across all performance metrics and key design considerations. While the 1st order topology's primary advantage lies in its lower power consumption, the 2nd order topology was deemed the most optimal design due to its superior SNR performance compared to all other 8-path designs at equivalent OSRs. Notably, the 2nd order KD1S topology, with half the number of paths, achieves higher SNR and effective number of bits ($N_{eff}$) at lower OSRs and operates at a lower sampling frequency than the ideal frequency values outlined in Tables 5 and 6. Even under slow ramp and DC input scenarios, the 2nd order 4-path KD1S topology consistently minimized dead zones, tracked input signals more accurately, and demonstrated greater responsiveness than the 1st order 8-Path KD1S topology. Its performance also improved significantly at higher input frequencies, particularly at 3 MHz. In this configuration, the 2nd order 4-path KD1S topology achieved peak SNR values of 64.58 dB (10.43 effective bits) in serial mode and 58.65 dB (9.45 bits) in parallel mode, with an oversampling ratio of 128. The average power consumption of approximately 78.5 mW, though higher than the 1st order 8-Path KD1S topology, is justified by its superior performance. There are several trade-offs seen in all the main components, including the clock generator, comparator, and differential amplifier:

- **Clock Generator:** The voltage-controlled design allows user-preferred adjustments, but the clock signals' duty cycle exceeded 50%, which introduces errors in the overall performance. To address this, complementary signals can be generated using inverters and implemented directly into the transmission gates, allowing the clock signals to have an ideal 50% duty cycle. This implementation would improve the overall performance of the topology.
- **Differential Amplifier:** A simple differential amplifier was used to minimize layout size and power consumption, at the expense of the gain. Future designs could explore alternative topologies to achieve higher gain while still maintaining low power consumption.
- **Comparator:** The comparator is arguably the most significant component in the design, as each feedback path requires one comparator. The current delay on the rising edge could be improved by increasing transistor widths, but this would also increase layout size and power consumption. In terms of future optimization, finding a balance between quick decisions and low power consumptions is the best direction moving forward.
- **Inverters:** Throughout the entire design, high-width inverters were used to ensure proper current sinking and signal driving, which is very apparent in the comparator and differential amplifier. However, the increase in transistor widths cause the power consumption to increase, as it prioritizes speed and strength. In the future, the optimal path should aim to reduce widths just enough to balance power efficiency with signal speed.

While the designs do not fully achieve the ideal SNR and $N_{eff}$ values predicted in theoretical calculations, they perform well with the baseline configurations. Overall, optimizing the clock generator, op-amp design, and comparator configurations, along with fine-tuning RC values, will help close the gap between the performances of the design and their ideal values.