CMOS Synchronous Buck Switching Power Supply
ECG 621 Final Course Project
By Edreese Basharyar

Introduction:

The final project for ECG 621 consists of designing a CMOS Synchronous Buck Switching Power Supply, whose primary function is to step down DC voltage that varies between 4-5.5V into a steady output voltage of 3.125V. While there are many ways to create a Buck SPS, such as using a PMOS-NMOS as your final switching transistors, along with a ring oscillator attached at the end of the comparator, my design will revolve around the NMOS-NMOS design that uses a charge-pump clock driver that feeds into the top NMOS switching transistor. The Buck SPS uses a feedback loop to control the output voltage due to the feedback from the input of the comparator, which consists of a voltage divider to match the duty cycle of our design and a capacitor to smooth the signal and control any oncoming noise.

Design Approach:

The CMOS Synchronous Buck Converter consists of several main components, starting with the bandgap circuit, used as a way to provide an independent voltage reference that feeds into the (+) input of the comparator. A voltage divider along with a smoothing capacitor is used to create the intended duty cycle in the feedback loop, and it is fed into (-) input of the comparator to ideally regulate both inputs of the comparator at 1.25V. The resistors used in the voltage divider are the same resistance in order to minimize the variation of temperature, all with a value of 52kΩ. The setup of the voltage divider provides an input current of 25uA, which is in between our intended range of 10-50uA. The comparator is then used as a feedback loop for the overall circuit, and its functionality is designed at a binary-level system, where the output of the overall circuit is a logic 1 (vdd) when the voltage of the feedback loop is greater than 3.125, and a logic 0 (ground) for any values less than 3.125V. The comparator was also designed with additional buffers to minimize the delay due to the capacitive loads between the inverters used in the circuit. The output of the comparator feeds into the pull up-pull down latch circuit, whose function is to make sure the clock signals never overlap during the operation of the circuit. This will prevent the switching transistors at the end of the circuit to turn on at the same time, which minimizes the amount of crossover current. The pull-up is fed into a charge pump clock driver, which essentially doubles the input voltage in order to drive the top switching transistor due to its much larger width compared to the pull down switching transistor. The output of the switching transistors lead into the off-chip area, which includes passive components such as an inductor, capacitor, and load resistor. These passive components were hand calculated and then used in the final schematic of the design to verify its validity. With all of these components in place, the result provides a way to step down the voltage that was first introduced and use hysteresis to keep the voltage steady.

Bandgap:

Below, we will show the schematic, symbol, and layout of the bandgap circuit for my design of the Buck SPS.

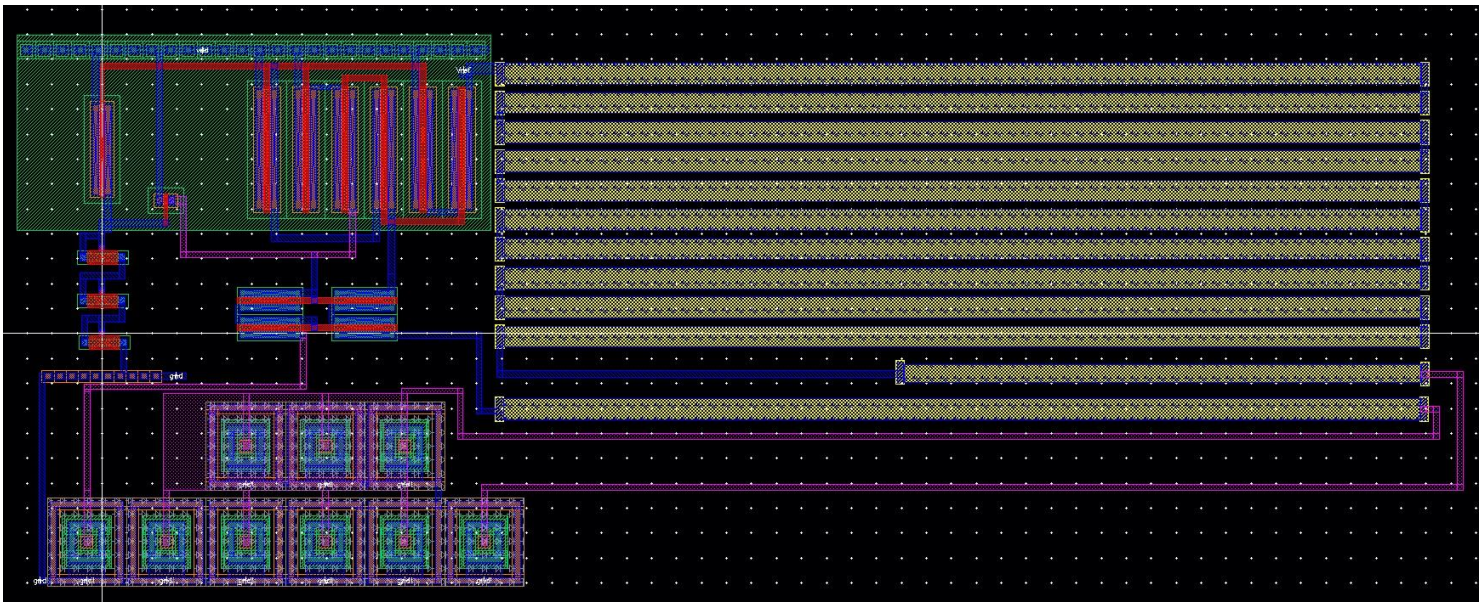

Figure 1: Bandgap Layout

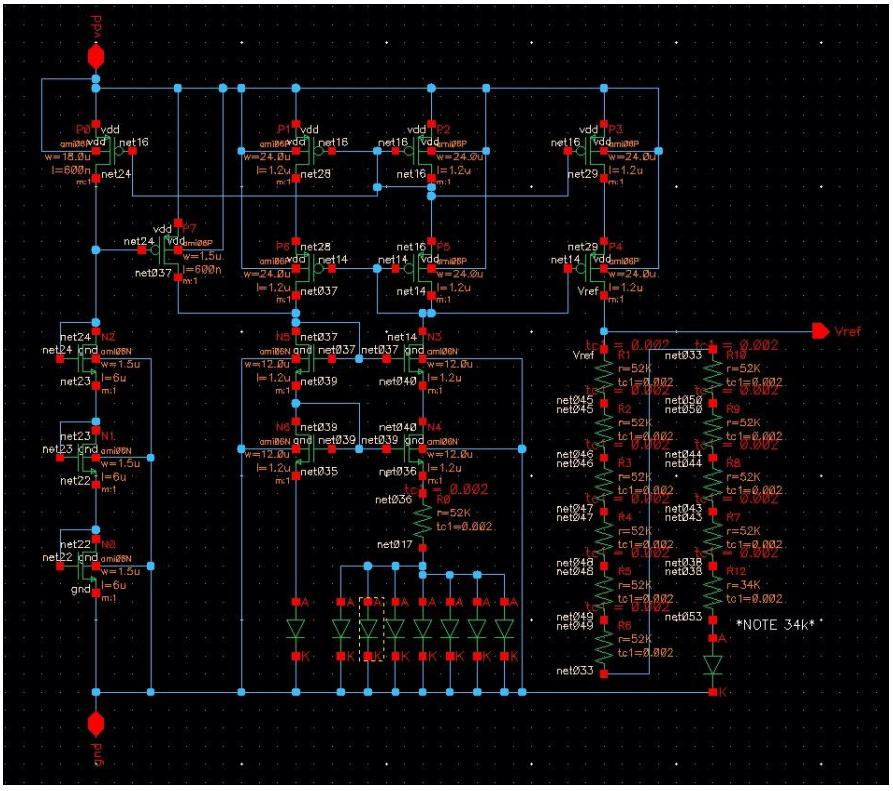

Figure 2: Bandgap Schematic

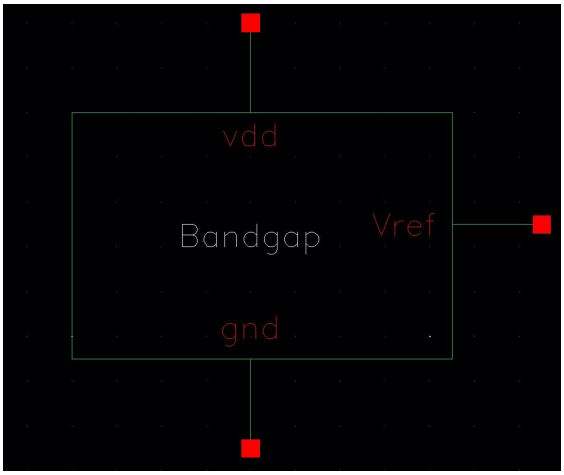

Figure 3: Bandgap Symbol

Comparator:

Below, we will show the schematic, symbol, and layout of the comparator for my design of the Buck SPS.

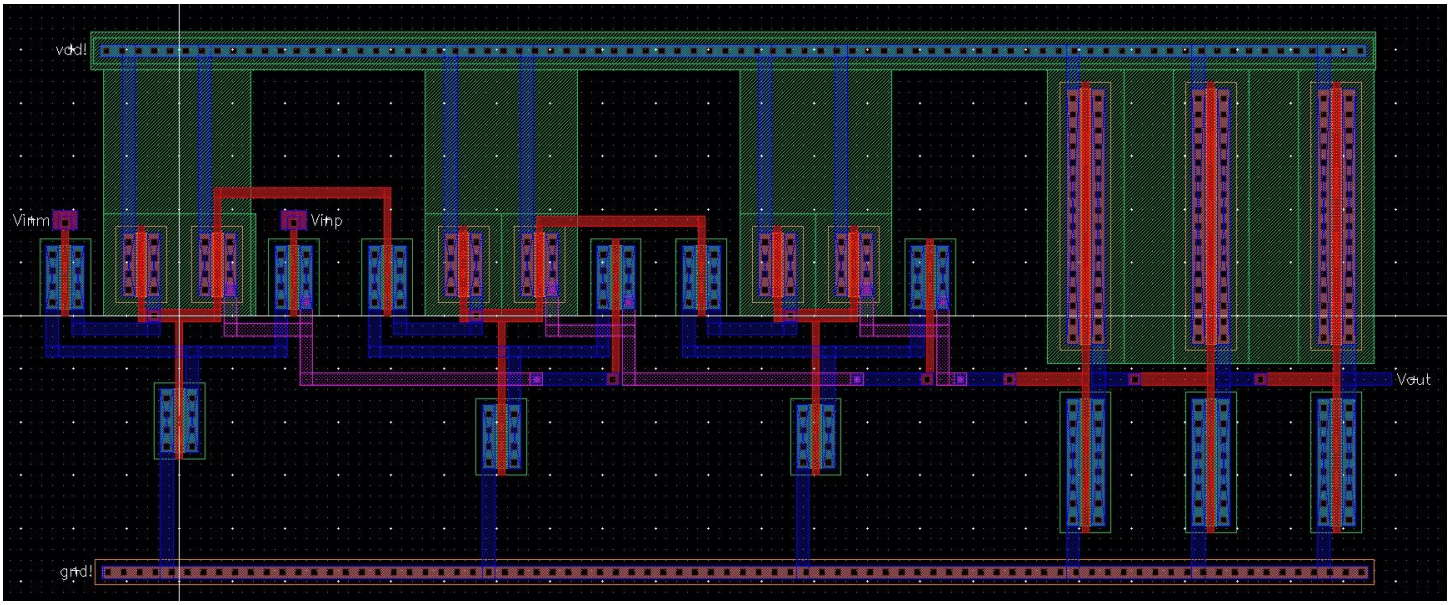

Figure 4: Comparator Layout

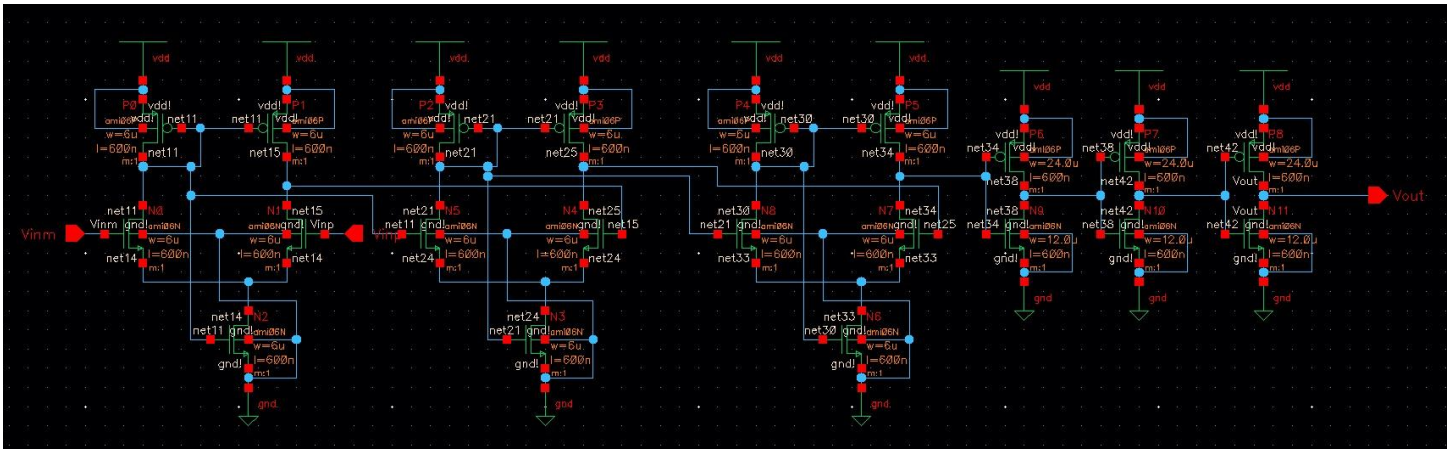

Figure 5: Comparator Schematic

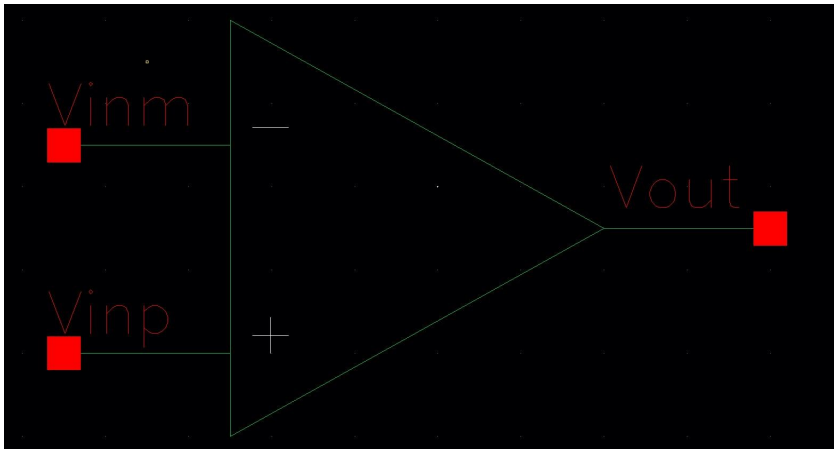

Figure 6: Comparator Symbol

Latch:

Below, we will show the schematic, symbol, and layout of the latch circuit for my design of the Buck SPS.

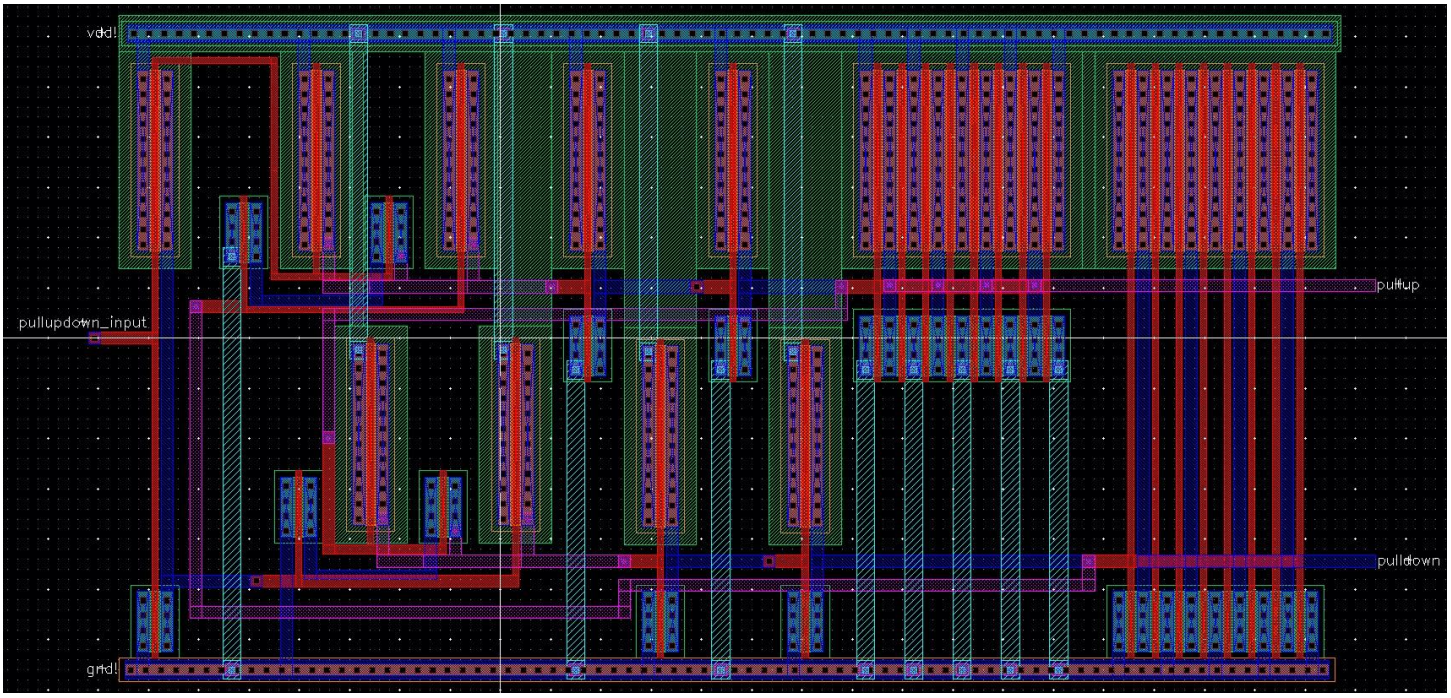

Figure 7: Latch Layout

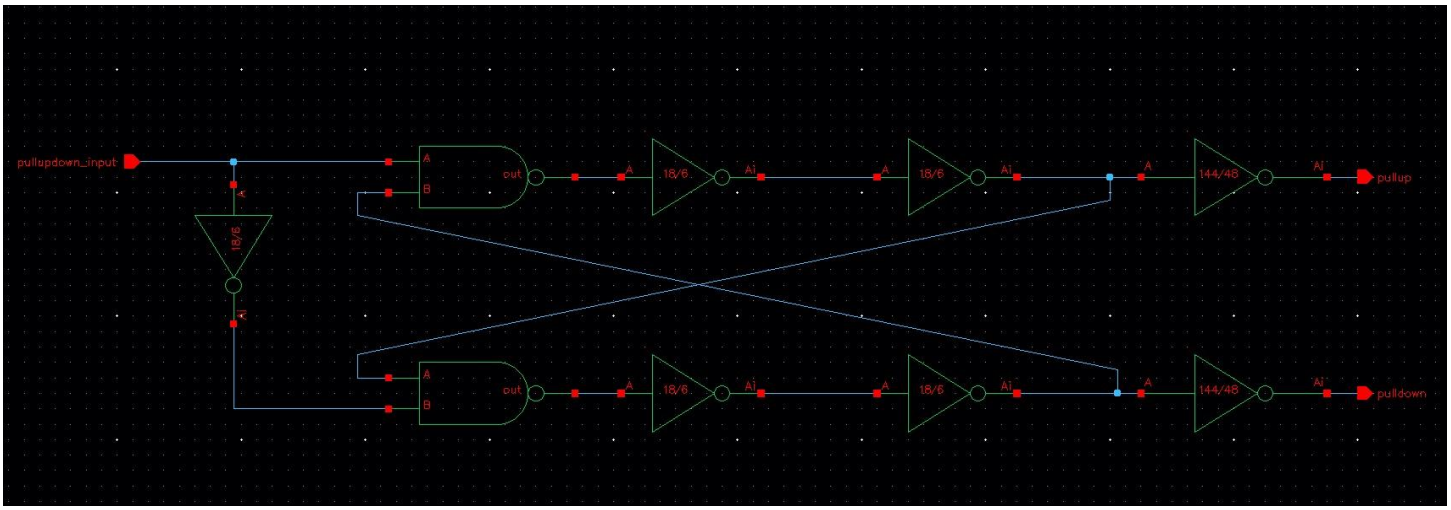

Figure 8: Latch Schematic

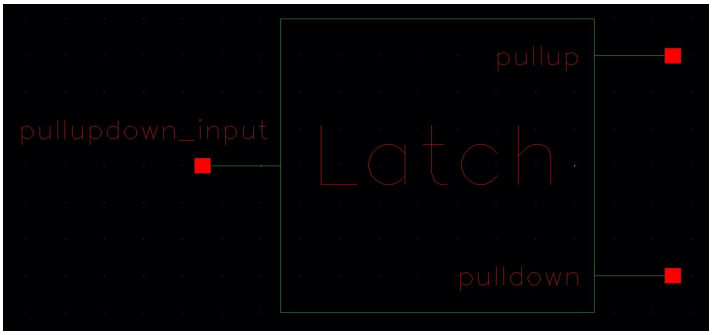

Figure 9: Latch Symbol

Charge Pump Clock Driver:

Below, we will show the schematic, symbol, and layout of the charge-pump for my design of the Buck SPS.

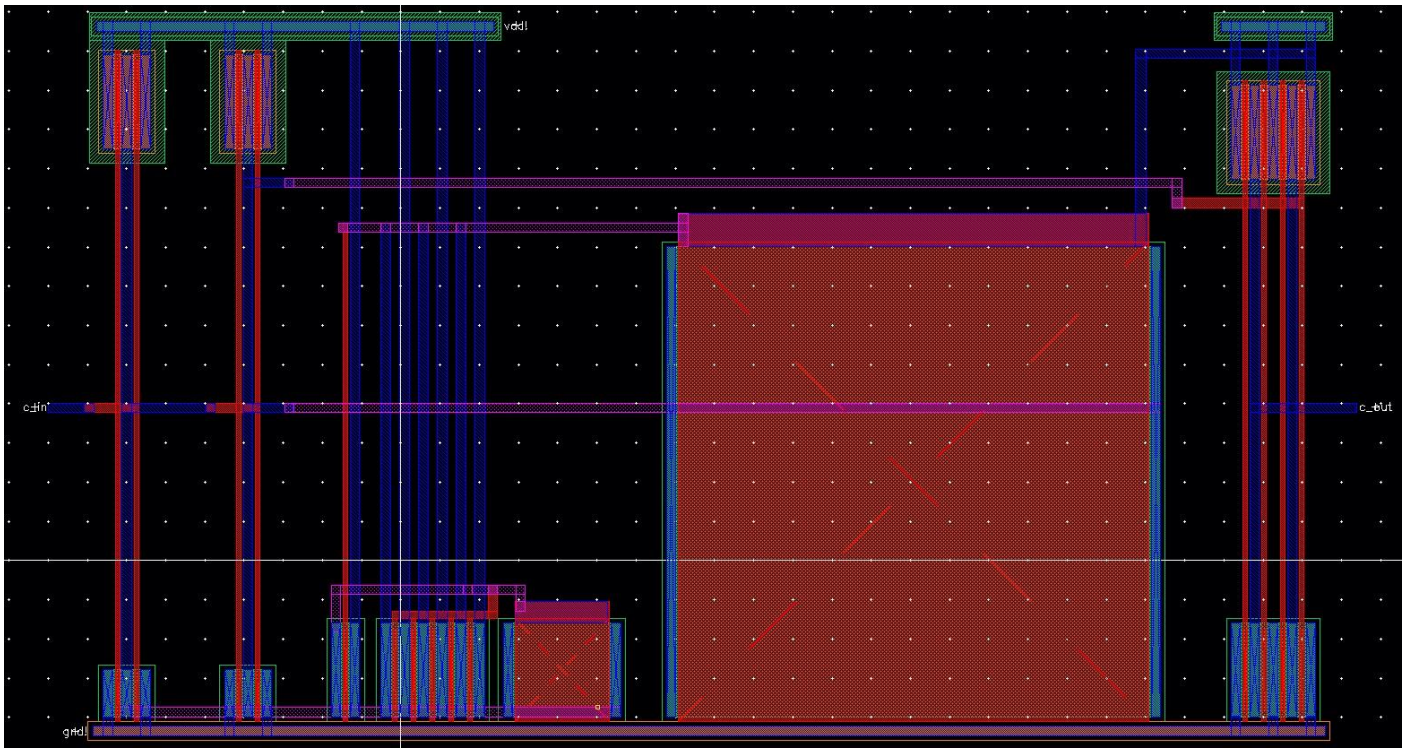

Figure 10: Charge Pump Clock Driver Layout

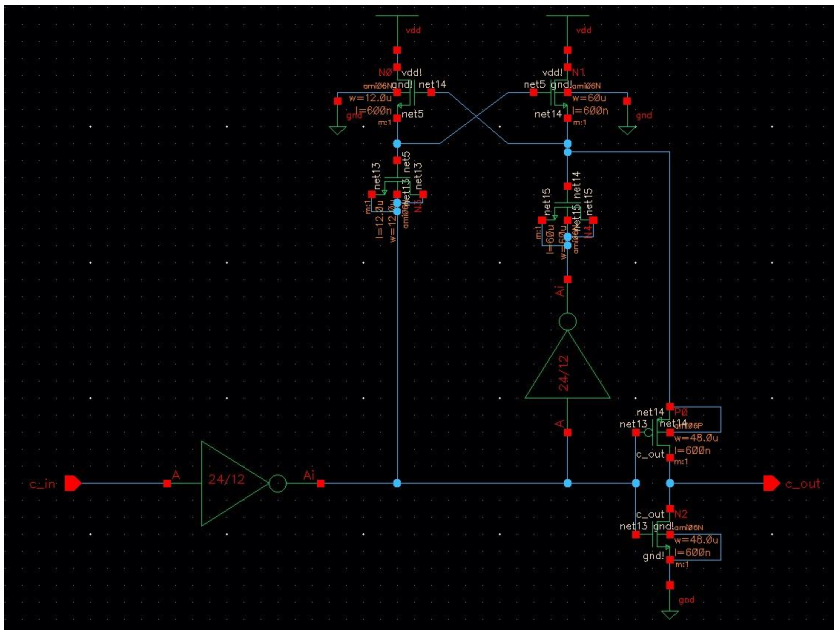

Figure 11: Charge Pump Clock Driver Schematic

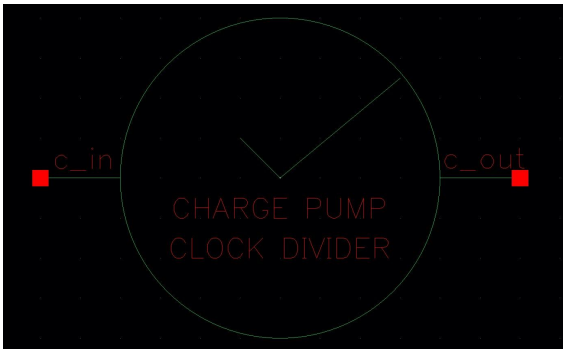

Figure 12: Charge Pump Clock Driver Symbol

Power MOSFETs (Switching Transistors):

Below, we will show the schematic, symbol, and layout of the switching transistors for my design of the Buck SPS.

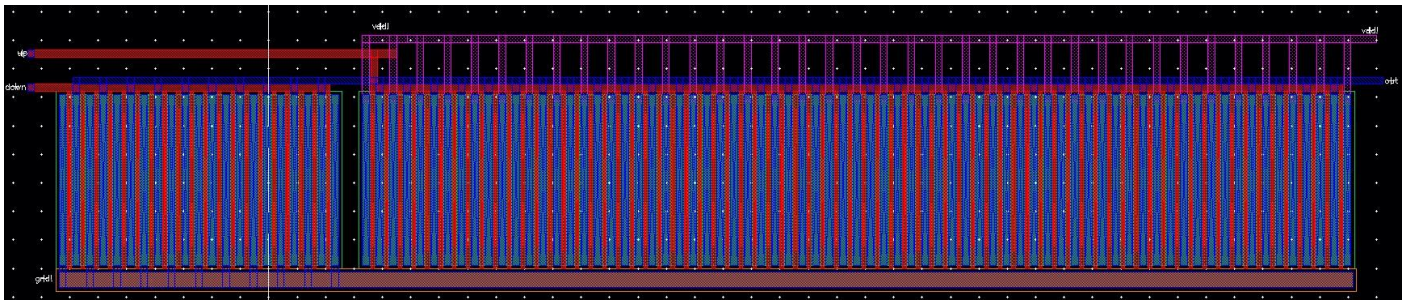

Figure 13: Power MOSFETs Layout

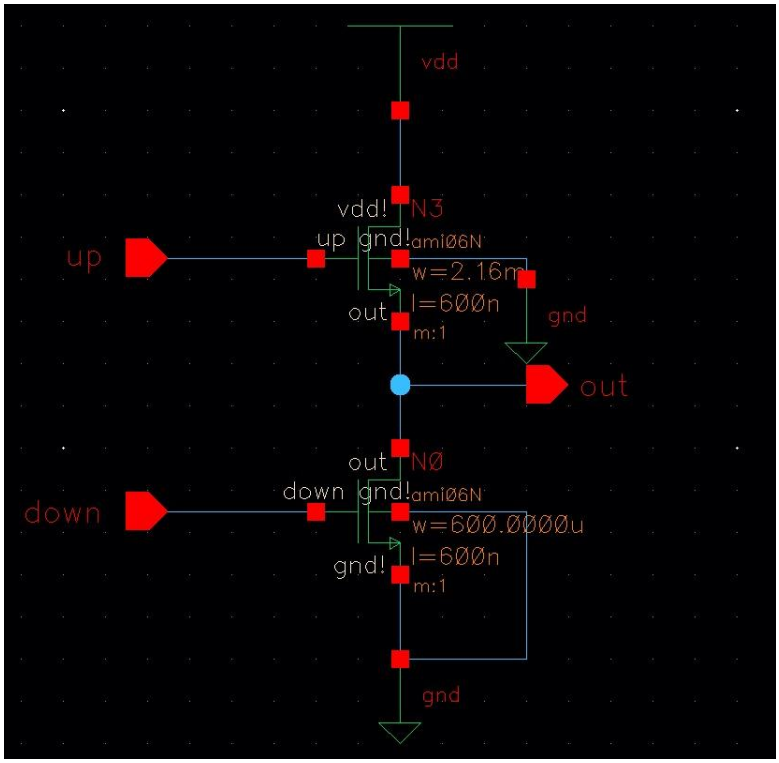

Figure 14: Power MOSFETs Schematic

Figure 15: Power MOSFETs Symbol

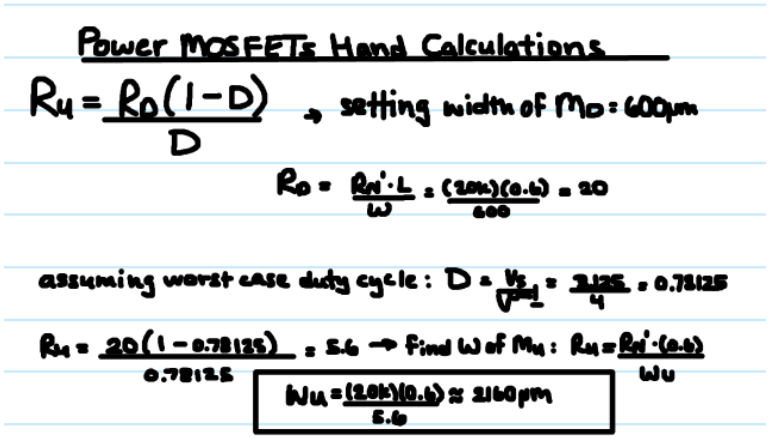

Figure 16: Hand Calculations for Power MOSFETs

Top-Level Design:

In the figure below, we can see all of the main components are all wired together, along with the voltage divider and smoothing capacitor at the feedback loop in order to create the top-level design of the Buck SPS excluding off-chip. We will now create a symbol of this schematic, include the off-chip components, and add the feedback loop to make our final, top-level design of the overall circuit. In Figure 18, we see the final layout of the Buck SPS, with every single component previously listed now wired all together in a compact and efficient display. The layout includes the four main pins that the top-level design has, such as vdd, gnd, out, and vout.

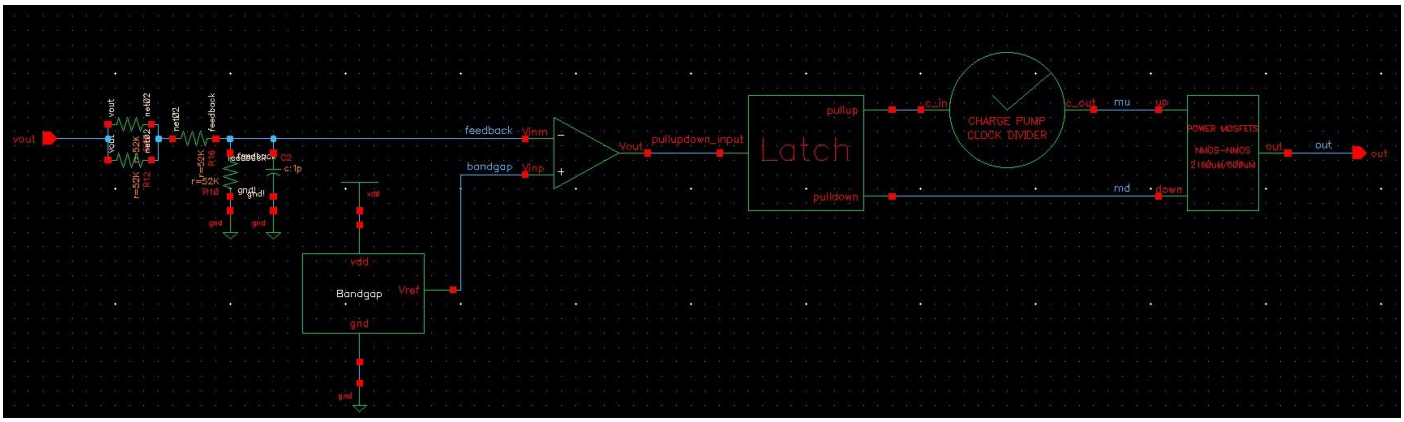

Figure 17: Schematic of Top-Level Design (excluding off-chip)

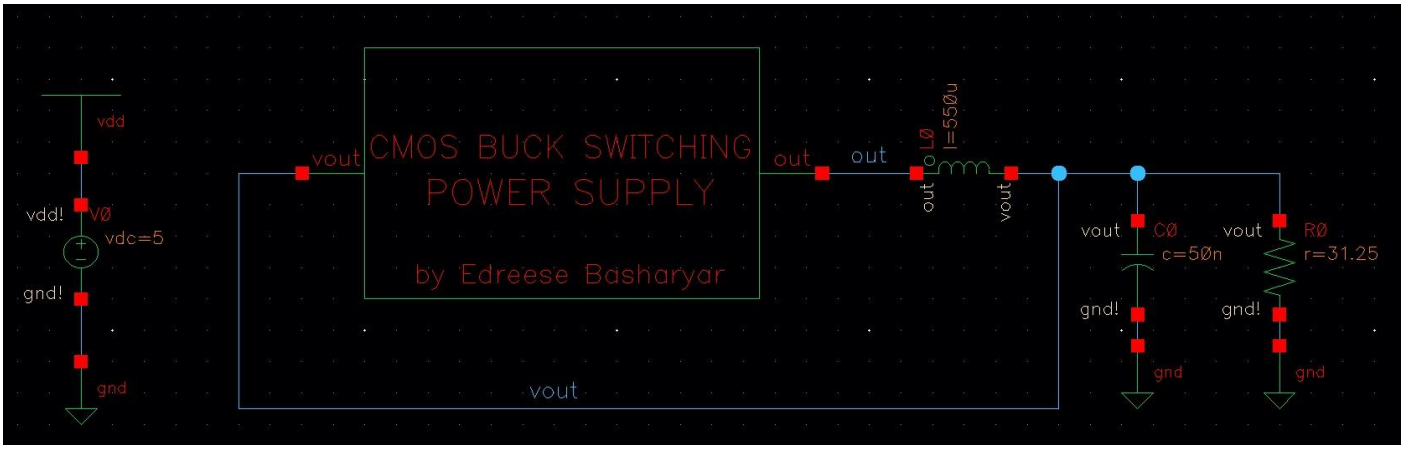

Figure 18: Symbol of Top-Level Schematic + Schematic of Top-Level Design (including off-chip)

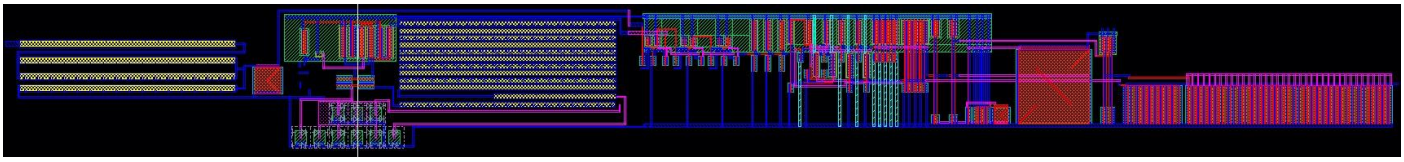

Figure 19: Final Layout of Buck SPS

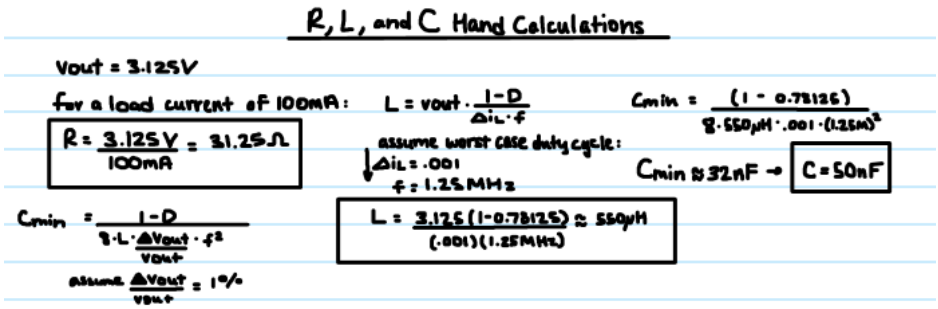

Figure 20: Hand Calculations for off-chip components including R, L, and C values

Simulations:

After showing all of the layouts, schematics, symbols, and hand calculations of the Buck SPS, it is time to show how the circuit simulates in different scenarios and situations, including temperature sweeps, supply voltage sweeps, efficiency calculations, and waveforms of all the main nodes used in the top-level schematic of the design. The figure below shows how the Buck SPS reacts to different supply voltages, specifically from 4V to 5.5V. In this waveform, the two nodes being probed are the output voltage before the inductor, indicated by *out*, and the feedback voltage that comes after the inductor and into the voltage divider before the comparator, indicated by *vout*. We can see that for all supply voltages that we have sweeped, we can see that the output voltage reaches 3.125V, and ripples at a reasonable amount similar to what we assumed in our hand calculations. The feedback voltage for all supply voltages also correctly jumps from 5V to -700mV, as it acts as a reverse-biased diode when the bottom transistor turns off.

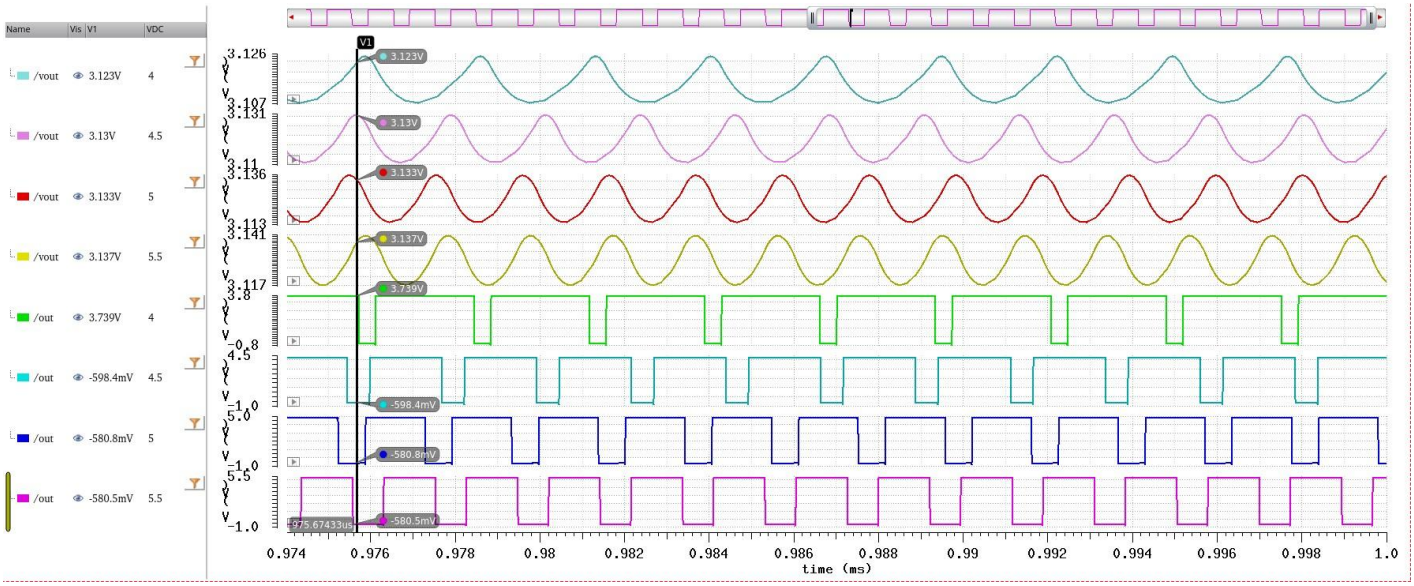

Figure 21: Transient Response of out and vout

The figure below shows how the Buck SPS reacts to different supply voltages. This specific waveform is probing the current through the inductor, indicated by *L0/PLUS*, and the current through the load resistor, indicated by *R0/PLUS*. We can see that the current through the inductor for all different VDD values is 100mA, with small and reasonable ripple values that match reasonably with our hand calculations.

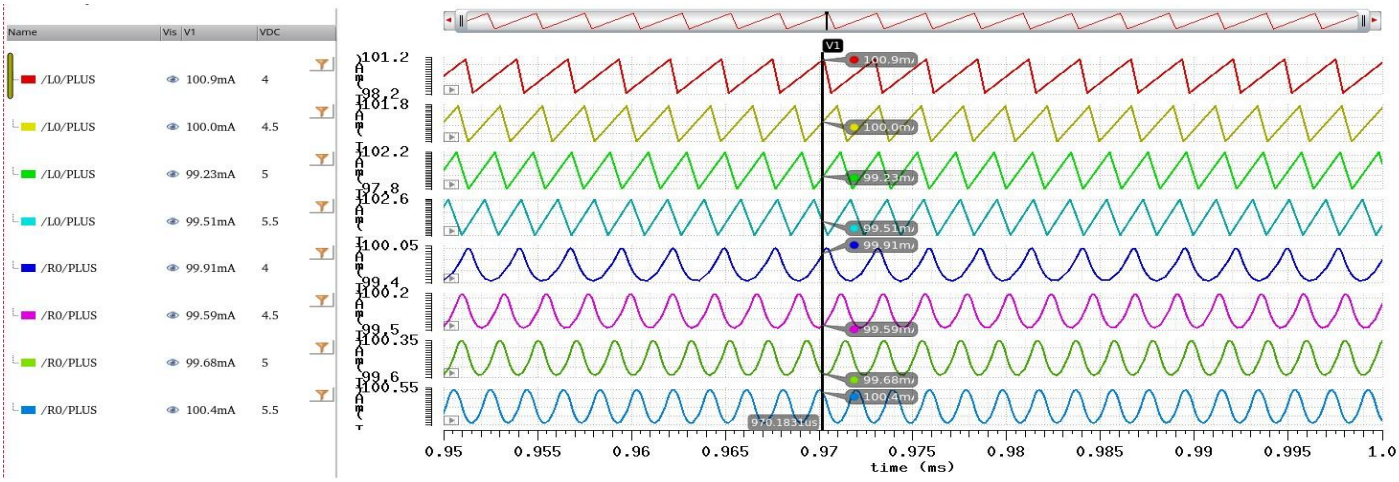

Figure 22: Transient Response of L0/PLUS and V0/PLUS

The figure below shows how the Buck SPS reacts at different temperatures, specifically from 0-100 degrees Celsius. All four main nodes were probed, and the waveforms show that the Buck SPS stops efficiently operating at 71 degrees Celsius and beyond.

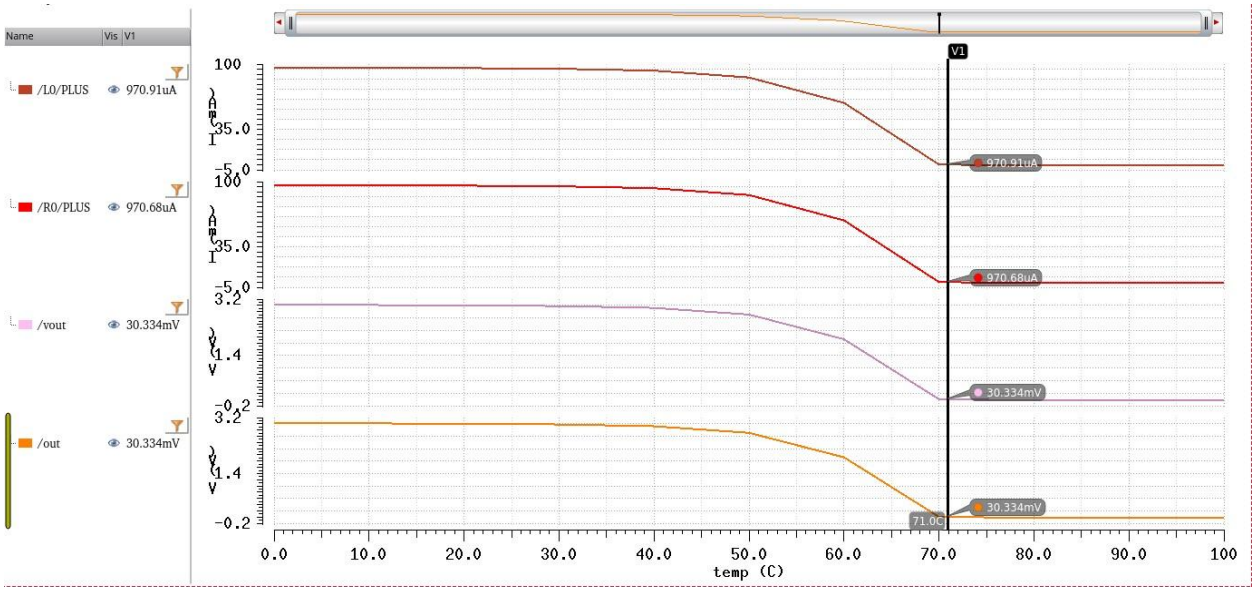

Figure 23: Temperature Sweep from 0-100C for all main nodes

Efficiency:

The most important observation out of all the waveforms is the overall efficiency of the Buck SPS. The five figures below contain multiple characteristics that will depict how efficient the design of the Buck SPS in relation to varying supply voltages as well as varying temperatures. The values indicate the average current supplied by the source from 4-5.5V, for five different temperatures with a range of 0-100C. This spread will efficiently show the different efficiencies over a spectrum of both supply voltages and temperatures. The figure below shows the hand calculations of the efficiency of the Buck SPS, and why we need to use the calculator in Cadence in order to find the average current supplied due to its large variations in its waveforms.

$$\text{Efficiency} = \frac{P_L}{P_s} = \frac{V_{out} \cdot \text{avg}(I_{load})}{V_s \cdot \text{avg}(I_{source})}$$

$\text{avg}(I_{load}) = 100\text{mA}$, $V_{out} = 3.125\text{V}$ $\Rightarrow P_L = 312.5\text{mW}$

$V_s = 4\text{-}5.5\text{V}$

$\text{avg}(I_{source})$ is based on calculator in Cadence

Figure 24: Hand Calculations of Efficiency for Buck SPS

The figures below show two examples of the calculator being used in order to calculate the average current supplied by the source at five different temperatures and at varying supply voltages at the same time. From here, we created a graph that demonstrates the load current vs efficiency at varying temperatures. However, we see that at 81 degrees Celsius and 100 degrees Celsius, the average current is negligible and invalid, which matches what we verified in Figure 22, which stated that the Buck SPS breaks down past 71 degrees Celsius.

average(leafValue(getData("/V0/PLUS" ?result "tran") "VDC" 5.5))
-68.8E-3
average(leafValue(getData("/V0/PLUS" ?result "tran") "VDC" 5))
-73.8E-3
average(leafValue(getData("/V0/PLUS" ?result "tran") "VDC" 4.5))
-79.54E-3
average(leafValue(getData("/V0/PLUS" ?result "tran") "VDC" 4))
-87.51E-3

Figure 25: Average Current Supplied at 0 degrees Celsius

average(leafValue(getData("/V0/PLUS" ?result "tran") "VDC" 5.5))
-1.171E-3
average(leafValue(getData("/V0/PLUS" ?result "tran") "VDC" 5))
-912.5E-6
average(leafValue(getData("/V0/PLUS" ?result "tran") "VDC" 4.5))
-695.9E-6
average(leafValue(getData("/V0/PLUS" ?result "tran") "VDC" 4))
-515.0E-6

Figure 26: Average Current Supplied at 100 degrees Celsius

With those calculations, we are able to plot a line graph that compares the load current versus the efficiency from a temperature sweep of 0-100C and a supply voltage sweep of 4-5.5V. The efficiencies at temperatures greater than 70 degrees Celsius are left zero for easier accessibility of the graph shown below. Based on the table, we can approximate that from 4-5.5V, our efficiencies range from a minimum of 82.58 to a maximum of 89.27%. Increasing the supply voltage caused a slight decrease in efficiency, and minimal variations of the efficiencies between 0-54C.

Power Supplied by Load (mW)	VDD (V)	Temp. (Celsius)	Average Load Current (mA)	Efficiency at 0C (%)	Efficiency at 27C (%)	Efficiency at 54C (%)	Efficiency at 81C (%)	Efficiency at 100C (%)
312.5	4	0	87.51	89.27551137	88.45674819	88.70784603	0	0
	4.5		79.54	87.30757411	86.18074515	86.55670503	0	0
	5		73.8	84.68834688	84.16374899	84.41383036	0	0
	5.5		68.8	82.5845666	82.63260881	82.90993991	0	0
	4	27	88.32					
	4.5		80.58					
	5		74.26					
	5.5		68.76					
	4	54	88.07					
	4.5		80.23					
	5		74.04					
	5.5		68.53					
	4	81	0.552					
	4.5		0.746					
	5		0.979					
	5.5		1.26					
	4	100	0.515					
	4.5		0.695					
	5		0.912					
	5.5		1.171					

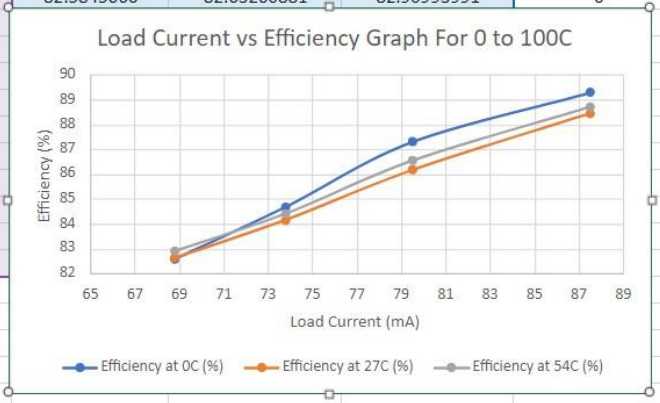

Figure 27: Table + Line Graph of Average Supplied Current vs Efficiency from 0-100C

Conclusions:

Overall, there are many improvements that could be made in the future in order to improve the efficiency of the overall design, such as adding more buffers at the end of the comparator, increasing the widths of the NMOS-NMOS switching transistors, and increasing the size of the off-chip inductor. Although they do increase the efficiency, the quality of the Buck SPS would decline in terms of size for the layout, as well as having unreasonable sizes that would not make sense if the chip were to be fabricated in reality. The final layout of the overall design can also be improved on if given more time, so that the power and ground rails would be laid at the highest and lowest points for the entire layout, rather than just the majority due to the size of the bandgap, and the size of the hi-res resistors. This project as a whole has provided a lot of great insight into chip design with the use of Cadence Virtuoso.