Evan Ruttenberg

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OBJECTIVE

To apply knowledge of computer engineering principles and gain valuable experience through co-op employment

EDUCATION

ROCHESTER INSTITUTE OF TECHNOLOGY, Rochester, NY
Bachelor/Master of Science in Computer Engineering, expected May 2024
GPA: 3.79/4.00
Awards: Dean's List Fall 2019 and 2020; RIT Founder's Merit Scholarship; 2019 National Merit Scholarship semi-finalist; AP + PLTW Student Achievement in Engineering
Courses:

Computer Organization	Applied Programming in C
Digital System Design I & II with Lab	Reconfigurable Computing
Intro to Microelectronic Fabrication	HW/SW Co-Design for Cryptographic Applications
Real Time and Embedded Systems	Multiple Processor Systems
Wines of the World I	Kinetic Glass Practice

SKILLS

Programming Languages: Python, VHDL, C, Verilog
Operating Systems: Linux, Windows, Mac OS X, Android
Software: Altera Quartus, ModelSim, Keil uVision, JetBrains IDE, Autodesk Inventor, Zoom, Xilinx Vivado, Microsoft Office, Arduino IDE, Git
Hardware: Oscilloscope, Digital Multimeter, Waveform Generator, Breadboard circuits

PROJECTS/LABS

- **Digital System Design II Lab**: Designed and verified a MIPS processor in VHDL using Xilinx Vivado
- **Open-Source Contributions**: Contributed Java code and Android UI XML to the open-source MTG Familiar Android app. Functionality was added to allow parsing Magic: The Gathering cards using regex. Full properties for the cards were retrieved from a SQL database and used to display metrics.
- **Senior Design Project**: Working on designing an autonomous chess board that can move pieces without user interaction.
- **PNNL Co-op:** Worked on using the MLIR framework, CIRCT, TensorFlow and Jax to compile Python code into Verilog
- **Hobby Projects**: Programmed the FRDM-K32L3A6 development board to collect microphone data using mixed C and ARM Assembly Language, 3D printing, FPGA development

EMPLOYMENT

Pacific Northwest National Laboratory Remote – Buffalo, NY July – September 2021
Worked on establishing a pipeline for compiling Python code into Verilog

Annapolis Microsystems Annapolis, MD January – May 2022
Expanded coverage of digital logic synthesis and simulation testing program

Pacific Northwest National Laboratory Remote – Buffalo, NY May – August 2022, 2023
Worked on the COMET compiler, focusing on end-to-end compilation from a DSL through execution on heterogeneous compute including FPGA, GPU, and CPU

ACTIVITIES / INTERESTS

Magic: The Gathering, High Level Synthesis