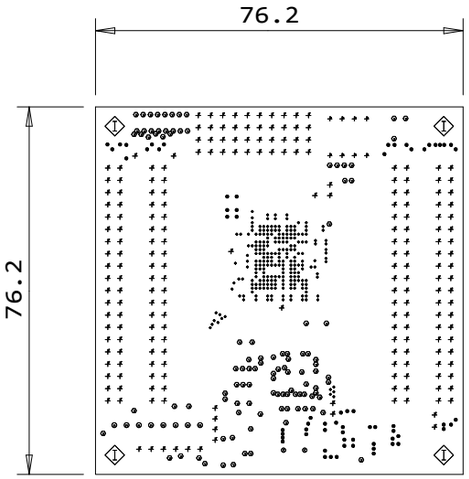
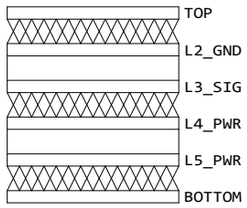


DRILL CHART: TOP to BOTTOM			
ALL UNITS ARE IN MILLIMETERS			
FIGURE	SIZE	PLATED	QTY
·	0.2	PLATED	237
○	0.25	PLATED	105
·	0.3	PLATED	66
+	0.9	PLATED	8
+	1.0	PLATED	221
◎	1.016	PLATED	8
○	0.9	NON-PLATED	2
◇	3.25	NON-PLATED	4



Stackup			Single-ended impedance		Differential impedance		
Layer name:	thickness (mm)	material	Trace Width (mm)	Impedance (Ohms)	Trace Width (mm)	Design Space(mm)	Impedance (Ohms)
TOP	0.5oz+plating	copper			0.17	0.11	90+/-10%
					0.12	0.12	100+/-10%
prepreg	0.194	2x2113					
L2_GND	1oz	copper					
core	0.4						
L3_SIG	1oz	copper					
prepreg	0.198	2113+2116					
L4_PWR	1oz	copper					
core	0.4						
L5_PWR	1oz	copper					
prepreg	0.194	2x2113					
BOTTOM	0.5oz+plating	copper					

TECHNICAL SPECIFICATION:

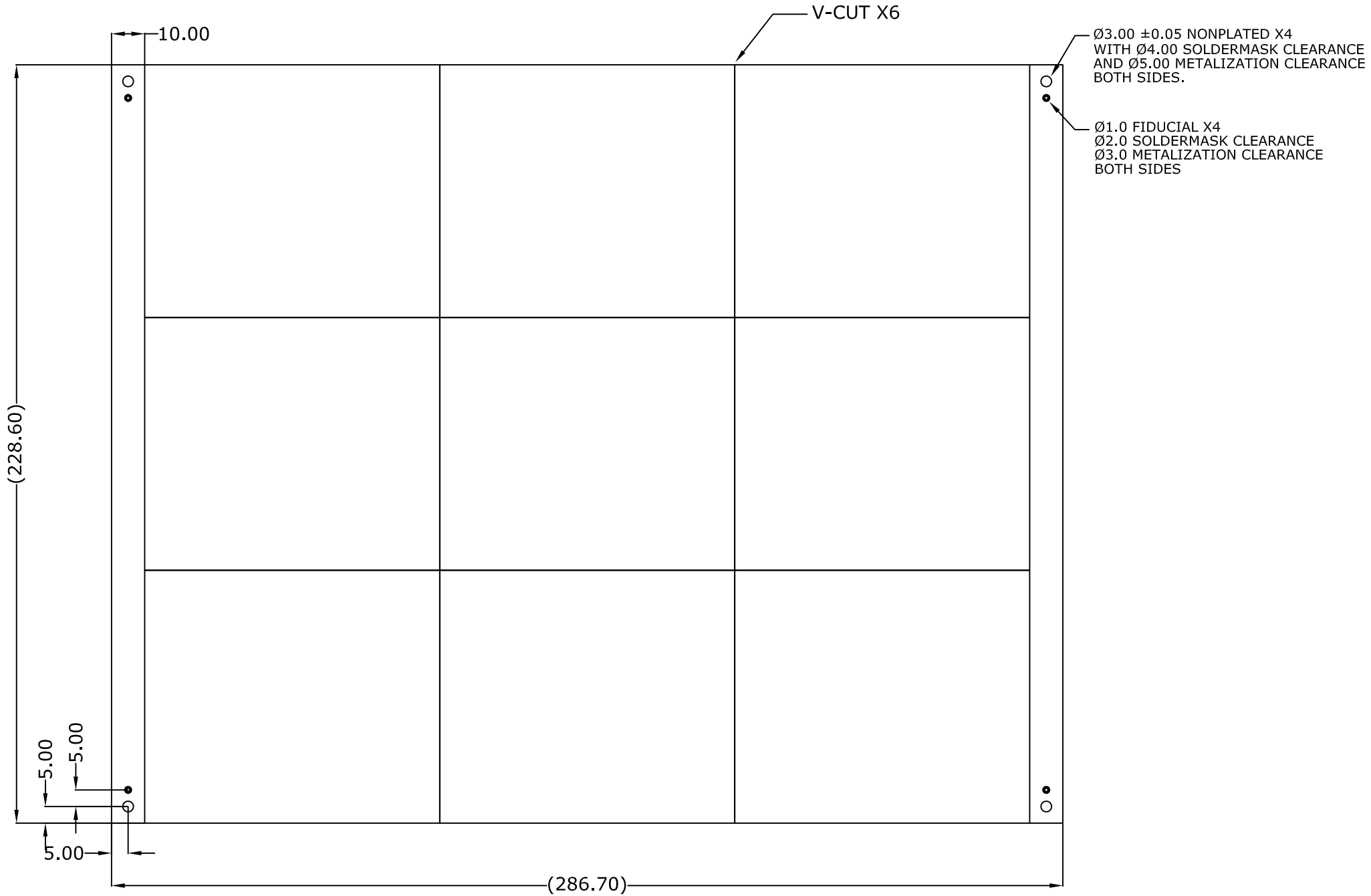
1. No. of layers: 6
2. Finished board size: 76.2mm x 76.2mm
3. Base material: Generic FR-4, glass epoxy material must conform to UL94V-0.
4. Finished board thickness & tolerance: 1.6 mm +/-10%
5. Bow&twist: <=0.7%
6. All hole sizes are specified after plating and marked.
   Thickness in hole wall: 20um (min)
7. Apply white, non-conductive silkscreen legend to top and bottom sides
   of the board. No ink is allowd in holes and on pads.
8. The layer order is as shown in the figure.
9. Add teardrops to all inner layer positive pads on holes as needed.
10. Fabricate board per IPC-6012A.
11. Surface finish:Both HASL and ENIG are OK, the cheaper option is preferred.
12. Green soldermask on top and bottom sides of board, LPI applied over bare copper.
    No soldermask is allowed on solder pad. Must conform to IPC-SM-840.
13. PCB vendor must print date, ID code, UL rating on bottom silkscreen layer
    of boards.
14. Test short/open against IPC-D-356A netlist provided by Axelsys.
15. Fabricate PCB using the Gerber data provided. If any Gerber edits are
    performed. A copy of the edited data must be provided to Axelsys no later
    than 24 hours after fabrication release.
16. Vendor strictly dispose according to customer's original Gerber file,
    without any modifications. If any, immediately inform customer for confirmation.
17. Plug all the 0.2mm vias with epoxy from both sides in the BGA area.
18. Refer to next page for the panelization.

PCB tolerance specification:

UNIT:mm

Outline dimension tolerance		L<=100	+/-0.20
		100<L<=300	+/-0.25
		L>300	+/-0.30
Hole diameter tolerance	PTH/NPTH	D=0.1-0.8	+/-0.08
		D=0.81-1.6	+/-0.10
		D=1.61-5.0	+/-0.15
		Position tolerance	+/-0.076
Slot	PTH	L>2W+0.15	(+/-0.08)X(+/-0.08)
		L<2W+0.15	(+/-0.10)X(+/-0.10)
	NPTH	L>2W+0.05	(+/-0.05)X(+/-0.05)
		L<2W+0.05	(+/-0.08)X(+/-0.08)
		NC routing	(+/-0.13)X(+/-0.13)

	FAB DRAWING	aXelsys
	DESIGNER:L.WANG	PROJECT NAME MACHXO3 STARTER KIT
	CHECKER:L.WANG	
	DATE:23SEP14	SIZE C FAB NUMBER LSCC15001
		SHEET 1/1 REV A



PRIMARY SIDE VIEW