**Microprocessador (processador- CPU)**

Executar cálculos e tomar decisões

Sistema binário

Entrada -> processamento-> saida

ULA (unidade de lógica e aritmética)

Pontos flutuantes

32, 64, 128 bits

Maior o aquecimento

Frequencia de operação, clock

relógio -> Hertz

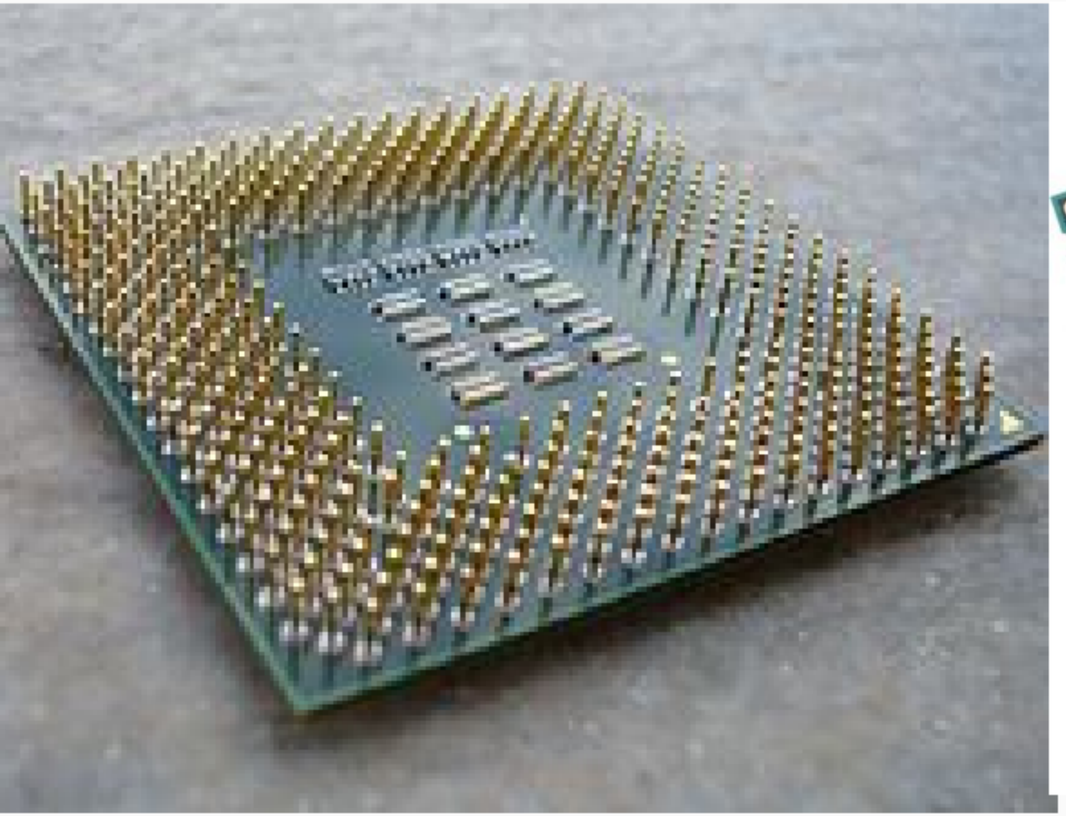
1.8 GHertz

Registradores

Apontador de instrução -> endereço da próxima execução

Registrador da instrução -> possui as instruções que serão executadas

Apontador de Pilha -> endereço da pilha de execução do programa




CISC

RISC

O que analisar?

arquitetura de pontos flutuantes

Clock

Modelo de computação

## Microcontrolador

"um pequeno computador" (SoC) Sistema em um chip

núcleo de processamento, memórias, I/O (E/S)

**sleep ou wait**

Circuito integrado (IC)

Circuito integrado de aplicação específica (ASIC)

SILICON LABS

NXP

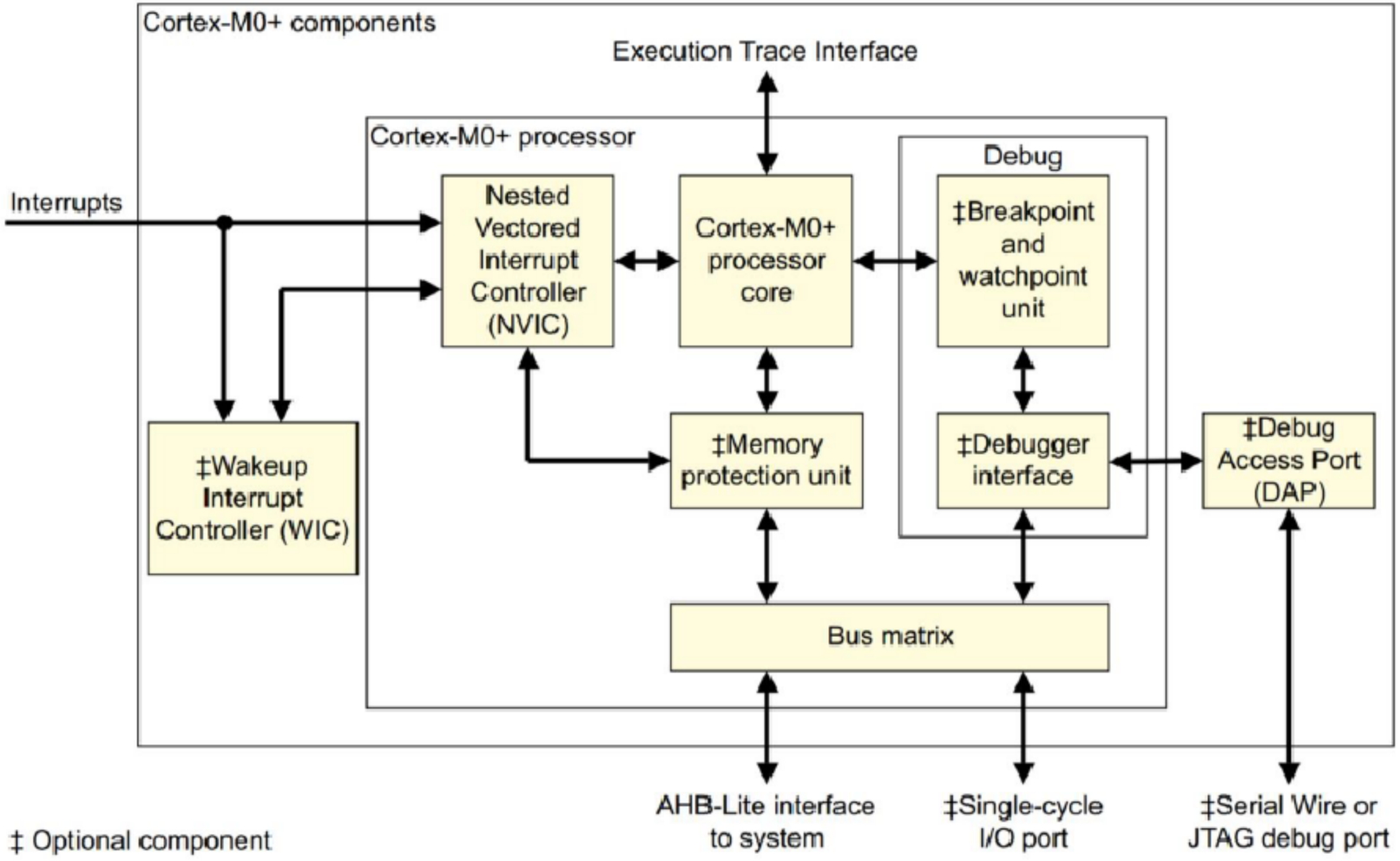
Atmel

TEXAS INSTRUMENTS


MSP432p401r ARM Cortex-M4 ASIC[2]

# ARM Cortex-M0+ is Inside the NXP MKL25Z Chip


MKL25Z128 Integrated Circuit[1]



Features mais importantes

arquitetura de processamento

Tamanho da palavra 32, 64, 128

Número de registradores

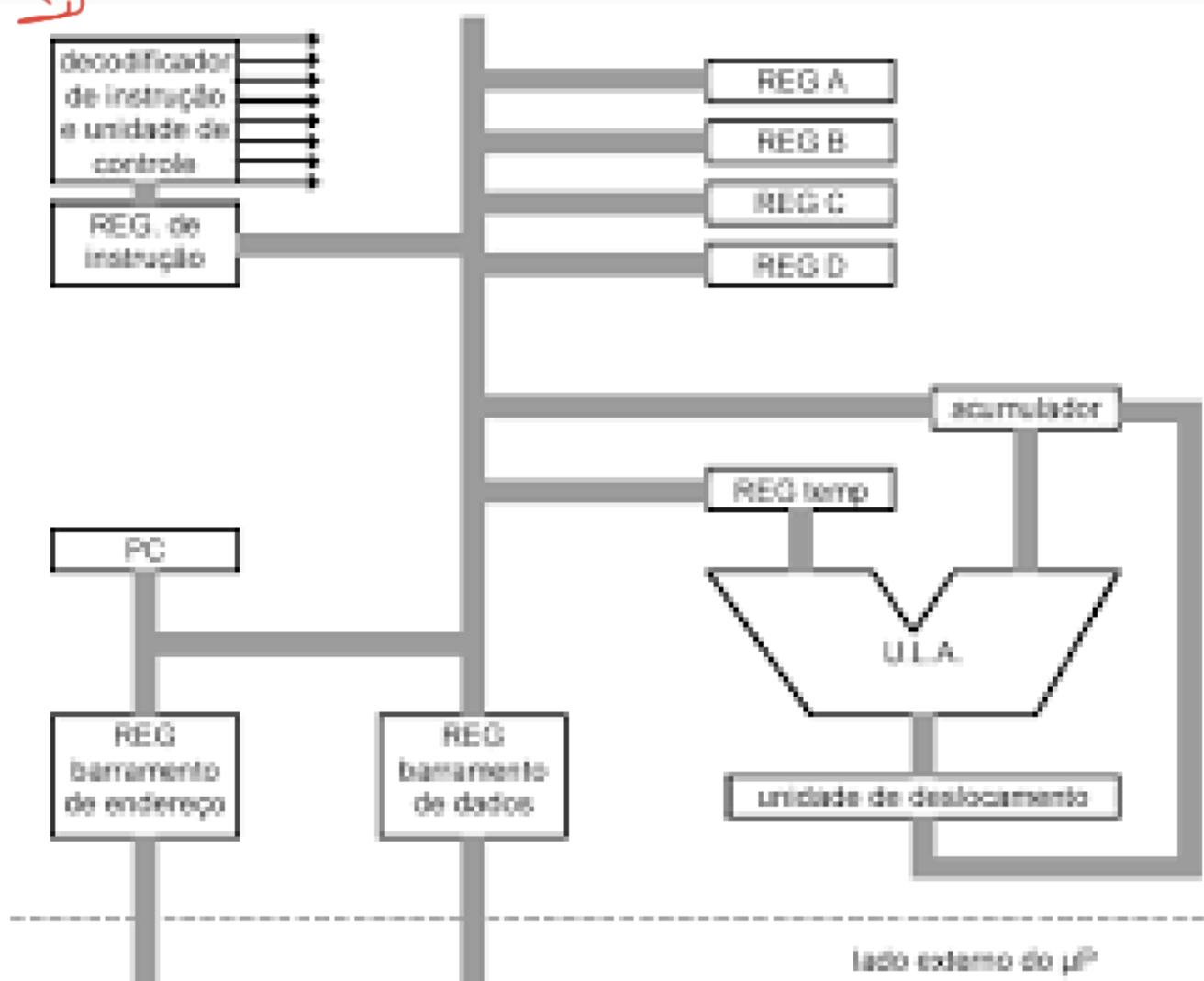
Tamanhos de Flash/RAM

Suporte de previsão de ramificação

Quais as intruções aritiméticas que ele opera

suporte a cache de dados

ponto fluturante aritmético



Quanta memória eu vou precisar para a minha aplicação?

O quão rápido a aplicação precisa rodar?

Que tipo de suporte matemático eu preciso?

# Selector guide | guide compare

| Sub-Family | Part Number | CPU (MHz) | Memory | | Features | | | | | | | | | | | | | | | | √ Package | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Flash (KB) | SRAM (KB) | DMA | Low-Power UART | UART | ISO7 816-3 | SPI | I²C | TSI | I²S | Flex IO | RTC | 12-bit DAC | 16-bit ADC w/DP Ch. | 12-bit ADC | Total I/Os | Other | FM 32 QFN (5 x 5, 0.5 mm) | FT 48 QFN (7 x 7, 0.5 mm) | DA 36X FBGA (3.5 x 3.5, 0.5 mm) | LH 64 LQFP (10 x 10, 0.5 mm) | LK 80 LQFP (12 x 12, 0.5 mm) | LL 100 LQFP (14 x 14, 0.5 mm) | MP 64 MAPBGA (5 x 5, 0.5 mm) | MC 121 MAPBGA (8 x 8, 0.65 mm) |
| KL24 | MKL24Z32xxx4 | 48 MHz | 32 | 4 | √ | 1 | 2 | | 2 | 2 | | | | √ | | | √ | 23~66 | USB 2.0 FS OTG/ Host/Device | √ | √ | √ | √ | | | | |
| | MKL24Z64xxx4 | 48 MHz | 64 | 8 | √ | 1 | 2 | | 2 | 2 | | | | √ | | | √ | 23~66 | USB 2.0 FS OTG/ Host/Device | √ | √ | √ | √ | | | | |
| KL25 | MKL25Z32xxx4 | 48 MHz | 32 | 4 | √ | 1 | 2 | | 2 | 2 | √ | | | √ | √ | √ | | 23~66 | USB 2.0 FS OTG/ Host/Device | √ | √ | √ | √ | | | | |
| | MKL25Z64xxx4 | 48 MHz | 64 | 8 | √ | 1 | 2 | | 2 | 2 | √ | | | √ | √ | √ | | 23~66 | USB 2.0 FS OTG/ Host/Device | √ | √ | √ | √ | | | | |
| | MKL25Z128xxx4 | 48 MHz | 128 | 16 | √ | 1 | 2 | | 2 | 2 | √ | | | √ | √ | √ | | 23~66 | USB 2.0 FS OTG/ Host/Device | √ | √ | √ | √ | | | | |
| | MKL26Z32xxx4 | 48 MHz | 32 | 4 | √ | 1 | 2 | | 2 | 2 | √ | √ | | √ | √ | √ | | 23~50 | USB 2.0 FS OTG/ Host/Device | √ | √ | √ | | | | | |
| | | 48 | | | | | | | | | | | | | | | | | USB 2.0 FS OTG/ | | | | | | | | |

# Manual do usuário


Datasheet

Eletricas

Timing

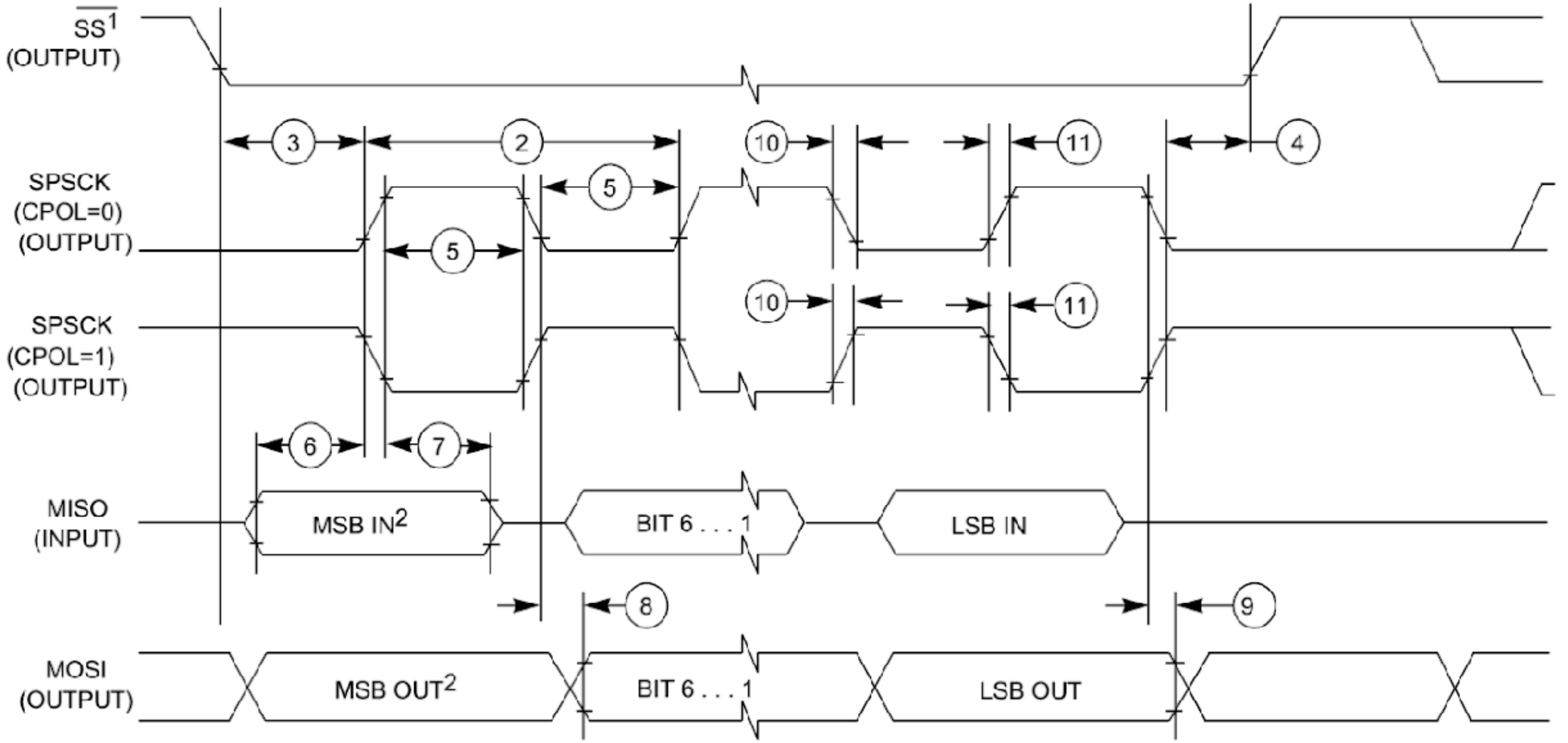
Ambiente de depuração

pacote físico

# 1.4 Voltage and current operating ratings

## Table 4. Voltage and current operating ratings

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{DD}$ | Digital supply voltage | –0.3 | 3.8 | V |
| $I_{DD}$ | Digital supply current | — | 120 | mA |
| $V_{IO}$ | IO pin input voltage | –0.3 | $V_{DD}$ + 0.3 | V |
| $I_D$ | Instantaneous maximum current single pin limit (applies to all port pins) | –25 | 25 | mA |
| $V_{DDA}$ | Analog supply voltage | $V_{DD}$ – 0.3 | $V_{DD}$ + 0.3 | V |
| $V_{USB\_DP}$ | USB_DP input voltage | –0.3 | 3.63 | V |
| $V_{USB\_DM}$ | USB_DM input voltage | –0.3 | 3.63 | V |
| $V_{REGIN}$ | USB regulator input | –0.3 | 6.0 | V |



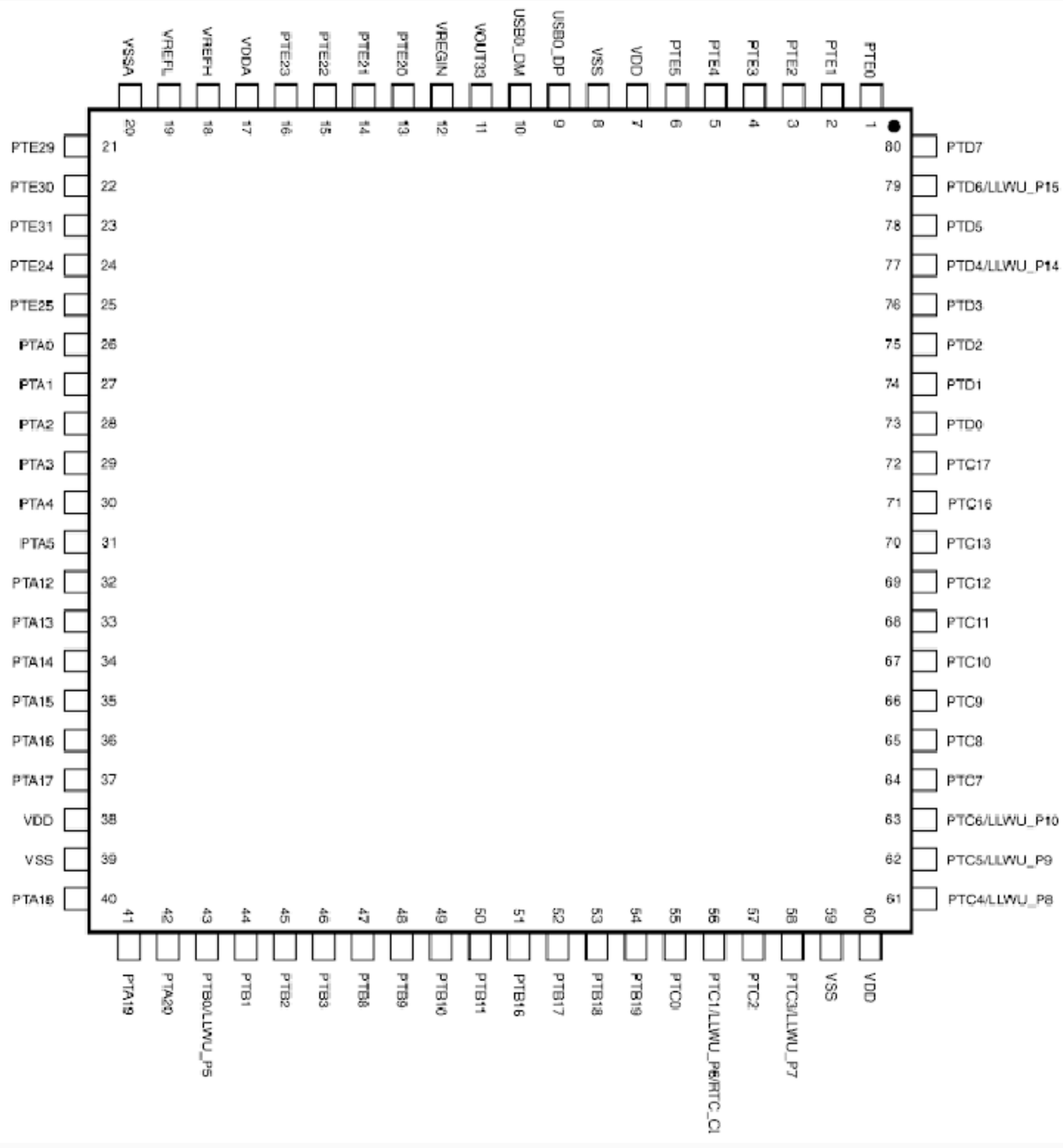

1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

**Figure 14. SPI master mode timing (CPHA = 0)**

## 2.4.1 Thermal operating requirements

**Table 15. Thermal operating requirements**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $T_J$ | Die junction temperature | –40 | 125 | °C |
| $T_A$ | Ambient temperature | –40 | 105 | °C |


PTE29 21
PTE30 22
PTE31 23
PTE24 24
PTE25 25
PTA0 26
PTA1 27
PTA2 28
PTA3 29
PTA4 30
PTA5 31
PTA12 32
PTA13 33
PTA14 34
PTA15 35
PTA16 36
PTA17 37
VDD 38
VSS 39
PTA18 40
PTA19 41
PTA20 42
PTB0/LLWU_P5 43
PTB1 44
PTB2 45
PTB3 46
PTB8 47
PTB9 48
PTB10 49
PTB11 50
PTB16 51
PTB17 52
PTB18 53
PTB19 54
PTC0 55
PTC1/LLWU_P6/RTC_CL 56
PTC2 57
PTC3/LLWU_P7 58
VSS 59
VDD 60
PTC4/LLWU_P8 61
PTC5/LLWU_P9 62
PTC6/LLWU_P10 63
PTC7 64
PTC8 65
PTC9 66
PTC10 67
PTC11 68
PTC12 69
PTC13 70
PTC16 71
PTC17 72
PTD0 73
PTD1 74
PTD2 75
PTD3 76
PTD4/LLWU_P14 77
PTD5 78
PTD6/LLWU_P15 79
PTD7 80
PTE0 1
PTE1 2
PTE2 3
PTE3 4
PTE4 5
PTE5 6
VDD 7
VSS 8
USB0_DP 9
USB0_DM 10
VOUT33 11
VREGIN 12
PTE20 13
PTE21 14
PTE22 15
PTE23 16
VDDA 17
VREFH 18
VREFL 19
VSSA 20

### 11.2.2 Modes of operation

#### 11.2.2.1 Run mode

In Run mode, the PORT operates normally.

#### 11.2.2.2 Wait mode

In Wait mode, PORT continues to operate normally and may be configured to exit the Low-Power mode if an enabled interrupt is detected. DMA requests are still generated during the Wait mode, but do not cause an exit from the Low-Power mode.

#### 11.2.2.3 Stop mode

In Stop mode, the PORT can be configured to exit the Low-Power mode via an asynchronous wakeup signal if an enabled interrupt is detected.

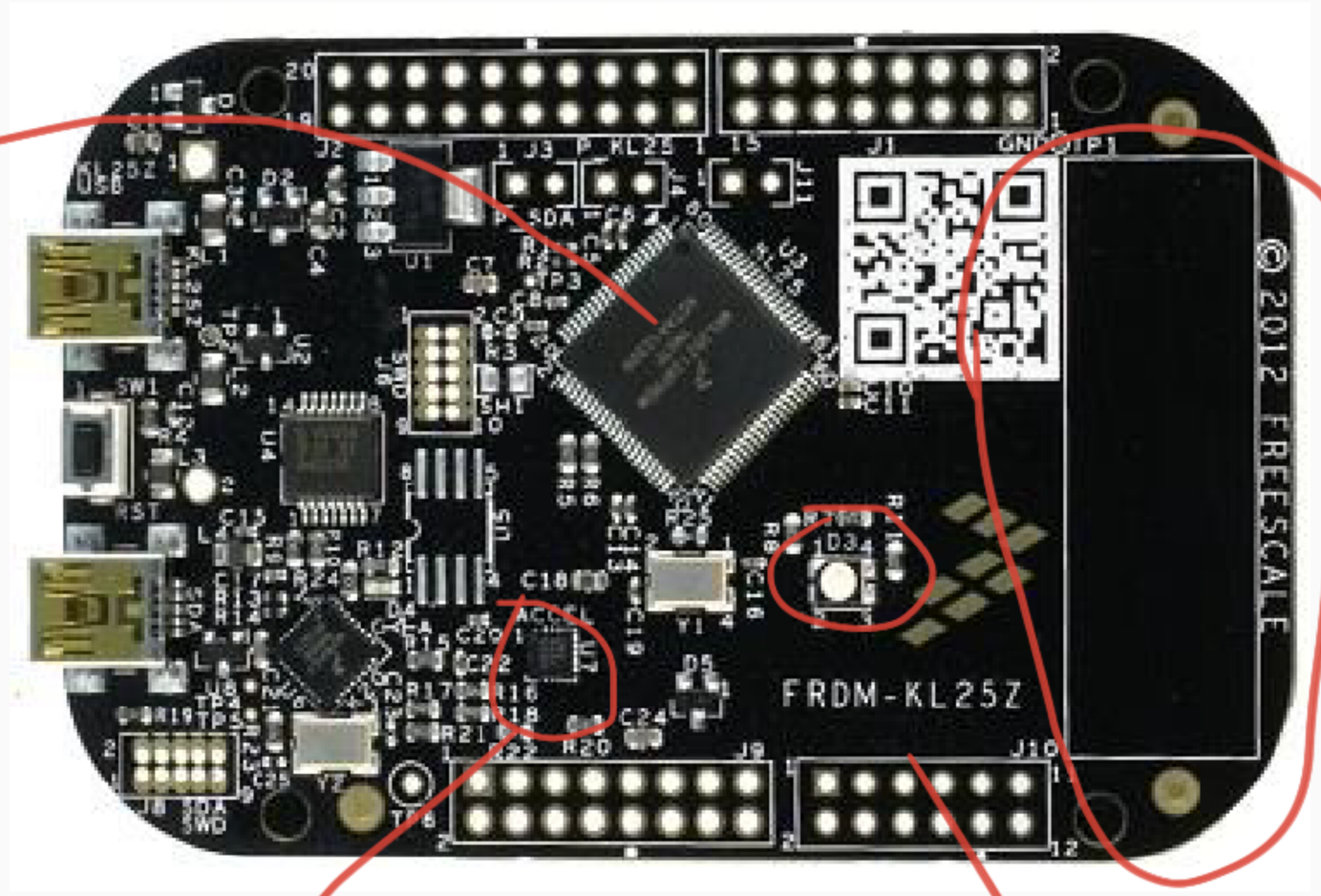
#### 11.2.2.4 Debug mode

In Debug mode, PORT operates normally.

# CHIP ERRATA

| Errata ID | Errata Title |
|---|---|
| 3863 | ADC: In 16-bit differential mode, ADC may result in a conversion error when positive input is near upper rail reference voltage |
| 5751 | FTFx: Launching the Read 1's Section command (RD1SEC) on an entire flash block results in access error (ACCER). |
| 6070 | I2C: Repeat start cannot be generated if the I2Cx_F[MULT] field is set to a non-zero value |
| 5746 | PIT: When using the PIT to trigger DMA transfers using cycle steal mode, two data transfers per request are generated |
| 5666 | PMC: Maximum current consumption in VLPR, VLPW, VLPS, LLS and VLLS modes may be higher than data sheet specification. |
| 5667 | PMC: When used as an input to ADC or CMP modules, the PMC bandgap 1-V voltage reference is not available in VLPx, LLS, or VLLSx modes |
| 5472 | SMC: Mode transition VLPR->VLLS0(POR disabled)->RUN, will cause POR & LVD. |
| 5745 | SPI1: Back to back DMA data transfers are not possible if the core:bus frequency ratio is greater than 4:1 |
| 5490 | SPI1: DMA data transfers at the maximum baud rate can result in corrupted data |
| 5515 | TSI: The end of scan flag is not automatically cleared when continuously scanning |
| 5744 | UART0: Receiver wakeup control bit cannot be set immediately after a wakeup event |
| 5563 | UART0: When the Receiver Wake Up control bit is set, an IDLE condition is not detected correctly |
| 5753 | UART1 / UART2: When the Receiver Wake Up control bit is set, an IDLE condition is not detected correctly |
| 5928 | USBOTG: USBx_USBTRC0[USBRESET] bit does not operate as expected in all cases |

# kits de desenvolvimento




Microcontrolador

acelerometro

LED

touchpad

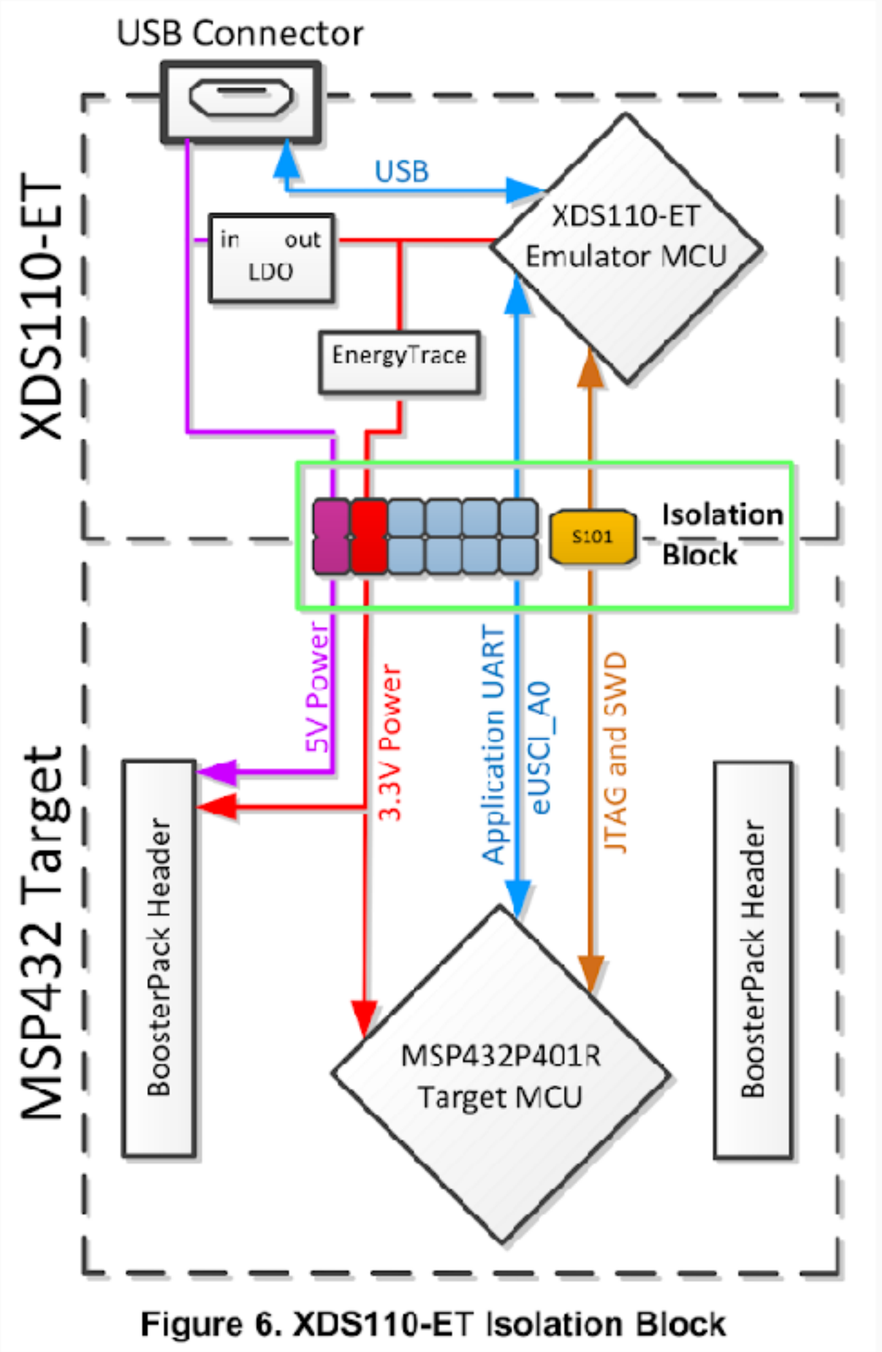



**Figure 6. XDS110-ET Isolation Block**