



# Mestrado em Engenharia Informática

2024/25

*João Luís Sobral*

# Course foundations



- **Lecturing/teaching team**
  - Lectures: João Sobral
  - Lab classes: João Sobral, Rui Silva, João Barbosa, Miguel Braga
- **Documentation & oral lectures/classes**
  - Documentation (slides, lab guides, books, reports...): English, on BB
  - Oral presentations and work defence: optional, but usually Portuguese
- **Expected background**
  - Imperative Programming and Computer Architecture
  - Lab skills in Unix, C programming and debugging
- **Assessment**
  - 1x written test/exam (test 20<sup>th</sup> Dec, exam 24<sup>th</sup> Jan, weight: 30%)
  - 2x intermediate works w/ reports (submission 21<sup>th</sup> Oct & 19<sup>th</sup> Nov, weight: 2x15%)
  - 1x final work w/ report & oral defence (end of 2024 & 6-10 Jan, weight: 40%)

# *Focus on this course: performance engineering*

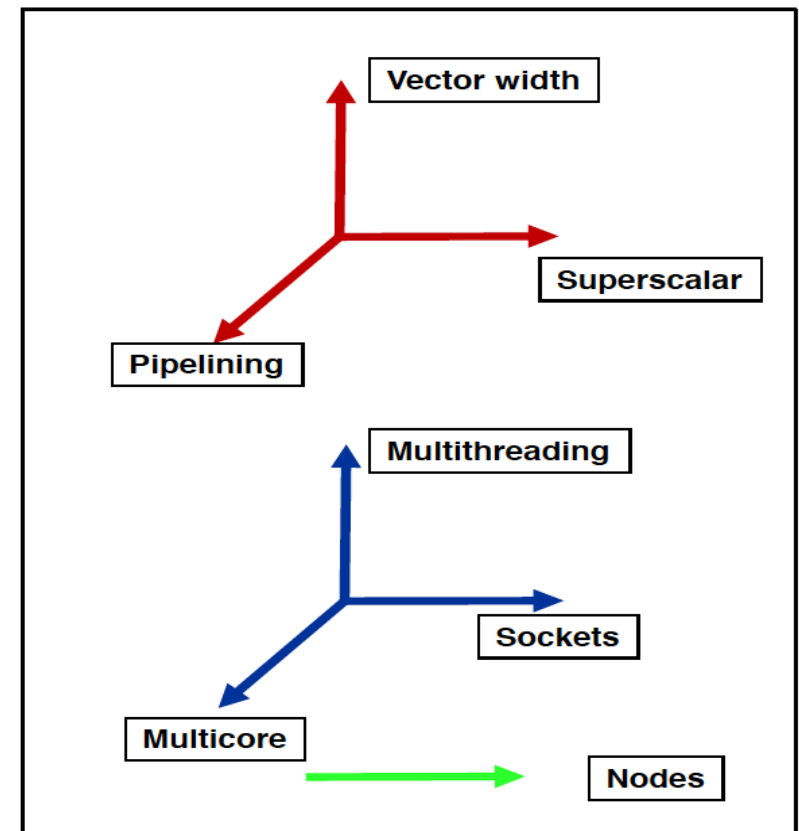


## How:

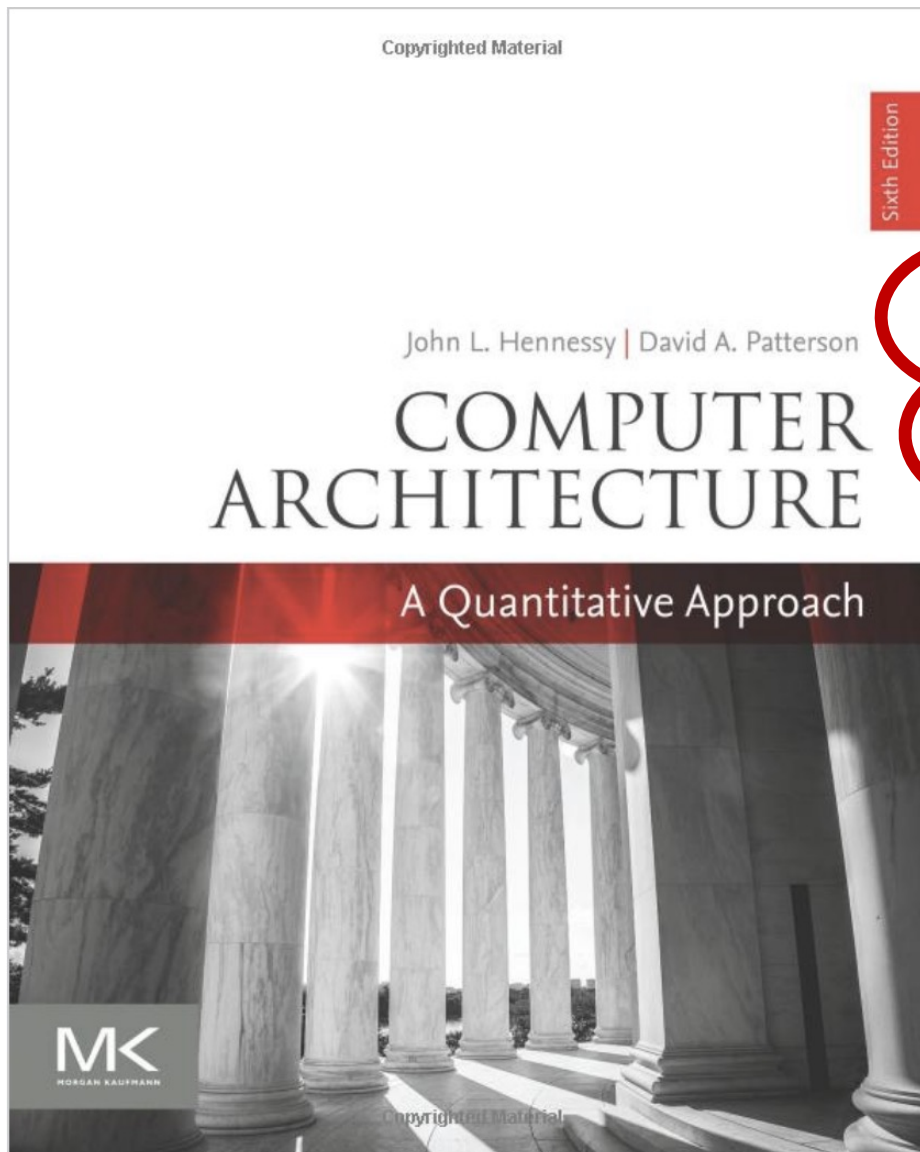
- plan and code efficient algorithms & data structures
- profiling & evaluating (through measurements) the execution efficiency
- understanding the organization of a computer system (its architecture)

## Where in the hardware:

- in sequential code with ILP
  - pipelining
  - superscalar w/ out-of-order exec
  - vector processing
- in a memory hierarchy
  - multi-level caches (+ distributed memory)
- w/ support for thread parallelism
  - multithreading in-core (SMT)
  - multithreading in multicore
- w/ computing accelerators (GPU, ...)
- w/ support for process-based parallelism
  - multiprocessing in a computer cluster



# Key textbook (1)



## Table of Contents

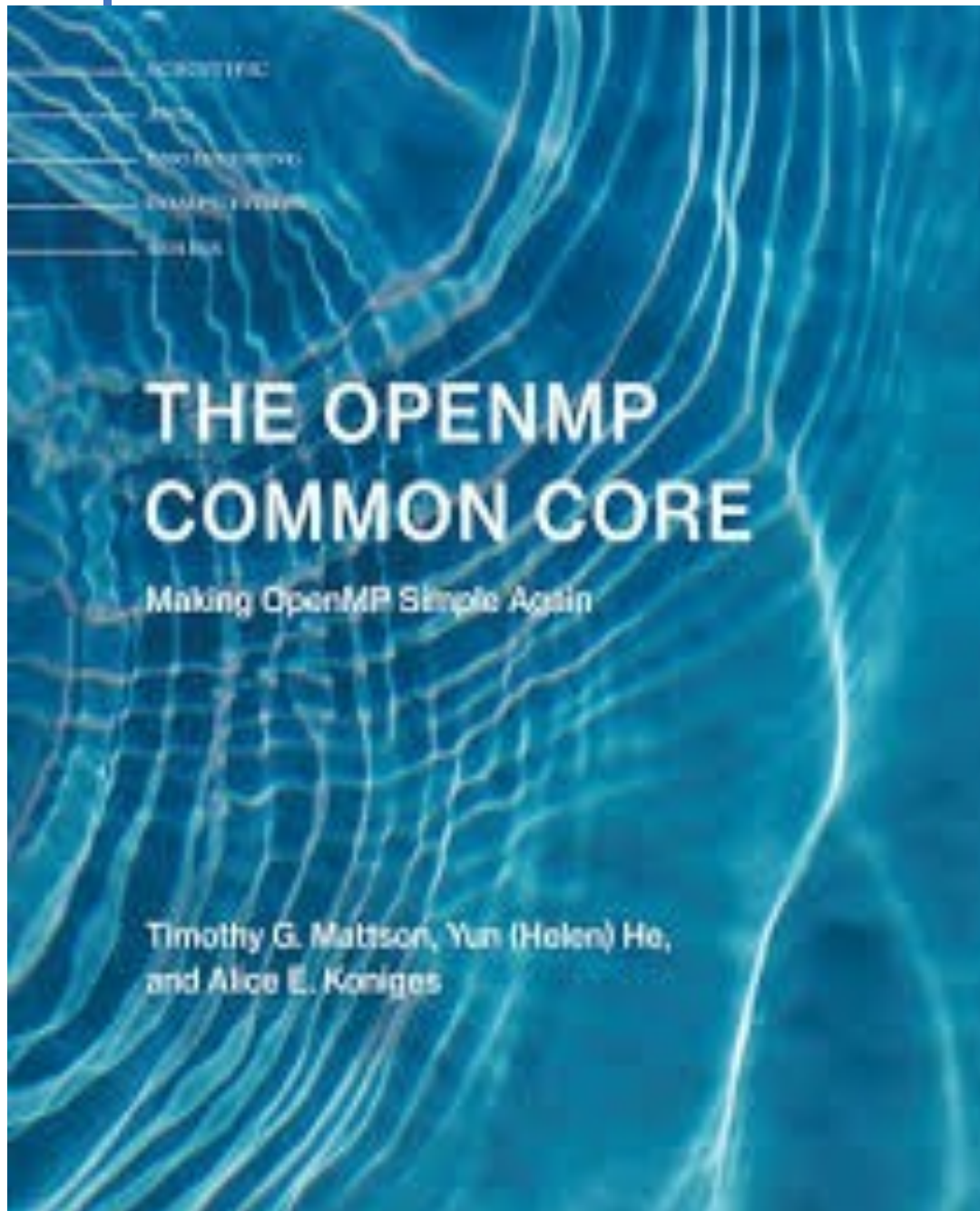
### Printed Text

1. Fundamentals of Quantitative Design and Analysis
2. Memory Hierarchy Design
3. Instruction-Level Parallelism and Its Exploitation
4. Data-Level Parallelism in Vector, SIMD, and GPU Architectures
5. Multiprocessors and Thread-Level Parallelism
6. The Warehouse-Scale Computer
7. Domain Specific Architectures
  - A. Instruction Set Principles
  - B. Review of Memory Hierarchy
  - C. Pipelining: Basic and Intermediate Concepts

### Online

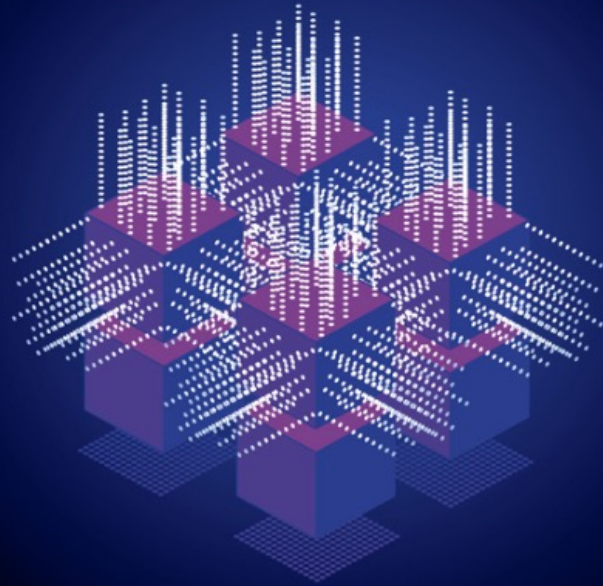
- D. Storage Systems
- E. Embedded Systems
- F. Interconnection Networks
- G. Vector Processors
- H. Hardware and Software for VLIW and EPIC
- I. Large-Scale Multiprocessors and Scientific Applications
- J. Computer Arithmetic
- K. Survey of Instruction Set Architectures
- L. Advanced Concepts on Address Translation
- M. Historical Perspectives and References

## Key textbook (2)



<b>II</b>	<b>The OpenMP Common Core</b>	
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## PARALLEL COMPUTING ARCHITECTURES AND APIs

IoT Big Data Stream Processing

Vivek Kale



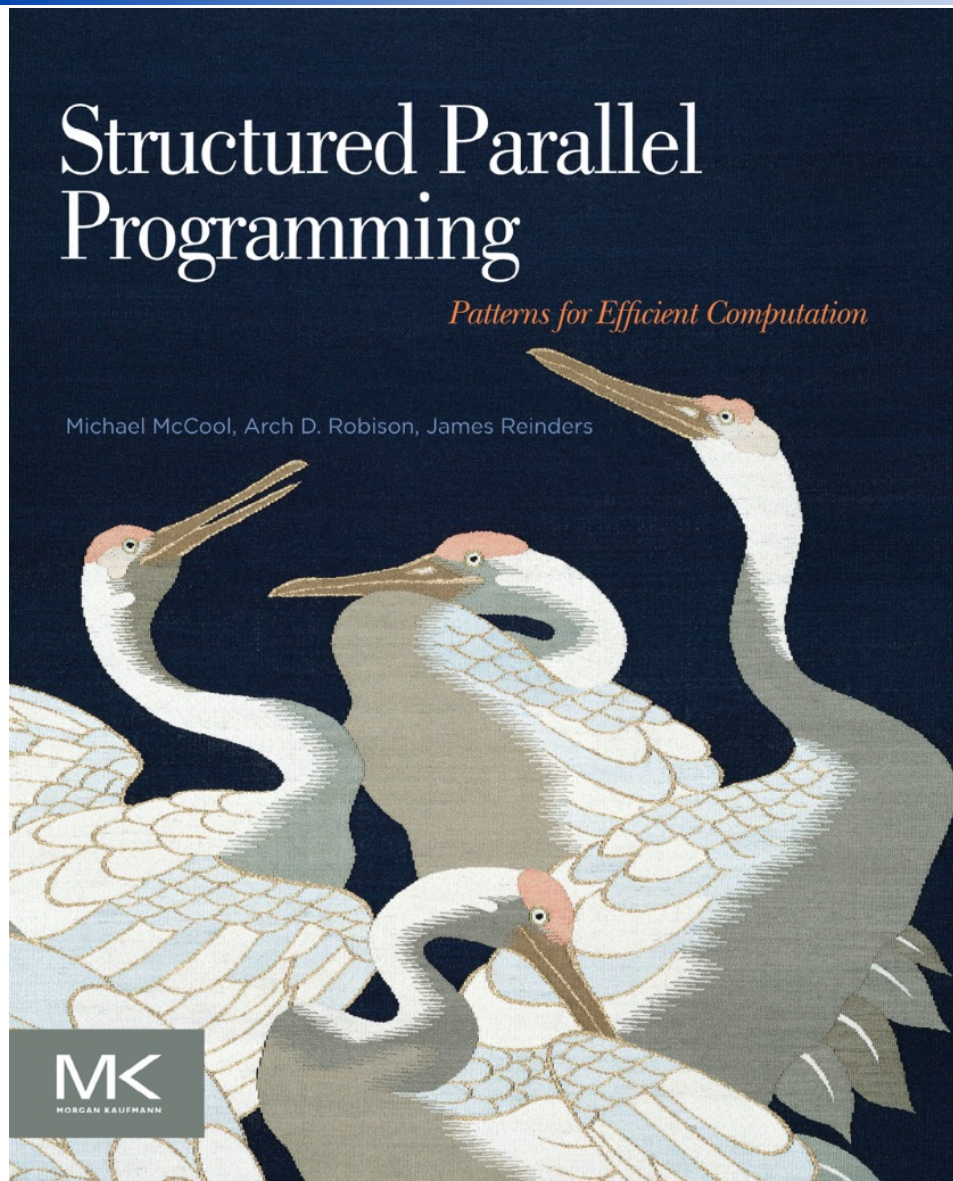
CRC Press  
Taylor & Francis Group

A CHAPMAN & HALL BOOK

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1. Uniprocessor Computers
2. Processor Physics and Moore's Law
- Section I Genesis of Parallel Computing
3. Processor Basics
4. Networking Basics
5. Distributed Systems Basics
- Section II Road to Parallel Computing
6. Parallel Systems
7. Parallel Computing Models
8. Parallel Algorithms
- Section III Parallel Computing Architectures
9. Parallel Computing Architecture Basics
10. Shared Memory Architecture
11. Message-Passing Architecture
12. Stream Processing Architecture
- Section IV Parallel Computing Programming
13. Parallel Computing Programming Basics
14. Shared-memory Parallel Programming with OpenMP
15. Message Passing Parallel Programming with MPI
16. Stream Processing Programming with CUDA, OpenCL, and OpenACC
- Section V Internet of Things Big Data Stream Processing
17. Internet of Things (IoT) Technologies
18. Sensor Data Processing
19. Big Data Computing
20. Big Data Stream Processing
- Epilogue: Quantum Computing

## Key textbook (4)

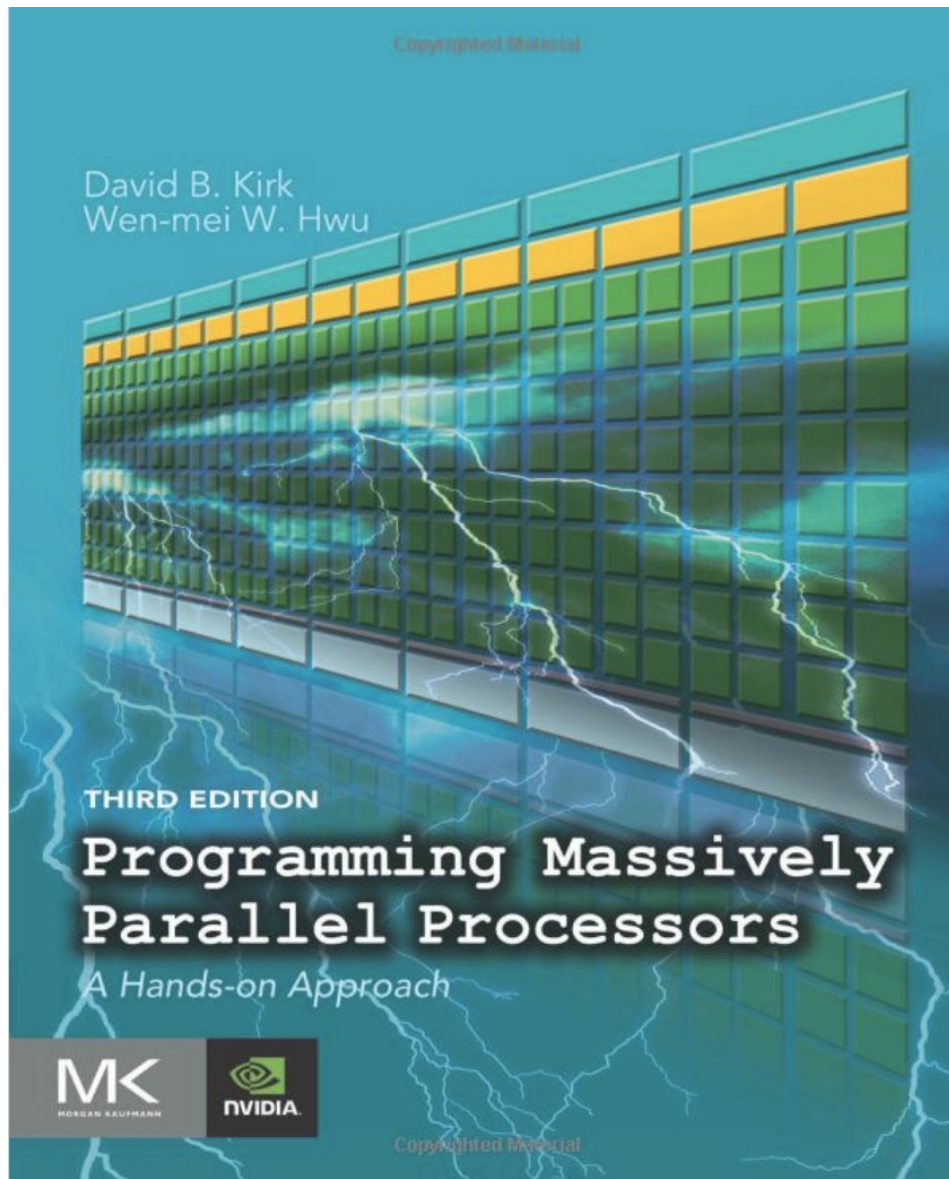


### Table of contents

- 1 - Introduction
- 2 - Background
- 3 - Patterns
- 4 - Map
- 5 - Collectives
- 6 - Data Reorganization
- 7 - Stencil and Recurrence
- 8 - Fork-Join
- 9 - Pipeline
- 10 - Forward Seismic Simulation
- 11 - K-Means Clustering
- 12 - Bzip2 Data Compression
- 13 - Merge Sort
- 14 - Sample Sort
- 15 - Cholesky Factorization
- Appendices



# Recommended textbook (1)



## Contents

## GPU & CUDA

1. Introduction
2. Data parallel computing
3. Scalable parallel execution
4. Memory and data locality
5. Performance considerations
6. Numerical considerations
7. Parallel patterns: Convolution
8. Parallel patterns: Prefix Sum
9. Parallel patterns : Parallel Histogram Computation
10. Parallel patterns: Sparse Matrix Computation
11. Parallel patterns: Merge Sort
12. Parallel patterns: Graph Searches
13. CUDA dynamic parallelism
14. Application case study—non-Cartesian magnetic ...
15. Application case study—molecular visualization ...
16. Application case study—machine learning
17. Parallel programming and computational thinking
18. Programming a heterogeneous computing cluster
19. Parallel programming with OpenACC
20. More on CUDA and graphics processing computing
21. Conclusion and outlook

Appendix A. An introduction to OpenCL

Appendix B. THRUST: a productivity-oriented library for CUDA



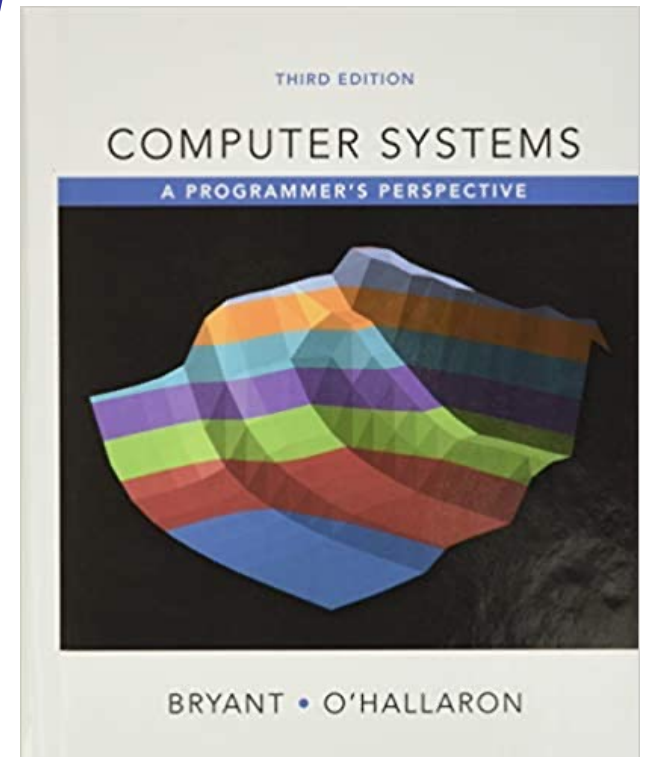
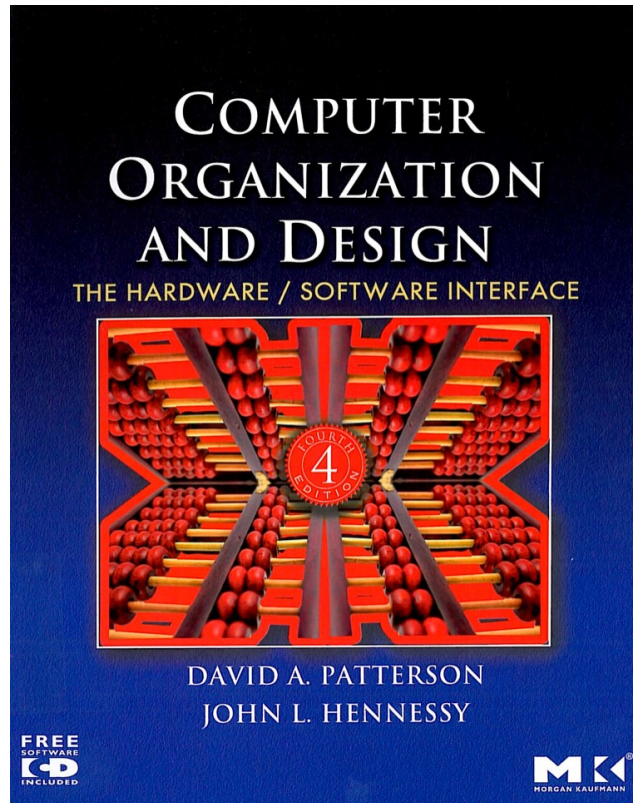
# Background concepts from a basic Computer Systems course



## Some notes/comments for this course:

– some slides are borrowed from

and some from



# A New Golden Age for Computer Architecture

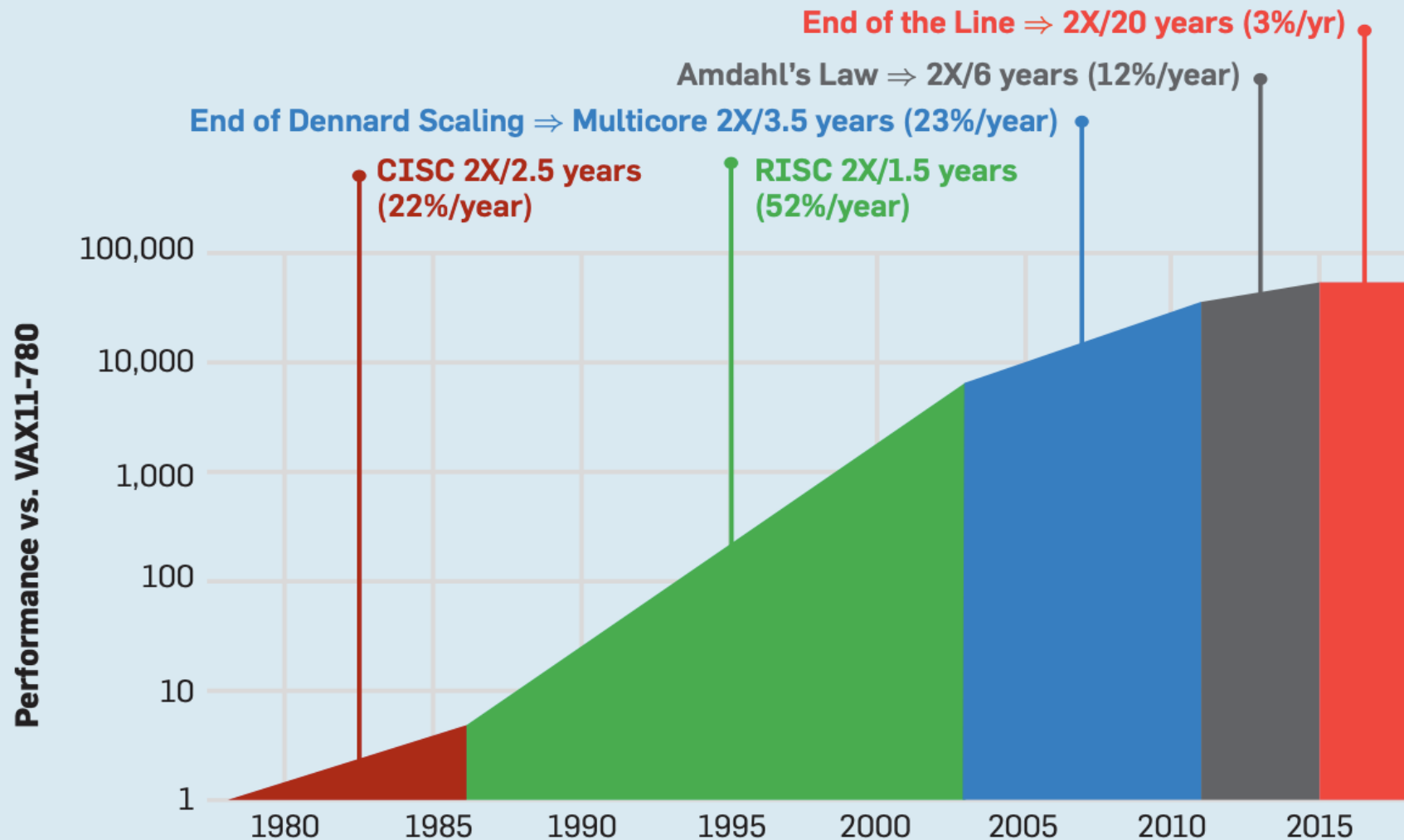
## Growth of computer performance (single-core)



BY JOHN L. HENNESSY AND DAVID A. PATTERSON

COMMUNICATIONS OF THE ACM | FEBRUARY 2019 | VOL. 62 | NO. 2

**Figure 6. Growth of computer performance using integer programs (SPECintCPU).**

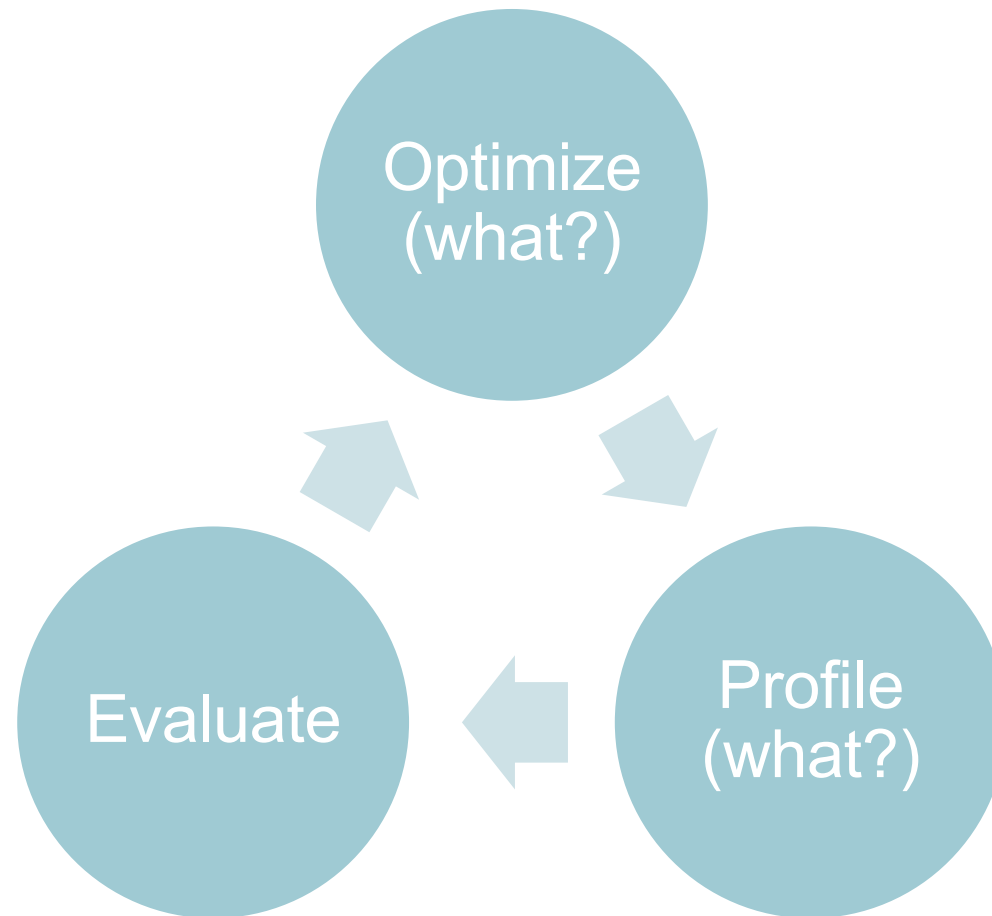


# Current Trends in Architecture

- Cannot continue to leverage Instruction-Level Parallelism (ILP)
  - Single processor performance improvement ended in 2003
- New models for performance:
  - Data-level parallelism (DLP)
  - Thread-level parallelism (TLP)
  - Process-level parallelism
  - Parallelism with accelerators
- These require explicit restructuring of the application

# Performance optimization

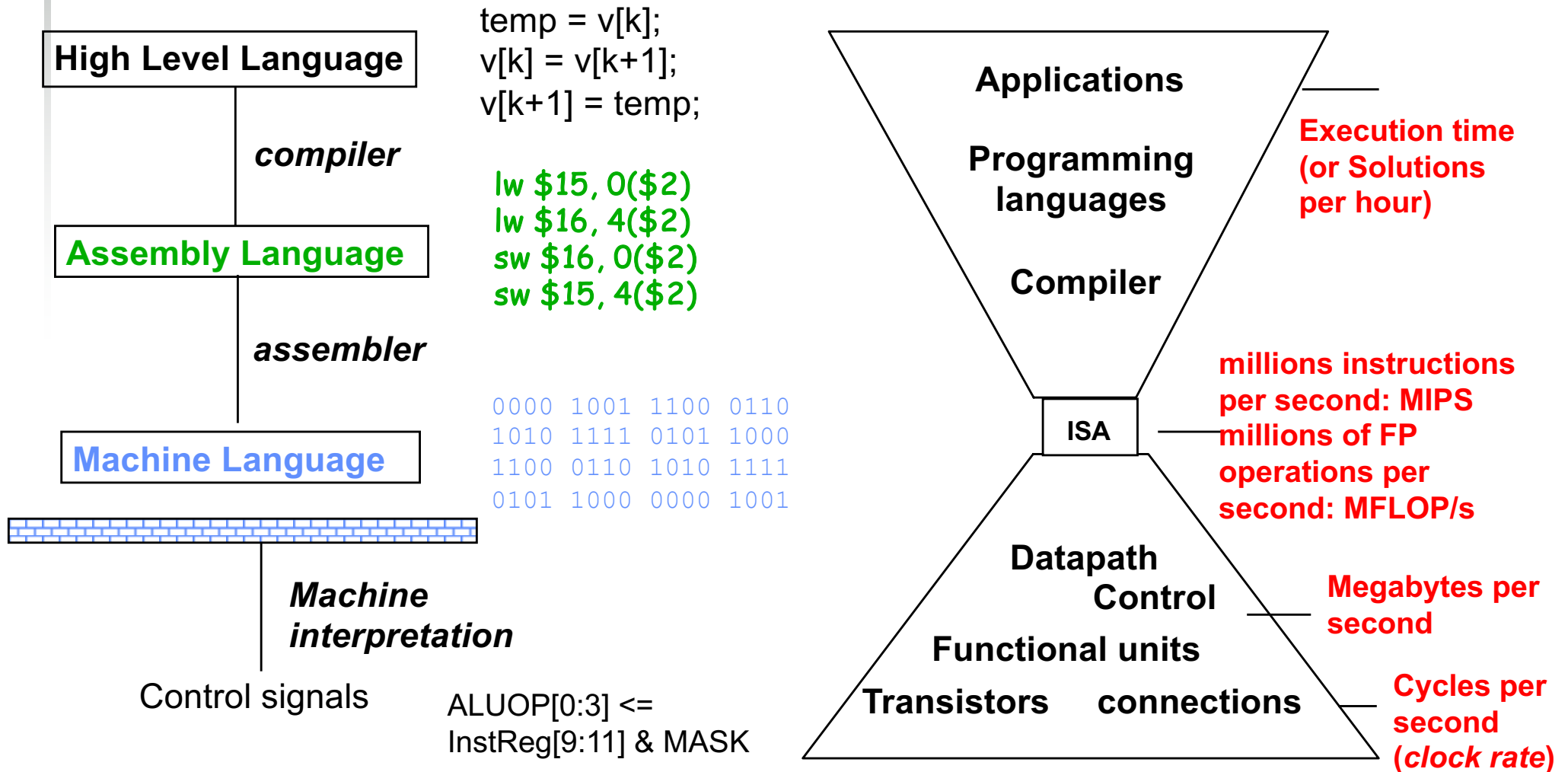
- Typical optimisation cycle





# Performance evaluation

- Can be performed at different levels



# Bandwidth and Latency

- Bandwidth or throughput
  - Total work done in a given time
  - 32,000-40,000x improvement for processors
  - 300-120x improvement for memory and disks
- Latency or response time
  - Time between start and completion of an event
  - 50-90x improvement for processors
  - 6-8x improvement for memory and disks

# Measuring Performance

- Typical performance metrics:
  - Response time
  - Throughput
- Speedup of X relative to Y
  - $\text{Execution time}_Y / \text{Execution time}_X$
- Execution time
  - Wall clock time: includes all system overheads
  - CPU time: only computation time
- Benchmarks
  - Kernels (e.g. matrix multiply)
  - Toy programs (e.g. sorting)
  - Synthetic benchmarks (e.g. Dhrystone)
  - Benchmark suites (e.g. SPEC06fp, TPC-C)

# Principles of Computer Design

## ■ The Processor Performance Equation

*CPU time = CPU clock cycles for a program × Clock cycle time*

$$\text{CPU time} = \frac{\text{CPU clock cycles for a program}}{\text{Clock rate}}$$

$$\text{CPI} = \frac{\text{CPU clock cycles for a program}}{\text{Instruction count}}$$

*CPU time = Instruction count × Cycles per instruction × Clock cycle time*

$$\frac{\text{Instructions}}{\text{Program}} \times \frac{\text{Clock cycles}}{\text{Instruction}} \times \frac{\text{Seconds}}{\text{Clock cycle}} = \frac{\text{Seconds}}{\text{Program}} = \text{CPU time}$$



# Measuring the CPU Time (single-core): an example

Consider the following piece of executable x86 code:

```
    movl 10, %eax
    movl 0, %ecx
loop:
    addl %eax, %ecx
    decl %eax
    jnz loop
```

Estimate its execution time in a computer system with a 2 GHz clock frequency and a CPI=1.5.

$$\text{CPU}_{\text{time}} = \# \text{Instr} * \text{CPI} * \text{Clk}_{\text{cycle}}$$

$$\text{PU}_{\text{time}} = 32 * 1.5 * 1/(2 * 10^{-9}) \text{ sec} = 24 * 10^{-9} \text{ s} = \mathbf{24 \text{ ns}}$$

# Lei de Amdahl



## O ganho no desempenho – *speedup* –

obtido com a melhoria do tempo de execução de uma parte do sistema, está limitado pela fração de tempo dessa parte.

$$\text{Speedup}_{\text{overall}} = \frac{\text{Tempo\_exec}_{\text{antigo}}}{\text{Tempo\_exec}_{\text{novo}}} = \frac{1}{f / s}$$

**f** - fração com melhoria **s**

**s** - *speedup* da fração

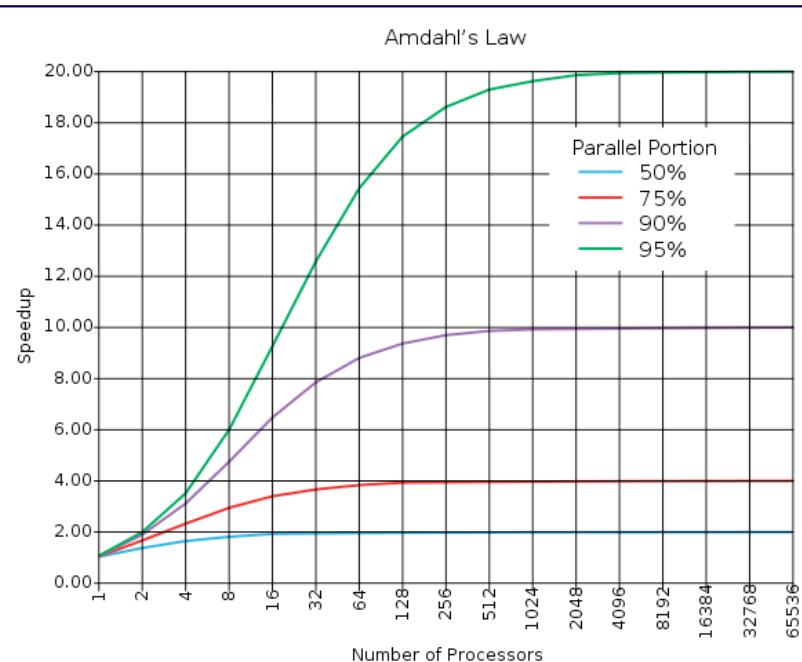
Ex.1: Se 10% de um programa  
executa 90x mais rápido

**Overall speedup = 1.11**

Ex.2: Se 90% de um prog  
executa 90x mais rápido

**Overall speedup = 9.09**

**Paralelismo:**  
se  $N_{\text{proc}} \equiv \text{speedup}$ , trocar **s** por  **$N_{\text{proc}}$**



# Amdahl's Law



$$\text{Overall Speedup} = \frac{\text{Old execution time}}{\text{New execution time}}$$

$$= \frac{1}{\left( (1 - \text{Fraction}_{\text{enhanced}}) + \frac{\text{Fraction}_{\text{enhanced}}}{\text{Speedup}_{\text{enhanced}}} \right)}$$

$$\text{Speedup} = \frac{1}{(1 - p) + p/N}$$

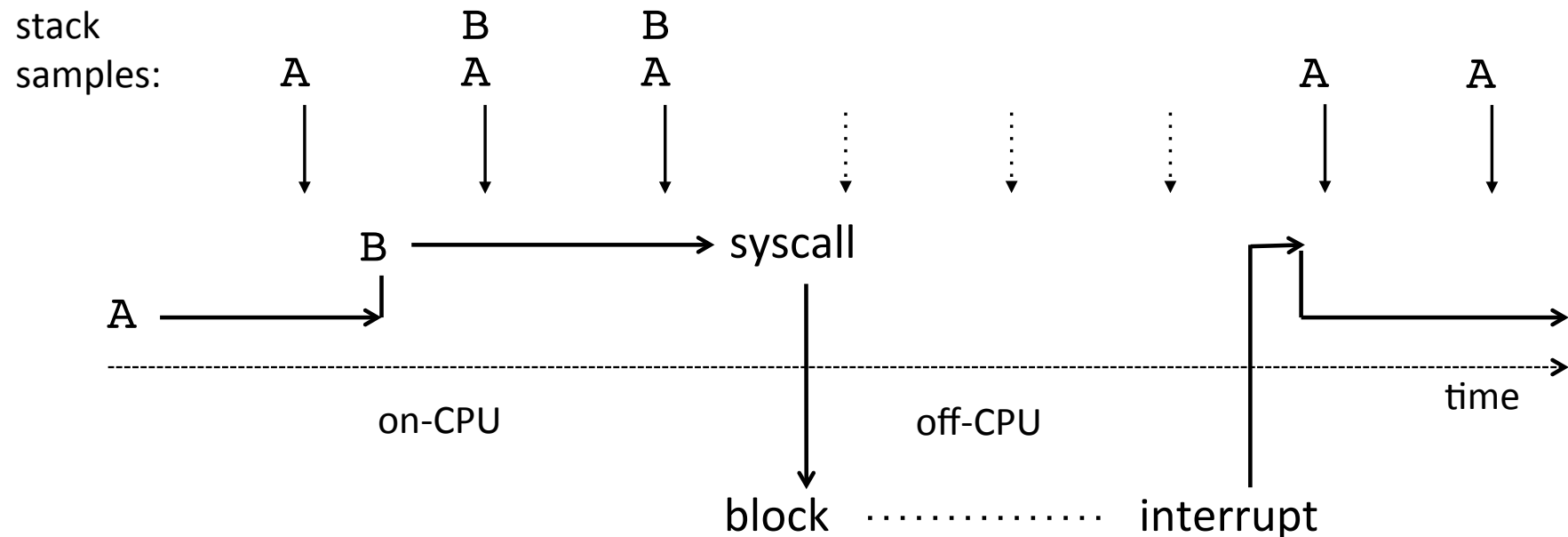
$$\text{Speedup}(N) = \frac{1}{(1-P) + \frac{P}{N}}$$

Serial part of job =  
1 (100%) - Parallel part

Parallel part is divided  
up by N workers

# CPU profiling using sampling

- Record stacks at a timed interval: simple and effective
  - Pros: Low (deterministic) overhead
  - Cons: Coarse accuracy, but usually sufficient





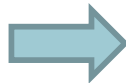
# Profiling code execution

## Techniques to measure the application time-profile (profiling)

### Polling (sampling)

- the application is periodically interrupted to collect performance data
- Example: gprof

Flat view



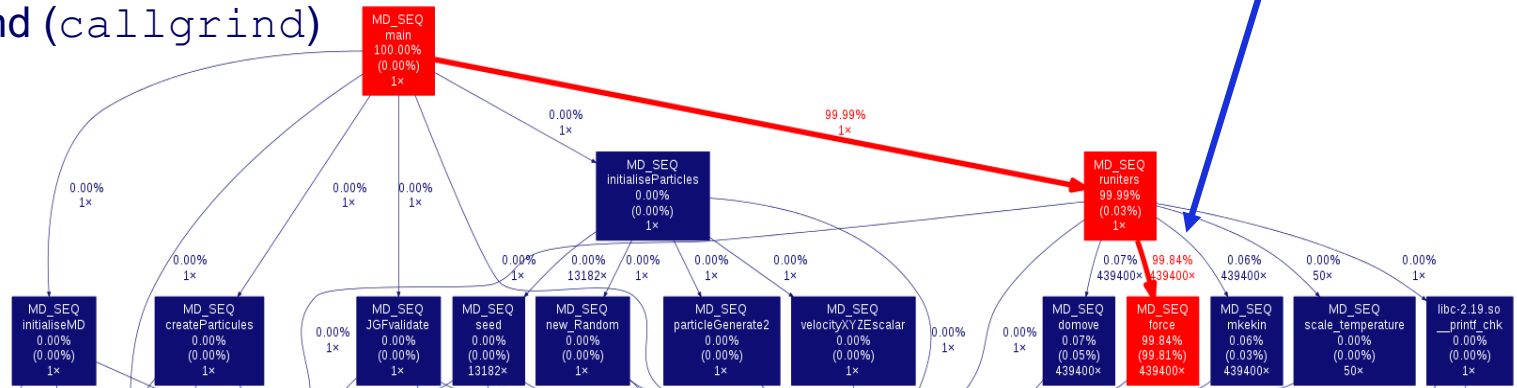
% time	cumulative seconds	self seconds	calls	self s/call	total s/call	name
50.00	2.47	2.47	2	1.24	1.24	matSqrt
24.70	3.69	1.22	1	1.22	1.22	matCube
24.70	4.91	1.22	1	1.22	1.22	sysCube
0.61	4.94	0.03	1	0.03	4.94	main
0.00	4.94	0.00	2	0.00	0.00	vecSqrt
0.00	4.94	0.00	1	0.00	1.24	sysSqrt
0.00	4.94	0.00	1	0.00	0.00	vecCube

Hot-spot

### Instrumentation

- programmer (or tools) introduce code to collect performance data on useful events
  - may produce better results but also produces more interference (e.g., overhead)
- Example: Valgrind (callgrind)

Tree view

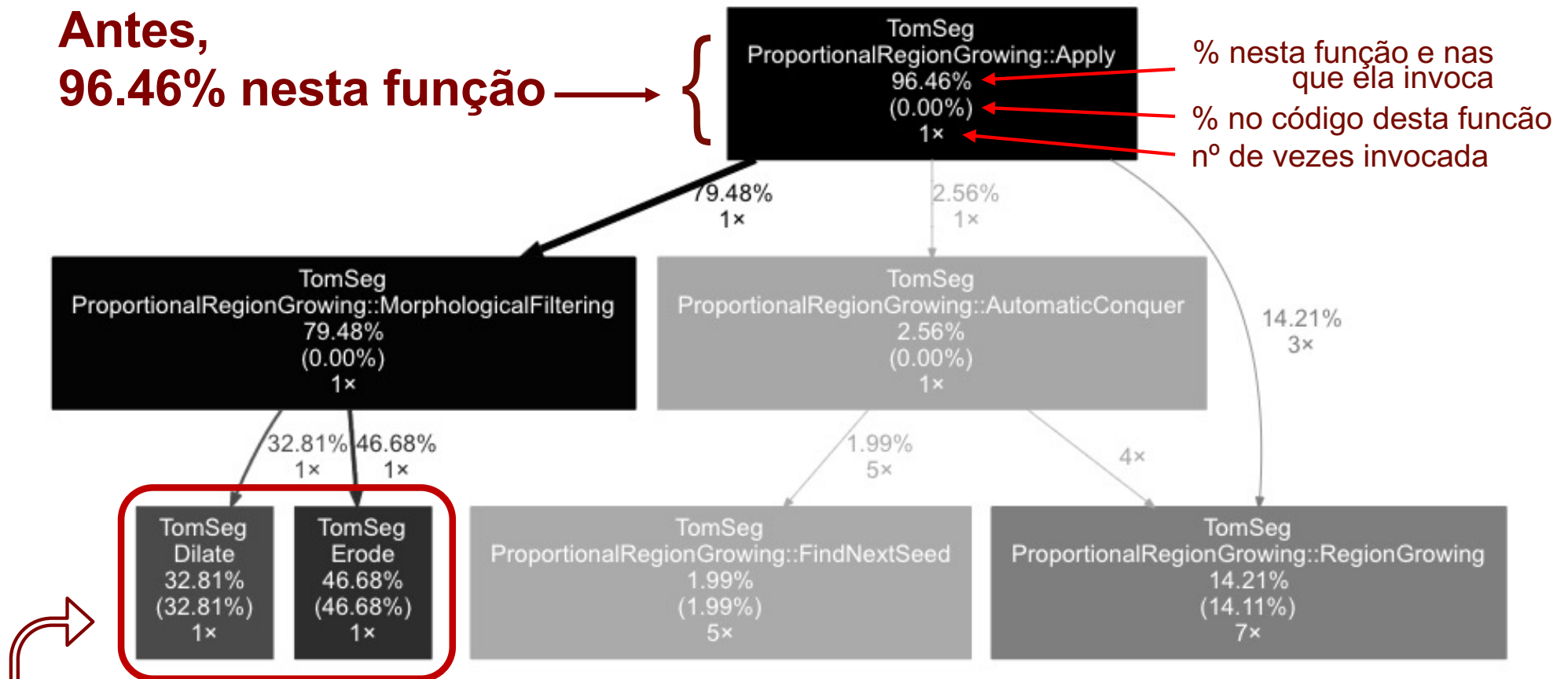


## Code profiling: análise visual da melhoria de código duma função (antes)



Antes,

96.46% nesta função



Quase 80% do tempo total é gasto nestas 2 funções da filtragem morfológica!

Conclusão: é aqui que se deve investir para melhorar a *performance* global

Figure 5.7.: Call-graph of the first version of *Propor. Region Growing* (DS<sub>3</sub>)

## Code profiling: análise visual da melhoria de código duma função (depois)

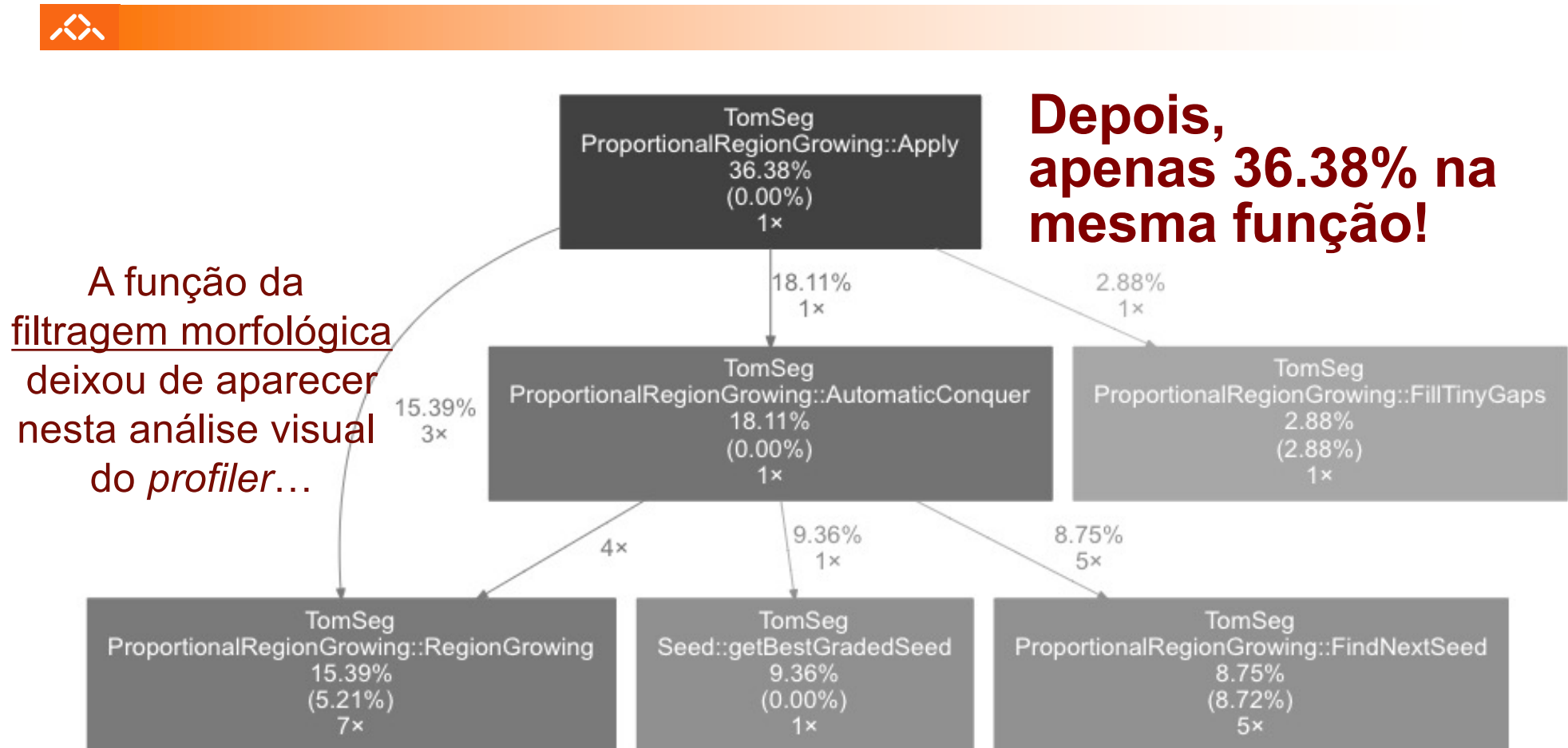


Figure 5.9.: Call-graph from the last version of *Propor. Region Growing* (DS<sub>3</sub>)