Projeto de Sistemas Digitais

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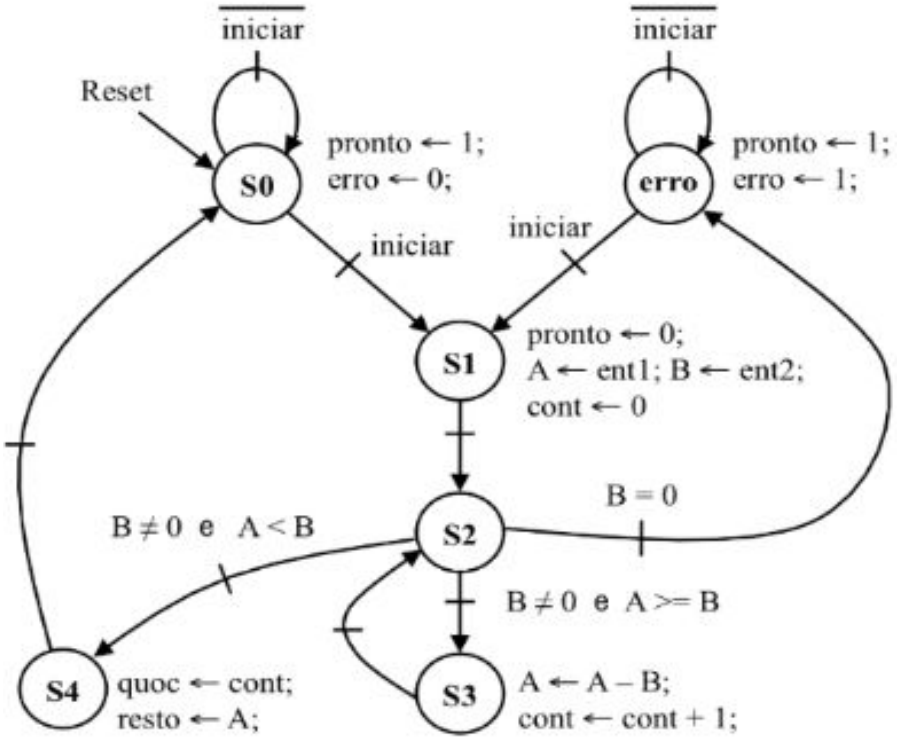
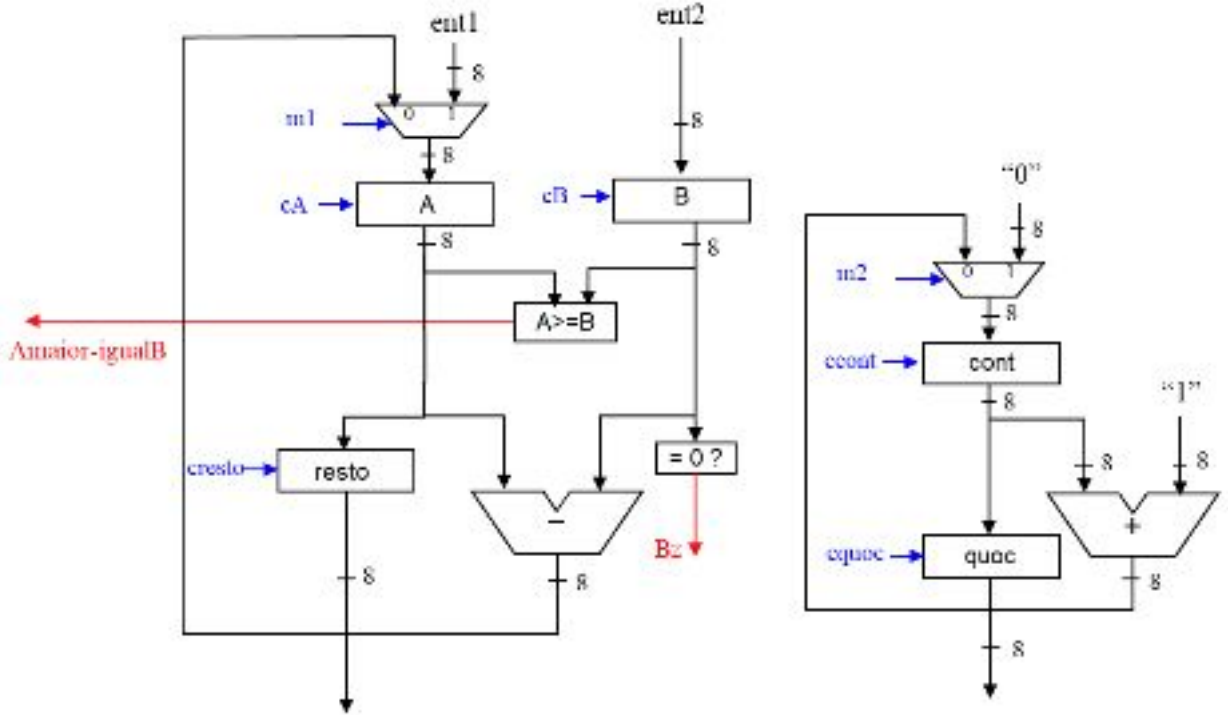
Algoritmo de divisão

```
   Algoritmo divseq
1  Início{
2    A ← ent1; B ← ent2; cont ← 0; pronto←0;
3    if B!=0 then {
4      while A >= B {
5        cont ← cont + 1;
6        A ← A - B; }
7      quoc ← cont; resto ← A;
8      pronto←1; erro←0;
9    }
10   else
11     pronto←1; erro←1;
12 }
```

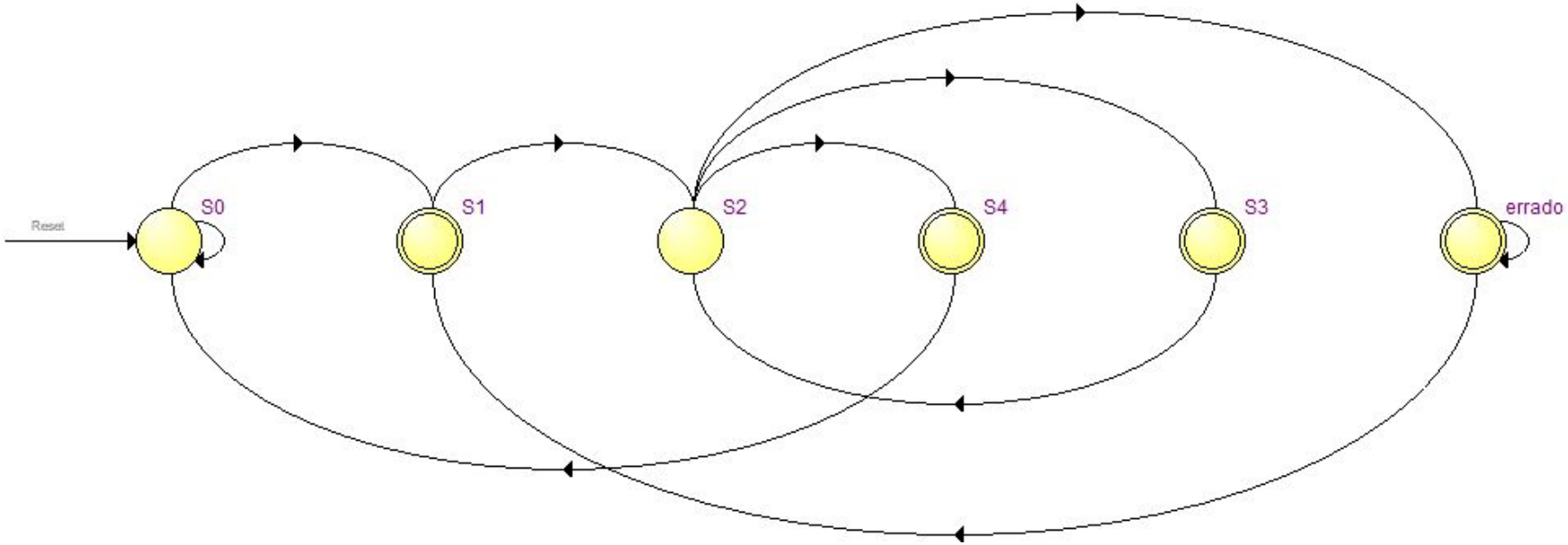
FSMD


iniciar
iniciar
Reset
pronto ← 1;
erro ← 0;
S0
erro
pronto ← 1;
erro ← 1;
iniciar
iniciar
S1
pronto ← 0;
A ← ent1; B ← ent2;
cont ← 0
B = 0
B ≠ 0 e A < B
S2
B ≠ 0 e A >= B
S4
quoc ← cont;
resto ← A;
S3
A ← A – B;
cont ← cont + 1;

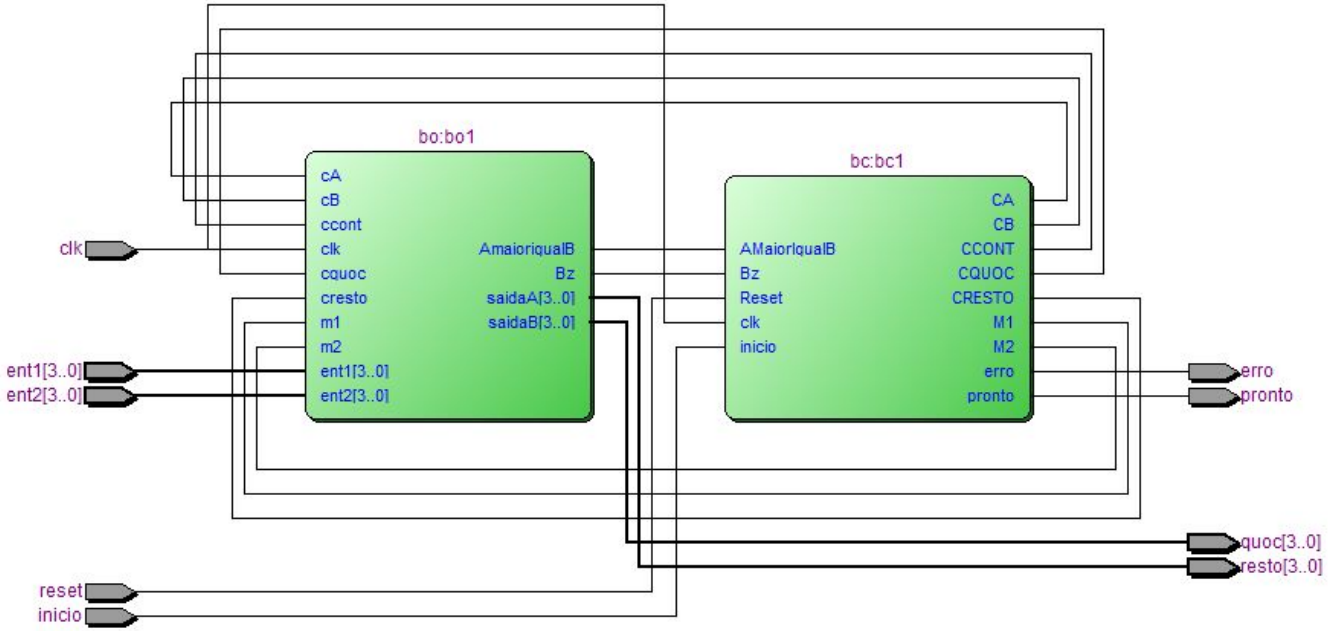
Bloco Operativo



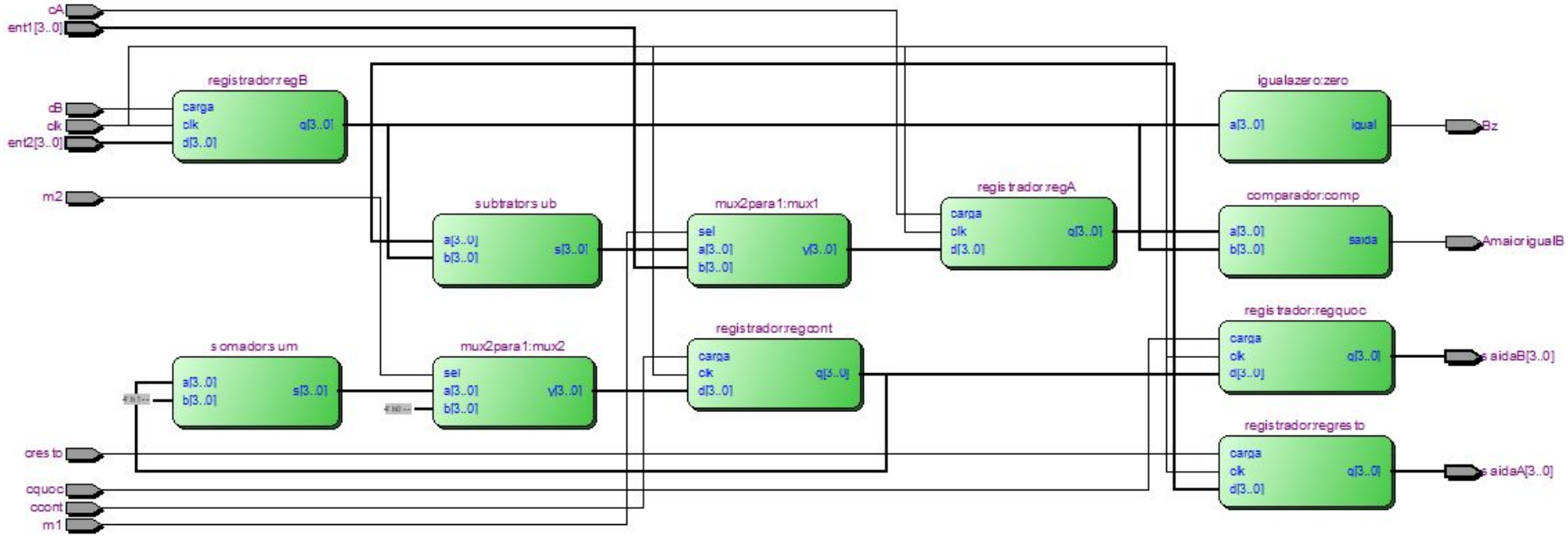
State Machine Viewer



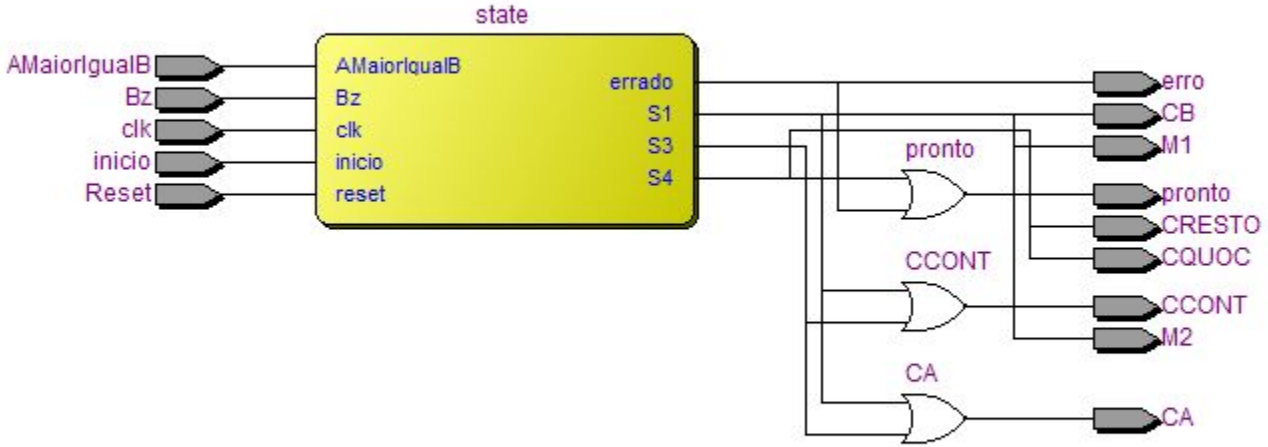
RTL Viewer - Topo



RTL Viewer - BO



RTL Viewer - BC



Comparação N = 4 e N = 8

Flow Status	Successful - Wed Nov 25 16:51:03 2020
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name	divisor
Top-level Entity Name	divisor
Family	Cyclone II
Device	EP2C35F672C6
Timing Models	Final
Total logic elements	33 / 33,216 (< 1 %)
Total combinational functions	21 / 33,216 (< 1 %)
Dedicated logic registers	26 / 33,216 (< 1 %)
Total registers	26
Total pins	21 / 475 (4 %)
Total virtual pins	0
Total memory bits	0 / 483,840 (0 %)
Embedded Multiplier 9-bit elements	0 / 70 (0 %)
Total PLLs	0 / 4 (0 %)

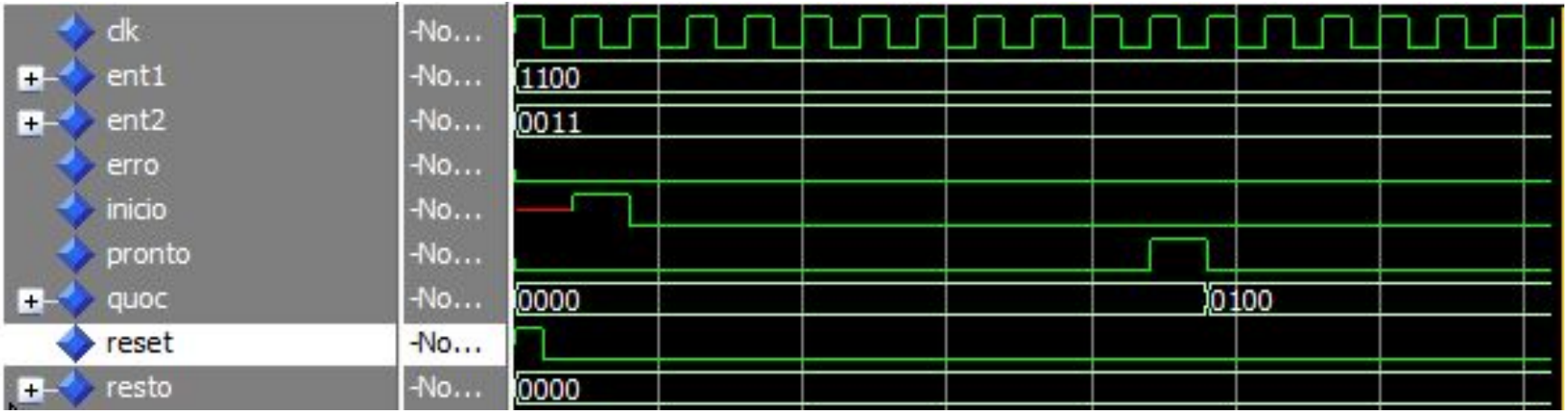
Flow Status	Successful - Wed Nov 25 16:55:59 2020
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name	divisor
Top-level Entity Name	divisor
Family	Cyclone II
Device	EP2C35F672C6
Timing Models	Final
Total logic elements	50 / 33,216 (< 1 %)
Total combinational functions	34 / 33,216 (< 1 %)
Dedicated logic registers	46 / 33,216 (< 1 %)
Total registers	46
Total pins	37 / 475 (8 %)
Total virtual pins	0
Total memory bits	0 / 483,840 (0 %)
Embedded Multiplier 9-bit elements	0 / 70 (0 %)
Total PLLs	0 / 4 (0 %)

Comparação N = 4 e N = 8

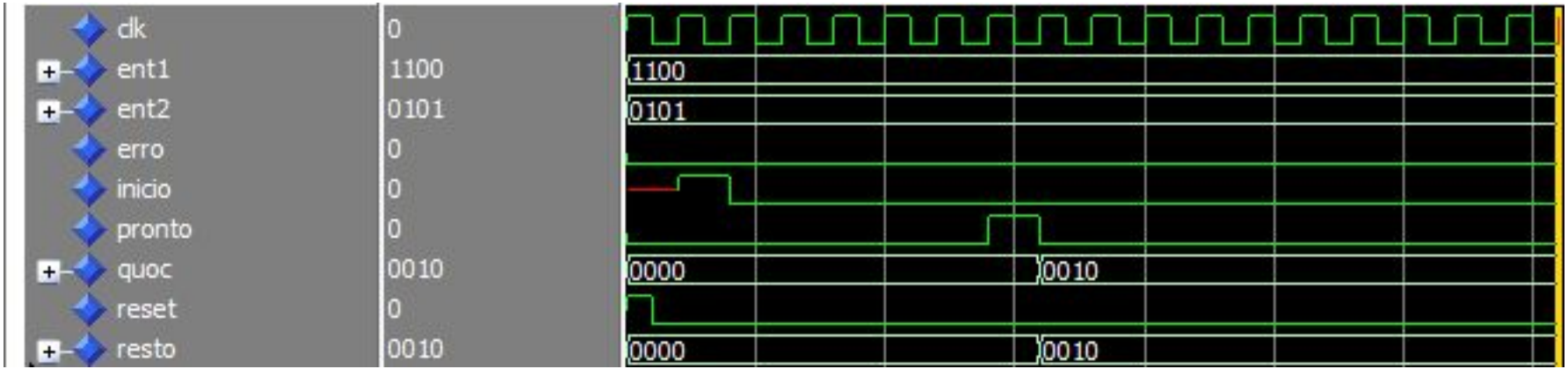
	Data Port	Clock Port	Rise	Fall	Clock Edge	Clock Reference
1	erro	clk	6.750	6.750	Rise	clk
2	pronto	clk	7.227	7.227	Rise	clk
3	quoc[*]	clk	6.392	6.392	Rise	clk
1	quoc[0]	clk	6.392	6.392	Rise	clk
2	quoc[1]	clk	6.585	6.585	Rise	clk
3	quoc[2]	clk	6.603	6.603	Rise	clk
4	quoc[3]	clk	6.600	6.600	Rise	clk
4	resto[*]	clk	6.342	6.342	Rise	clk
1	resto[0]	clk	6.402	6.402	Rise	clk
2	resto[1]	clk	6.342	6.342	Rise	clk
3	resto[2]	clk	6.595	6.595	Rise	clk
4	resto[3]	clk	6.610	6.610	Rise	clk

	Data Port	Clock Port	Rise	Fall	Clock Edge	Clock Reference
1	erro	clk	6.613	6.613	Rise	clk
2	pronto	clk	7.186	7.186	Rise	clk
3	quoc[*]	clk	6.270	6.270	Rise	clk
1	quoc[0]	clk	6.370	6.370	Rise	clk
2	quoc[1]	clk	6.358	6.358	Rise	clk
3	quoc[2]	clk	6.270	6.270	Rise	clk
4	quoc[3]	clk	6.411	6.411	Rise	clk
5	quoc[4]	clk	6.523	6.523	Rise	clk
6	quoc[5]	clk	6.528	6.528	Rise	clk
7	quoc[6]	clk	6.357	6.357	Rise	clk
8	quoc[7]	clk	6.396	6.396	Rise	clk
4	resto[*]	clk	6.333	6.333	Rise	clk
1	resto[0]	clk	6.370	6.370	Rise	clk
2	resto[1]	clk	6.333	6.333	Rise	clk
3	resto[2]	clk	6.838	6.838	Rise	clk
4	resto[3]	clk	6.351	6.351	Rise	clk
5	resto[4]	clk	6.582	6.582	Rise	clk
6	resto[5]	clk	6.550	6.550	Rise	clk
7	resto[6]	clk	6.840	6.840	Rise	clk
8	resto[7]	clk	6.370	6.370	Rise	clk

Simulação 12 / 3 - 4 bits



Simulação 12 / 5 - 4 bits



Simulação 12 / 3 - 8 Bits

Conclusão

- Aumento de aprox. 50% na quantidade de elementos lógicos comparando 4 e 8 bits.

- O tempo mínimo de clock até a saída diminui levemente na versão com 8 bits.

Fim