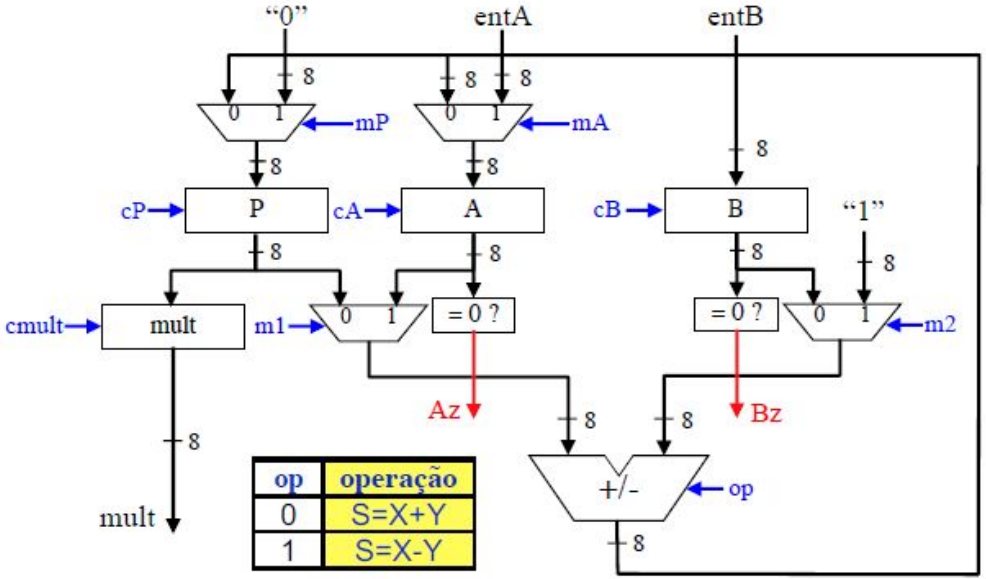
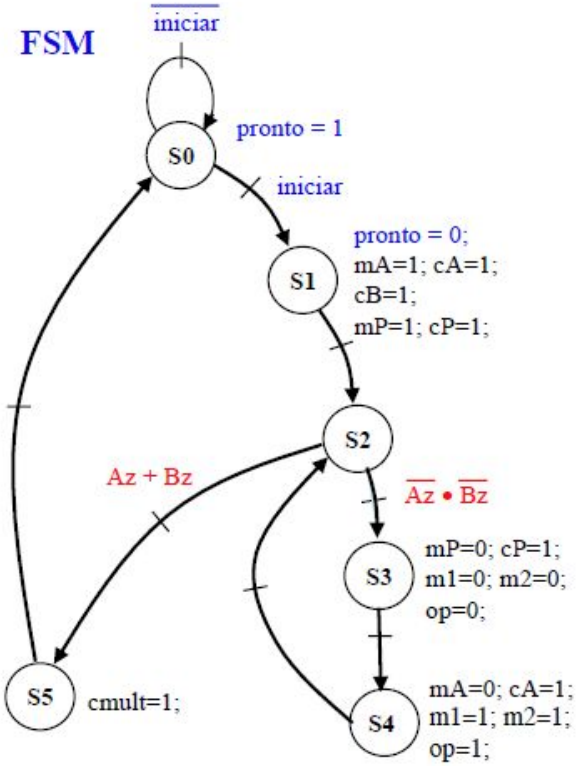
Arquiteturas de multiplicadores

- Arthur Alexandre Nascimento
- Eduardo Vinicius Betim
- Fábio Pereira dos Santos
- Rafael Francisco Réus

Exemplo 4 - Aula 5T (Circuito/FSM)

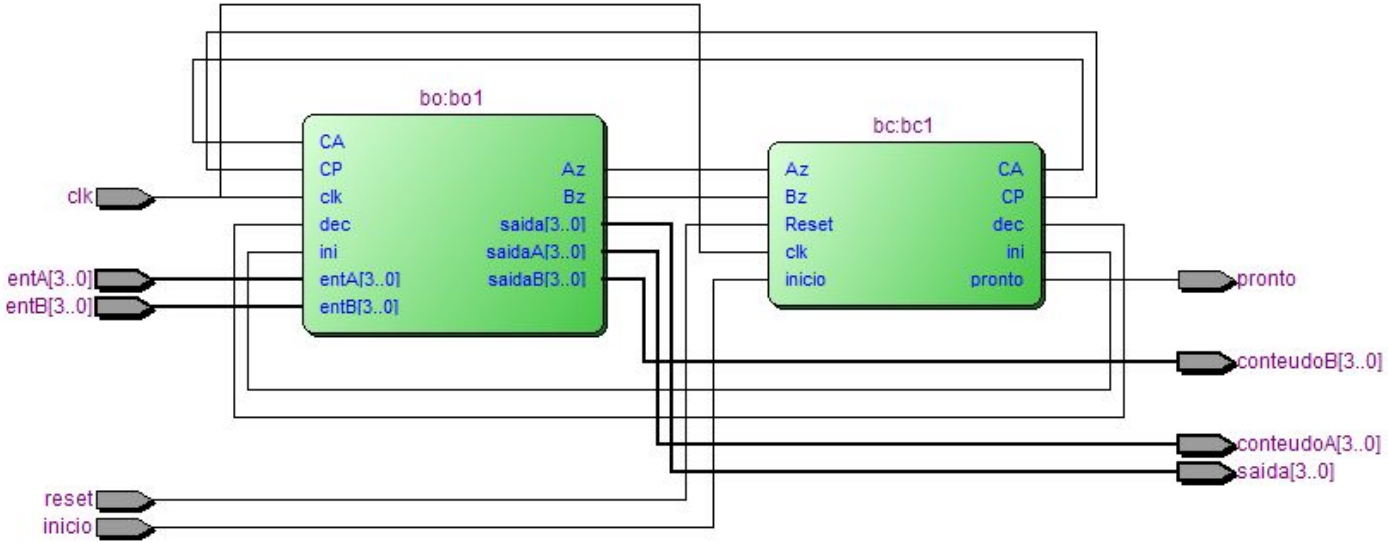


op	operação
0	S=X+Y
1	S=X-Y

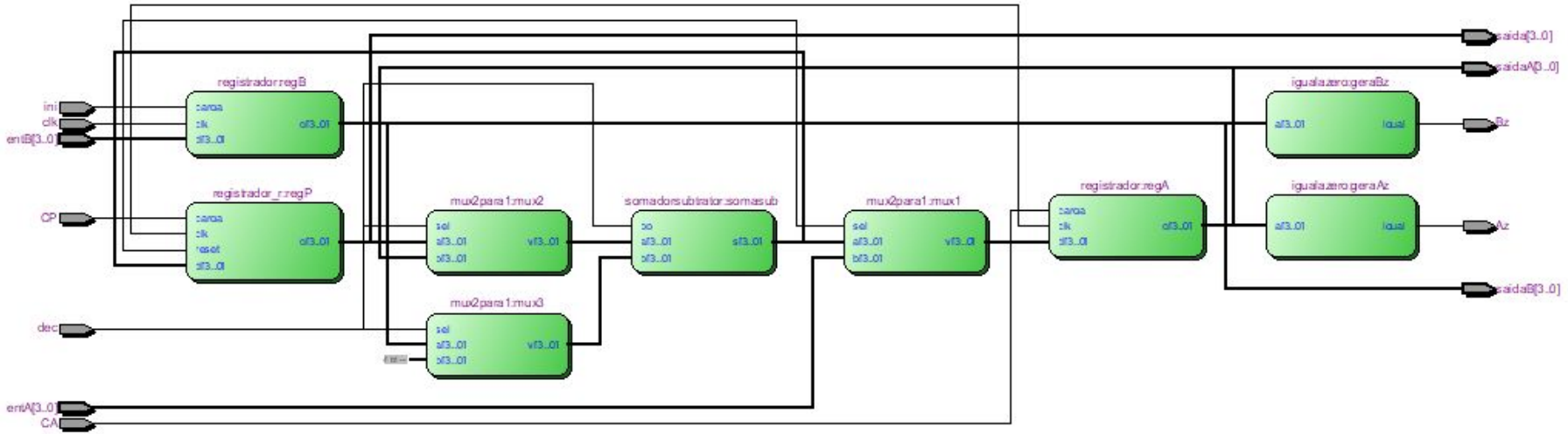


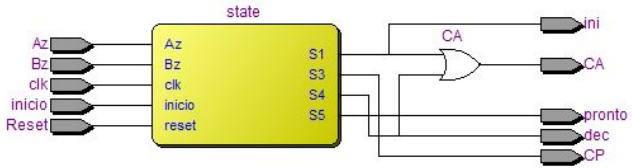
Exemplo 4 - Aula 5T(RTL View)

RTL Viewer:



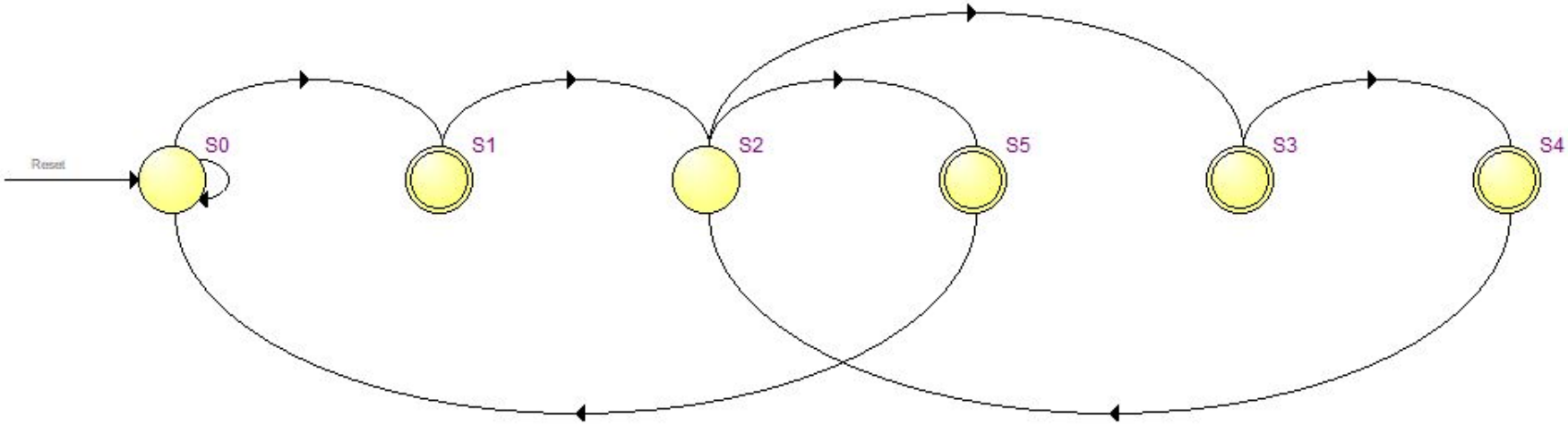
Exemplo 4 - Aula 5T(RTL VIEW2)





Exemplo 4 - Aula 5T (FSM)

State Machine:



Exemplo 4 - Aula 5T (N = 4)

Sumário:

Flow Status	Successful - Wed Nov 11 14:55:55 2020
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name	multiplicador
Top-level Entity Name	multiplicador
Family	Cyclone II
Device	EP2C35F672C6
Timing Models	Final
Total logic elements	29 / 33,216 (< 1 %)
Total combinational functions	24 / 33,216 (< 1 %)
Dedicated logic registers	18 / 33,216 (< 1 %)
Total registers	18
Total pins	24 / 475 (5 %)
Total virtual pins	0
Total memory bits	0 / 483,840 (0 %)
Embedded Multiplier 9-bit elements	0 / 70 (0 %)
Total PLLs	0 / 4 (0 %)

Temporização:

	Data Port	Clock Port	Rise	Fall	Clock Edge	Clock Reference
1	conteudoA[*]	clk	6.379	6.379	Rise	clk
1	conteudoA[0]	clk	6.822	6.822	Rise	clk
2	conteudoA[1]	clk	6.755	6.755	Rise	clk
3	conteudoA[2]	clk	6.556	6.556	Rise	clk
4	conteudoA[3]	clk	6.379	6.379	Rise	clk
2	conteudoB[*]	clk	6.399	6.399	Rise	clk
1	conteudoB[0]	clk	6.423	6.423	Rise	clk
2	conteudoB[1]	clk	6.604	6.604	Rise	clk
3	conteudoB[2]	clk	6.399	6.399	Rise	clk
4	conteudoB[3]	clk	6.603	6.603	Rise	clk
3	pronto	clk	6.655	6.655	Rise	clk
4	saida[*]	clk	6.370	6.370	Rise	clk
1	saida[0]	clk	6.613	6.613	Rise	clk
2	saida[1]	clk	6.370	6.370	Rise	clk
3	saida[2]	clk	6.808	6.808	Rise	clk
4	saida[3]	clk	6.828	6.828	Rise	clk

Exemplo 4 - Aula 5T (N = 8)

Sumário:

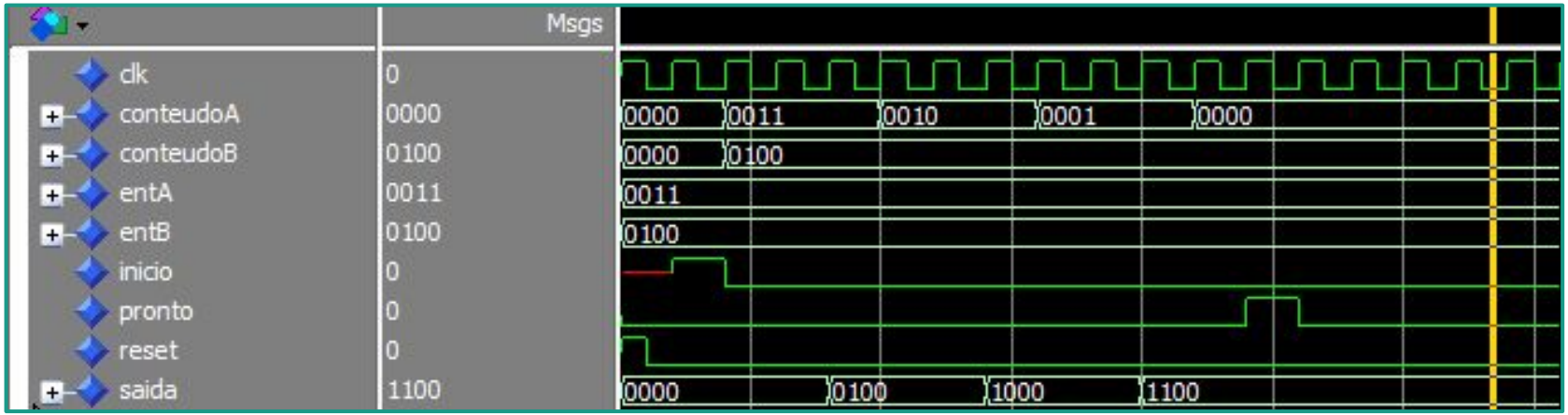
Flow Status	Successful - Wed Nov 11 15:01:08 2020
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name	multiplicador
Top-level Entity Name	multiplicador
Family	Cyclone II
Device	EP2C35F672C6
Timing Models	Final
Total logic elements	48 / 33,216 (< 1 %)
Total combinational functions	43 / 33,216 (< 1 %)
Dedicated logic registers	30 / 33,216 (< 1 %)
Total registers	30
Total pins	44 / 475 (9 %)
Total virtual pins	0
Total memory bits	0 / 483,840 (0 %)
Embedded Multiplier 9-bit elements	0 / 70 (0 %)
Total PLLs	0 / 4 (0 %)

Temporização:

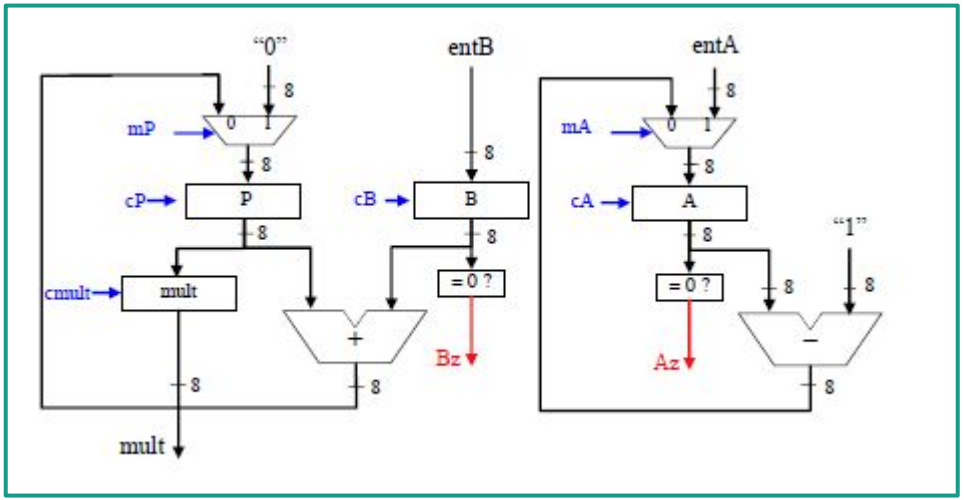
	Data Port	Clock Port	Rise	Fall	Clock Edge	Clock Reference
2	conteudoA[1]	clk	6.589	6.589	Rise	clk
3	conteudoA[2]	clk	6.338	6.338	Rise	clk
4	conteudoA[3]	clk	7.142	7.142	Rise	clk
5	conteudoA[4]	clk	6.586	6.586	Rise	clk
6	conteudoA[5]	clk	6.366	6.366	Rise	clk
7	conteudoA[6]	clk	6.366	6.366	Rise	clk
8	conteudoA[7]	clk	6.330	6.330	Rise	clk
2	⌄ conteudoB[*]	clk	6.365	6.365	Rise	clk
1	conteudoB[0]	clk	7.007	7.007	Rise	clk
2	conteudoB[1]	clk	6.570	6.570	Rise	clk
3	conteudoB[2]	clk	7.035	7.035	Rise	clk
4	conteudoB[3]	clk	7.029	7.029	Rise	clk
5	conteudoB[4]	clk	6.880	6.880	Rise	clk
6	conteudoB[5]	clk	7.012	7.012	Rise	clk
7	conteudoB[6]	clk	6.780	6.780	Rise	clk
8	conteudoB[7]	clk	6.365	6.365	Rise	clk
3	pronto	clk	6.584	6.584	Rise	clk
4	⌄ saida[*]	clk	6.354	6.354	Rise	clk
1	saida[0]	clk	6.563	6.563	Rise	clk
2	saida[1]	clk	6.797	6.797	Rise	clk
3	saida[2]	clk	6.853	6.853	Rise	clk
4	saida[3]	clk	7.016	7.016	Rise	clk
5	saida[4]	clk	6.354	6.354	Rise	clk
6	saida[5]	clk	6.833	6.833	Rise	clk
7	saida[6]	clk	6.799	6.799	Rise	clk
8	saida[7]	clk	6.784	6.784	Rise	clk

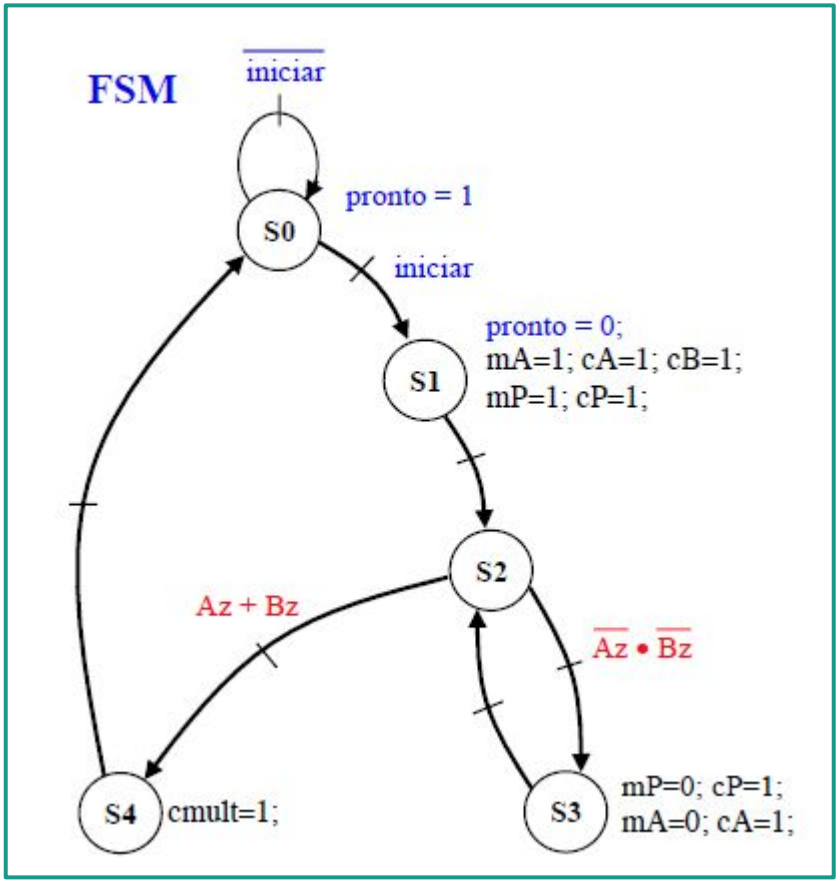
Exemplo 4 - Aula 5T (Wave Simulation - TestBench)

Simulação:

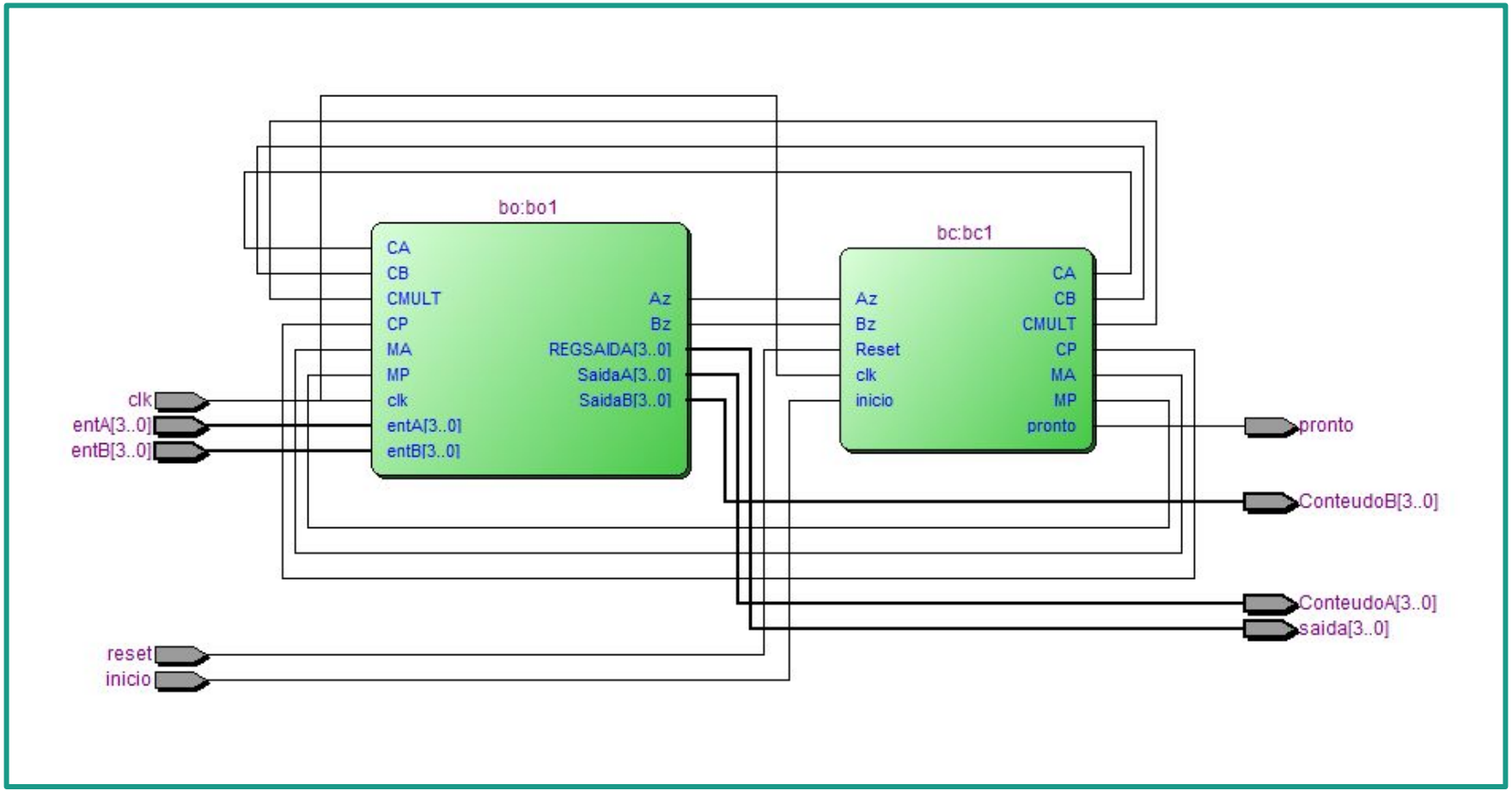


Exemplo 5 - Aula 5T (Circuito e FSM)

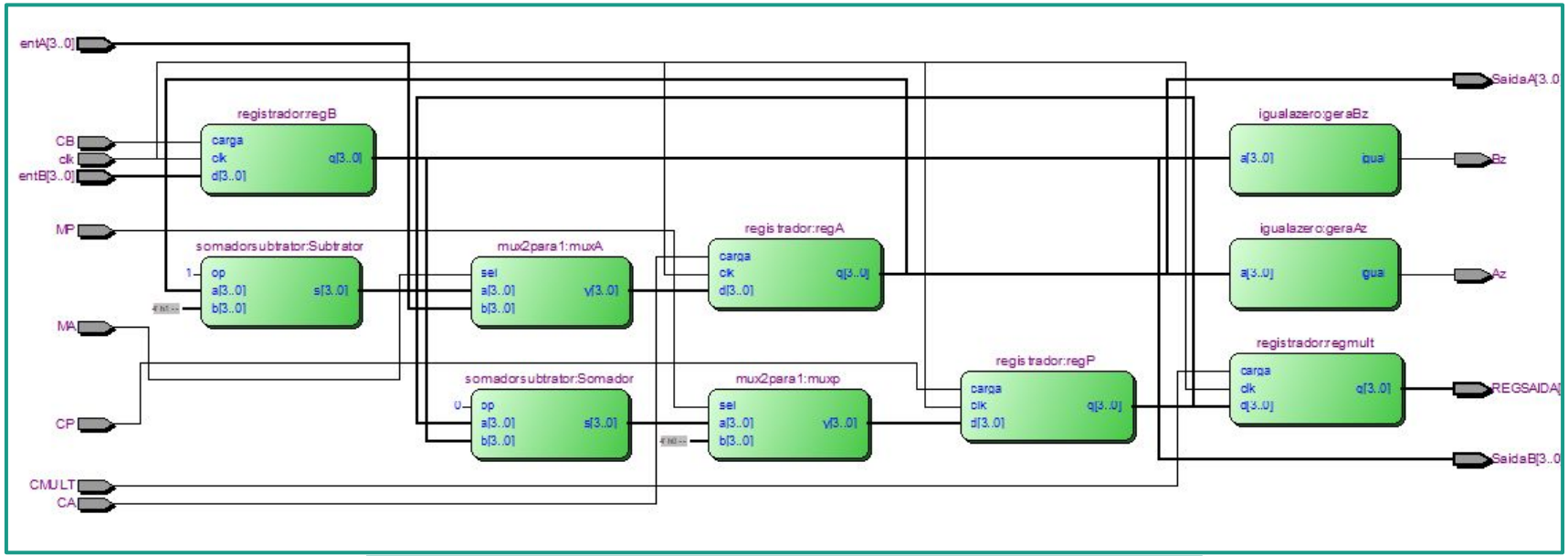


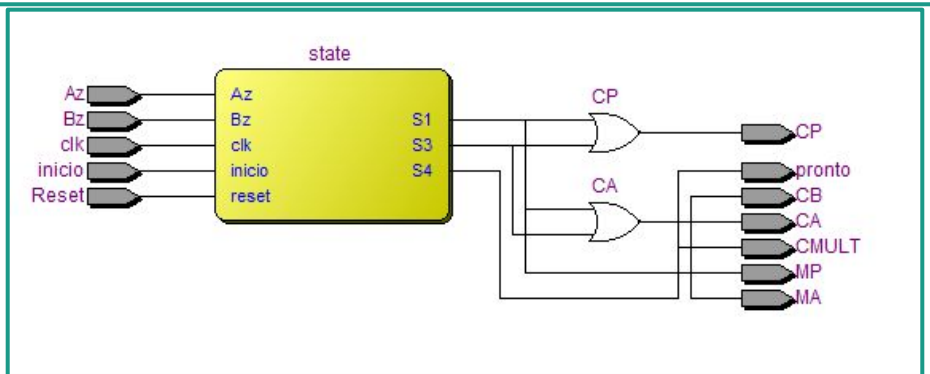


Exemplo 5 - Aula 5T (RTL View)



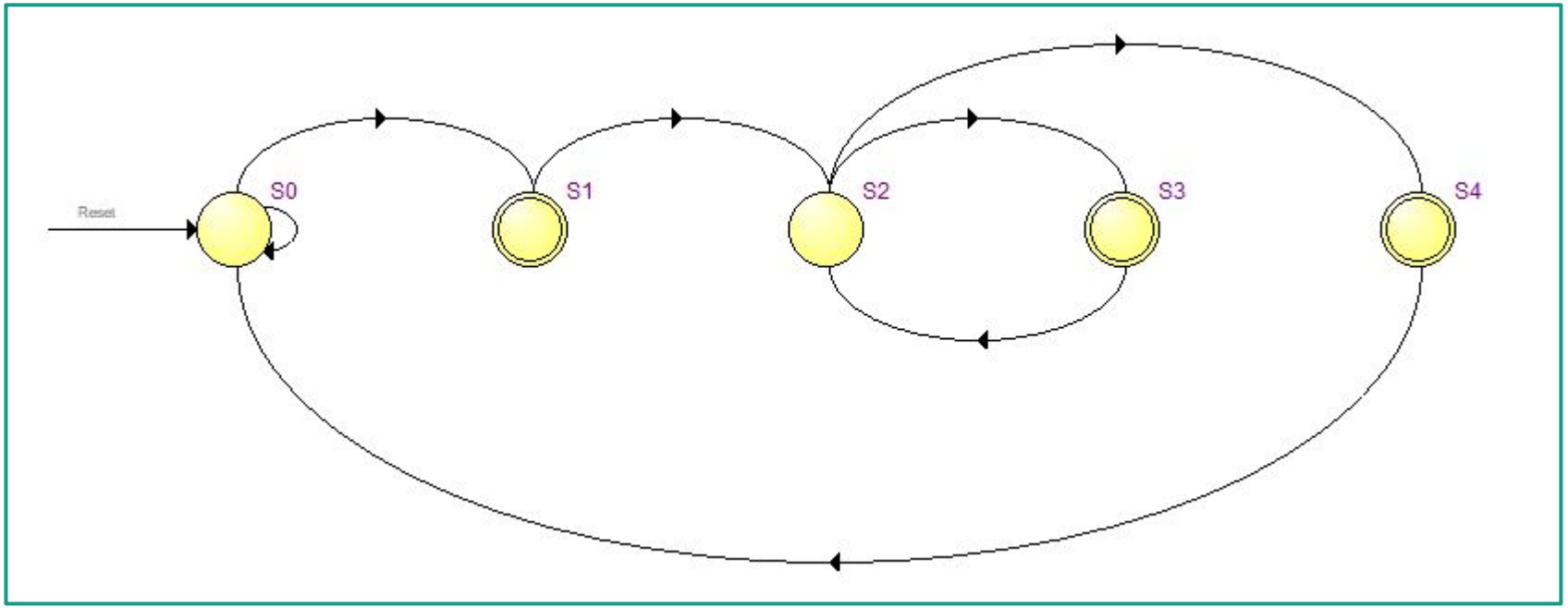
Exemplo 5 - Aula 5T (RTL View2)





Exemplo 5 - Aula 5T (FSM)

State Machine:



Exemplo 5 - Aula 5T (N = 4)

Sumário:

Flow Status	Successful - Wed Nov 11 15:06:05 2020
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name	multiplicador
Top-level Entity Name	multiplicador
Family	Cyclone II
Device	EP2C35F672C6
Timing Models	Final
Total logic elements	24 / 33,216 (< 1 %)
Total combinational functions	16 / 33,216 (< 1 %)
Dedicated logic registers	21 / 33,216 (< 1 %)
Total registers	21
Total pins	24 / 475 (5 %)
Total virtual pins	0
Total memory bits	0 / 483,840 (0 %)
Embedded Multiplier 9-bit elements	0 / 70 (0 %)
Total PLLs	0 / 4 (0 %)

Temporização:

	Data Port	Clock Port	Rise	Fall	Clock Edge	Clock Reference
1	ConteudoA[*]	clk	6.359	6.359	Rise	clk
1	ConteudoA[0]	clk	6.368	6.368	Rise	clk
2	ConteudoA[1]	clk	6.678	6.678	Rise	clk
3	ConteudoA[2]	clk	6.361	6.361	Rise	clk
4	ConteudoA[3]	clk	6.359	6.359	Rise	clk
2	ConteudoB[*]	clk	6.363	6.363	Rise	clk
1	ConteudoB[0]	clk	6.363	6.363	Rise	clk
2	ConteudoB[1]	clk	6.563	6.563	Rise	clk
3	ConteudoB[2]	clk	6.796	6.796	Rise	clk
4	ConteudoB[3]	clk	6.581	6.581	Rise	clk
3	pronto	clk	6.575	6.575	Rise	clk
4	saida[*]	clk	6.326	6.326	Rise	clk
1	saida[0]	clk	6.803	6.803	Rise	clk
2	saida[1]	clk	6.795	6.795	Rise	clk
3	saida[2]	clk	6.327	6.327	Rise	clk
4	saida[3]	clk	6.326	6.326	Rise	clk

Exemplo 5 - Aula 5T (N = 8)

Sumário:

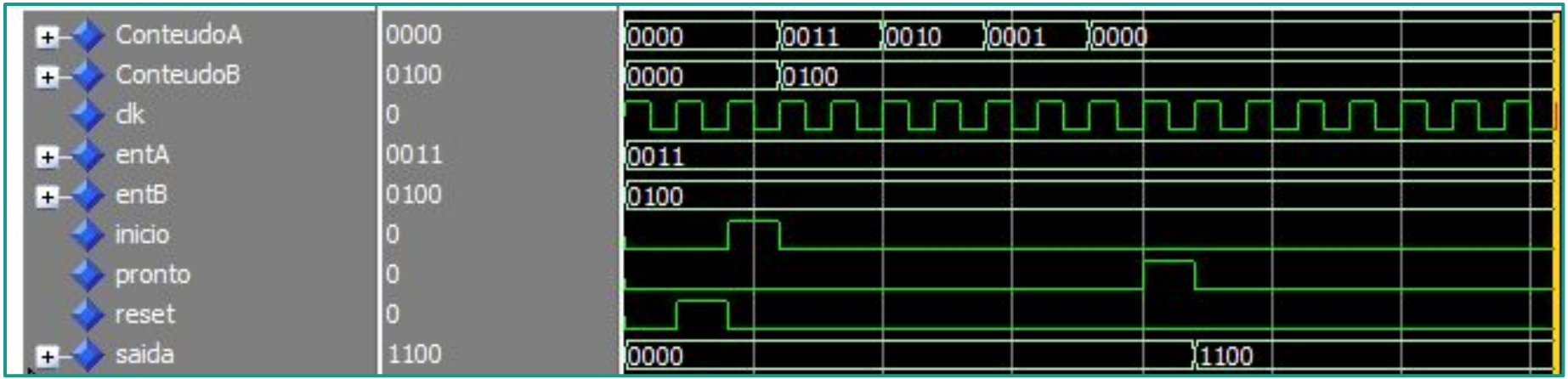
Flow Status	Successful - Wed Nov 11 15:32:48 2020
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name	multiplicador
Top-level Entity Name	multiplicador
Family	Cyclone II
Device	EP2C35F672C6
Timing Models	Final
Total logic elements	42 / 33,216 (< 1 %)
Total combinational functions	26 / 33,216 (< 1 %)
Dedicated logic registers	37 / 33,216 (< 1 %)
Total registers	37
Total pins	44 / 475 (9 %)
Total virtual pins	0
Total memory bits	0 / 483,840 (0 %)
Embedded Multiplier 9-bit elements	0 / 70 (0 %)
Total PLLs	0 / 4 (0 %)

Temporização:

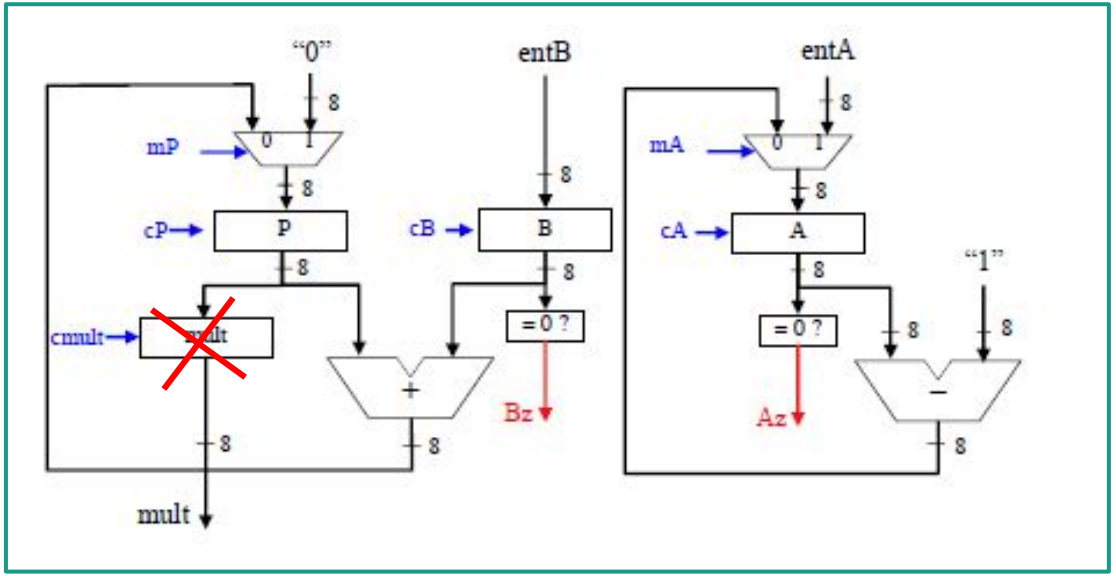
	Data Port	Clock Port	Rise	Fall	Clock Edge	Clock Reference
2	ConteudoA[1]	clk	6.796	6.796	Rise	clk
3	ConteudoA[2]	clk	7.015	7.015	Rise	clk
4	ConteudoA[3]	clk	7.063	7.063	Rise	clk
5	ConteudoA[4]	clk	7.013	7.013	Rise	clk
6	ConteudoA[5]	clk	6.835	6.835	Rise	clk
7	ConteudoA[6]	clk	6.574	6.574	Rise	clk
8	ConteudoA[7]	clk	6.568	6.568	Rise	clk
2	ConteudoB[*]	clk	6.364	6.364	Rise	clk
1	ConteudoB[0]	clk	6.595	6.595	Rise	clk
2	ConteudoB[1]	clk	6.587	6.587	Rise	clk
3	ConteudoB[2]	clk	6.591	6.591	Rise	clk
4	ConteudoB[3]	clk	6.364	6.364	Rise	clk
5	ConteudoB[4]	clk	6.812	6.812	Rise	clk
6	ConteudoB[5]	clk	6.706	6.706	Rise	clk
7	ConteudoB[6]	clk	6.814	6.814	Rise	clk
8	ConteudoB[7]	clk	6.558	6.558	Rise	clk
3	pronto	clk	6.354	6.354	Rise	clk
4	saida[*]	clk	6.325	6.325	Rise	clk
1	saida[0]	clk	6.829	6.829	Rise	clk
2	saida[1]	clk	6.775	6.775	Rise	clk
3	saida[2]	clk	6.842	6.842	Rise	clk
4	saida[3]	clk	6.329	6.329	Rise	clk
5	saida[4]	clk	6.819	6.819	Rise	clk
6	saida[5]	clk	6.805	6.805	Rise	clk
7	saida[6]	clk	6.325	6.325	Rise	clk
8	saida[7]	clk	6.809	6.809	Rise	clk

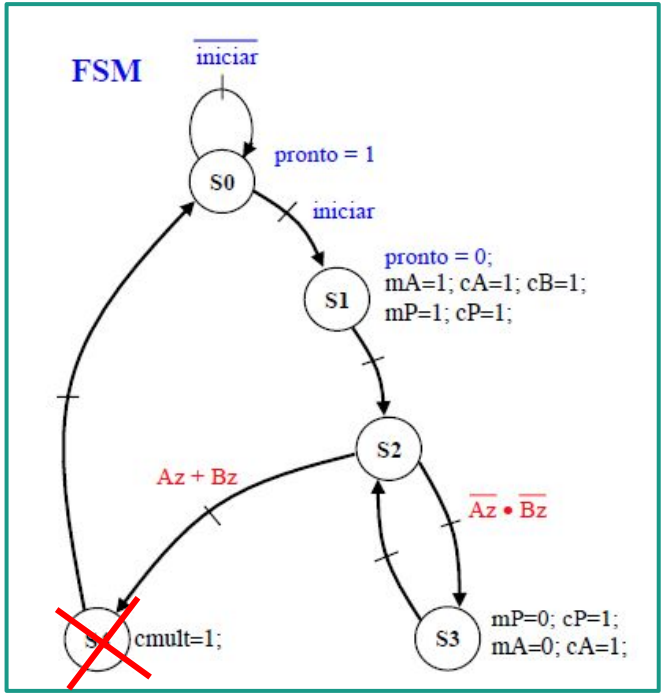
Exemplo 5 - Aula 5T

Simulação:

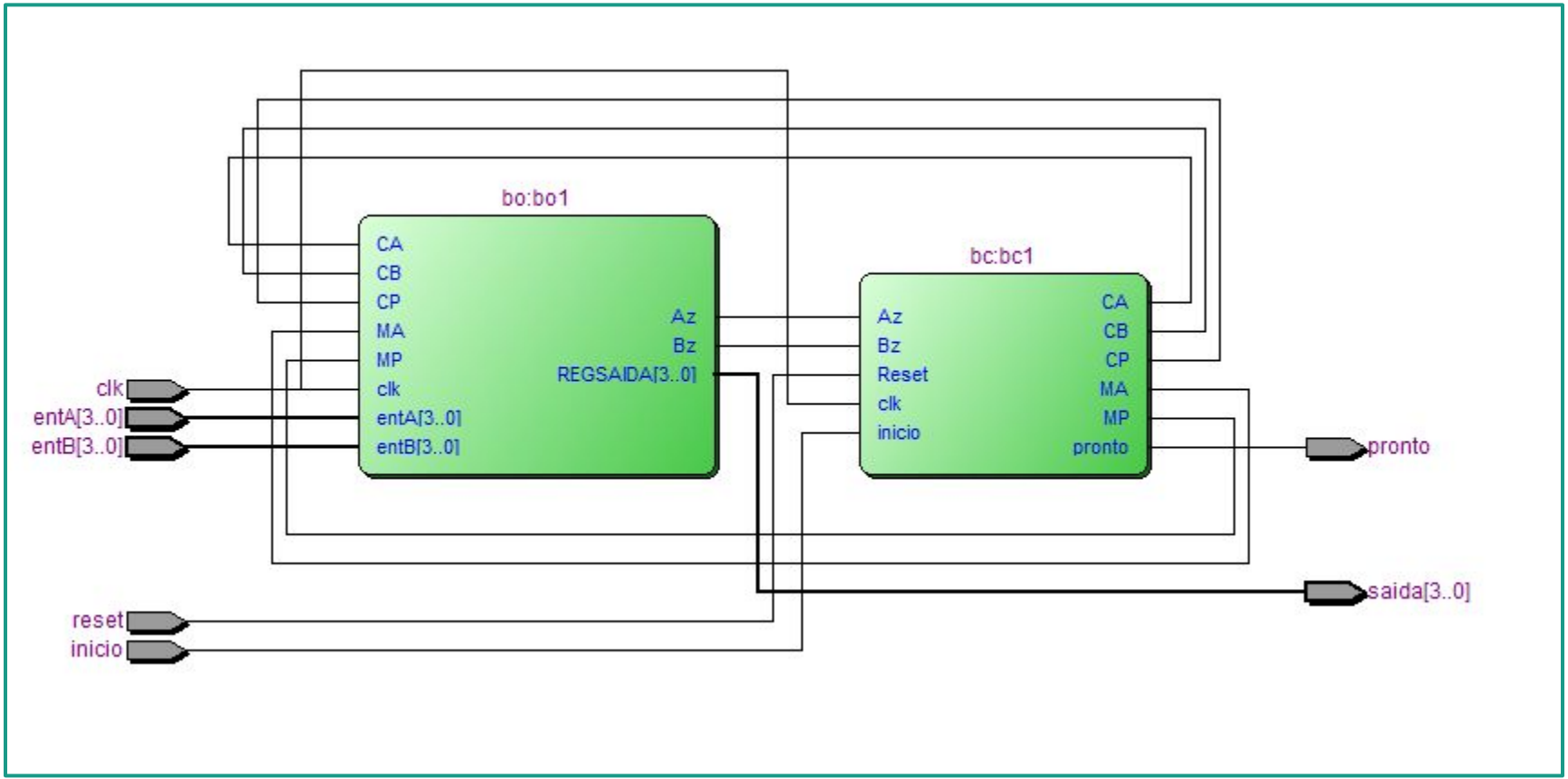


Exemplo 5 adaptado (menor área, mealy)

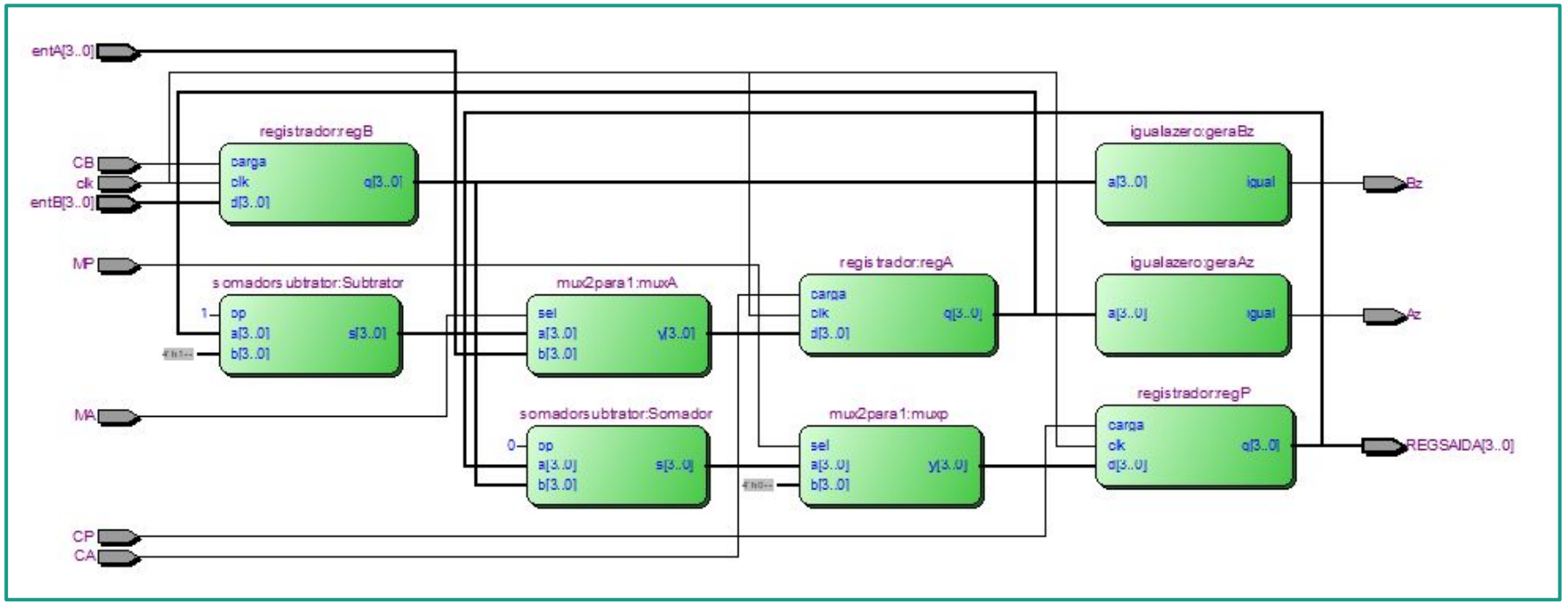




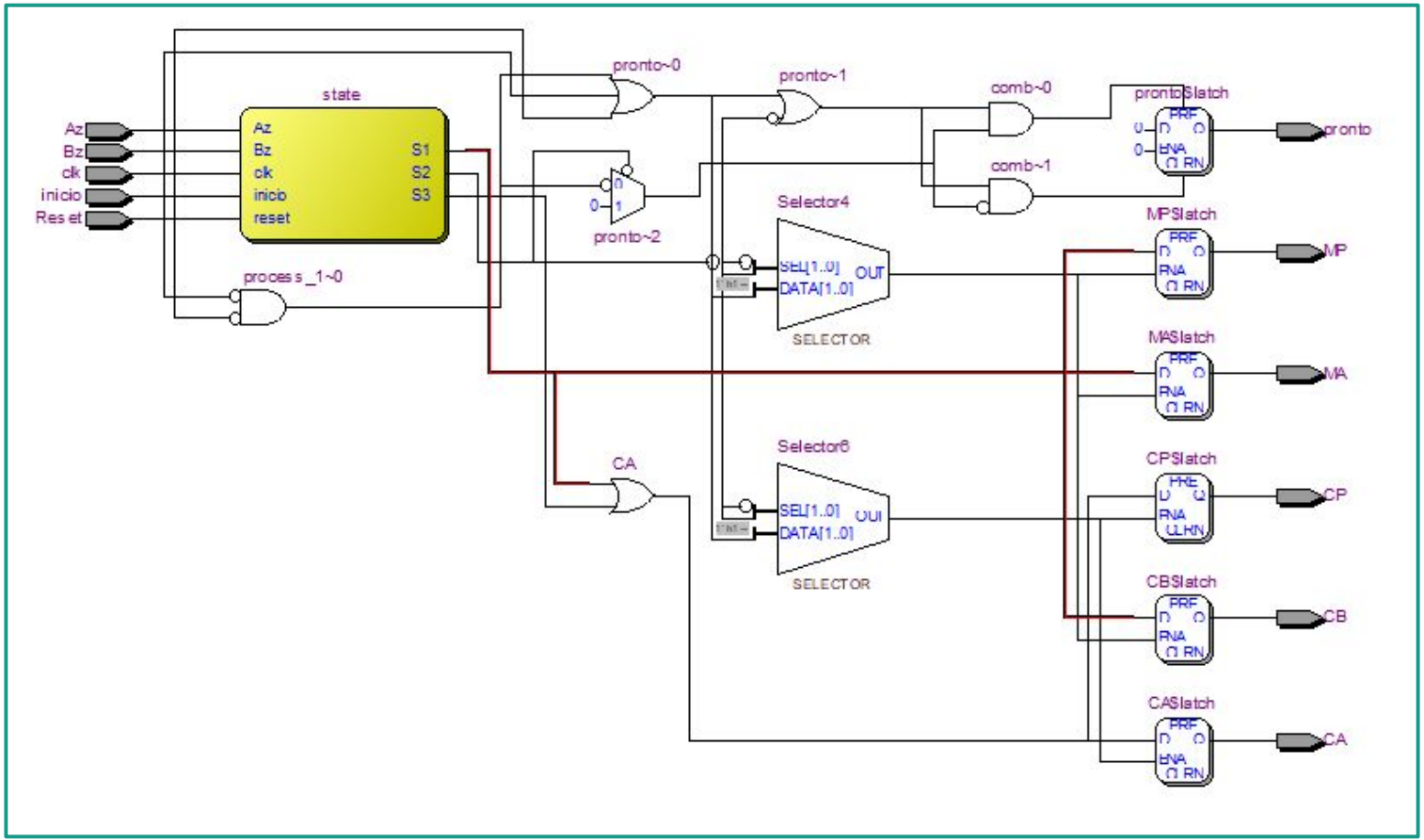
Exemplo 5 adaptado (RTL Viewer)



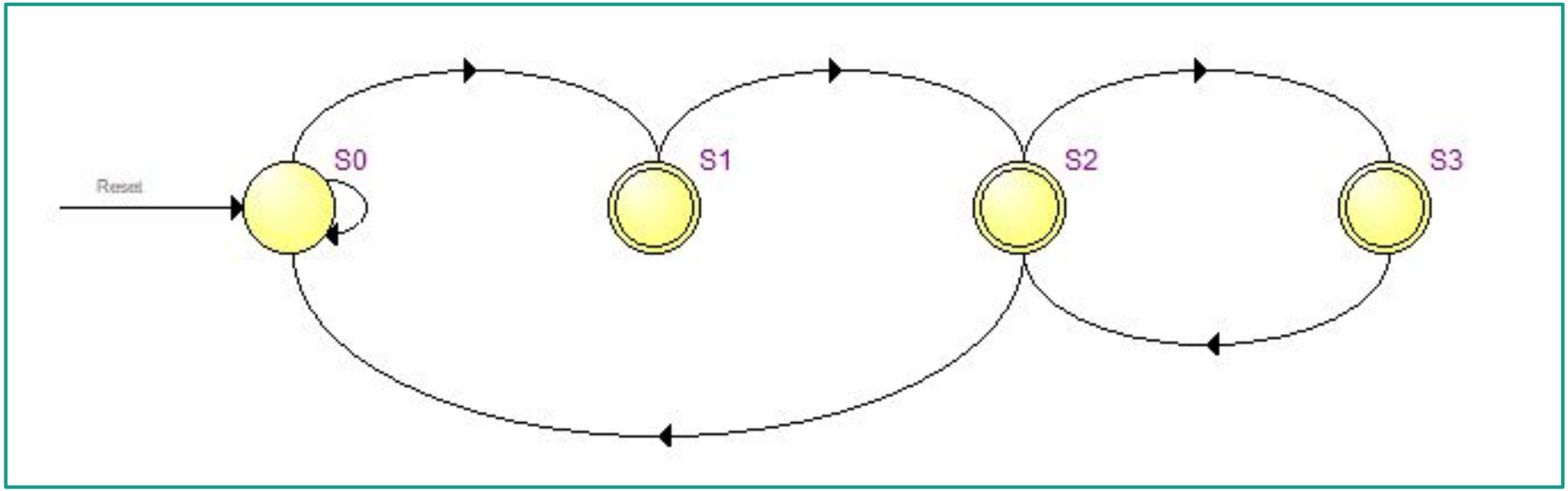
Exemplo 5 adaptado (RTL Viewer)



Exemplo 5 adaptado (RTL Viewer)



Exemplo 5 adaptado (FSM)



Exemplo 5 - adaptado (N = 4)

Sumário:

Flow Status	Successful - Thu Nov 12 00:10:47 2020
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name	multiplicador
Top-level Entity Name	multiplicador
Family	Cyclone II
Device	EP2C35F672C6
Timing Models	Final
Total logic elements	21 / 33,216 (< 1 %)
Total combinational functions	18 / 33,216 (< 1 %)
Dedicated logic registers	16 / 33,216 (< 1 %)
Total registers	16
Total pins	16 / 475 (3 %)
Total virtual pins	0
Total memory bits	0 / 483,840 (0 %)
Embedded Multiplier 9-bit elements	0 / 70 (0 %)
Total PLLs	0 / 4 (0 %)

Temporização:

	Data Port	Clock Port	Rise	Fall	Clock Edge	Clock Reference
1	pronto	clk	7.316	7.316	Rise	clk
2	saida[*]	clk	6.055	6.055	Rise	clk
1	saida[0]	clk	6.058	6.058	Rise	clk
2	saida[1]	clk	6.367	6.367	Rise	clk
3	saida[2]	clk	6.055	6.055	Rise	clk
4	saida[3]	clk	6.083	6.083	Rise	clk

Exemplo 5 - adaptado (N = 8)

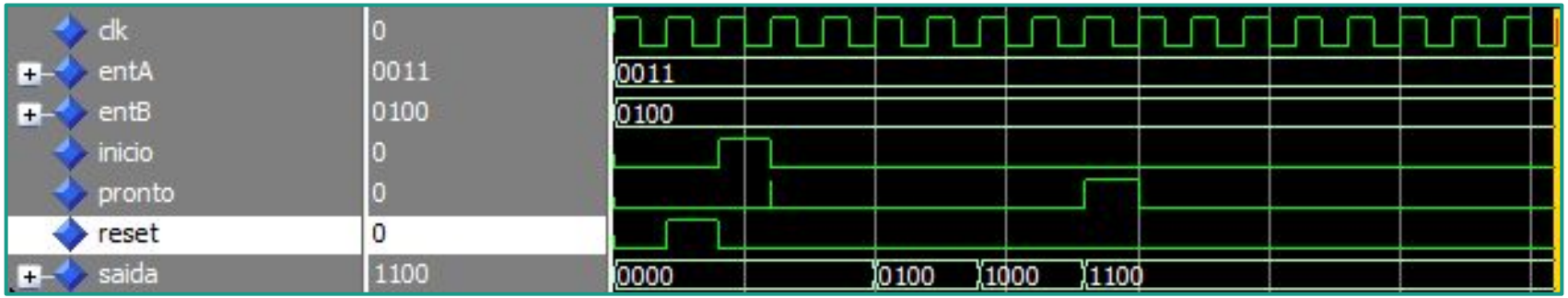
Sumário:

Flow Status	Successful - Thu Nov 12 00:17:46 2020
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name	multiplicador
Top-level Entity Name	multiplicador
Family	Cyclone II
Device	EP2C35F672C6
Timing Models	Final
Total logic elements	34 / 33,216 (< 1 %)
Total combinational functions	26 / 33,216 (< 1 %)
Dedicated logic registers	28 / 33,216 (< 1 %)
Total registers	28
Total pins	28 / 475 (6 %)
Total virtual pins	0
Total memory bits	0 / 483,840 (0 %)
Embedded Multiplier 9-bit elements	0 / 70 (0 %)
Total PLLs	0 / 4 (0 %)

Temporização:

	Data Port	Clock Port	Rise	Fall	Clock Edge	Clock Reference
1	pronto	clk	7.314	7.314	Rise	clk
2	saida[*]	clk	6.803	6.803	Rise	clk
1	saida[0]	clk	6.982	6.982	Rise	clk
2	saida[1]	clk	6.838	6.838	Rise	clk
3	saida[2]	clk	6.830	6.830	Rise	clk
4	saida[3]	clk	6.953	6.953	Rise	clk
5	saida[4]	clk	6.803	6.803	Rise	clk
6	saida[5]	clk	6.960	6.960	Rise	clk
7	saida[6]	clk	6.836	6.836	Rise	clk
8	saida[7]	clk	6.834	6.834	Rise	clk

Exemplo 5 - adaptado (Wave Simulation - TestBench



Conclusão

1. O exemplo 5 é mais rápido que o exemplo 4 por executar a soma e subtração juntas no mesmo ciclo.
2. Entretanto, o exemplo usa dois somadores/subtratores, aumentando o custo do projeto.
3. A função do registrador P era de soltar a saída somente quando ela fosse final. Tirando esse registrador, o circuito libera a saída incompleta em cada ciclo, mas temos uma redução de área.
4. O registrador B tem uma entrada fixa, então outra possível diminuição de área acontece retirando ele e colocando a entrada direto no somador (contudo, teremos a problemática de: se colocarmos um valor diferente no meio da operação → gerar problema, ou seja, precisamos de um período de *clock* bem definido.

→ Logo, conseguimos retirar, aproximadamente, 25% da área total.

Implementação secundária

Além disso, o grupo tentou implementar uma nova ideia paralela às das aulas. Em que houve a realização do multiplicador com base no circuito proposto pela própria ferramenta do Quartus. No *import* das bibliotecas *numeric* tentou-se criar 4 estados os quais eram responsáveis, de primeiro momento, por:

-S0: Inicializar a FSM;

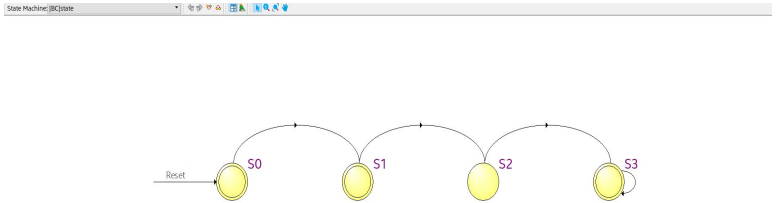
-S1: Receber as entradas ent1, ent2;

-S2: Multiplicá-las;

-S3: Repassar o resultado. *Loop* infinito até o *reset* para o estado S0.

Todavia, não foi adiante, já que o grupo consentiu em efetivar mudanças nos circuitos apresentados anteriormente. Entretanto, iremos apresentar algumas partes do circuito; sua prototipação.

FSM



RTL View