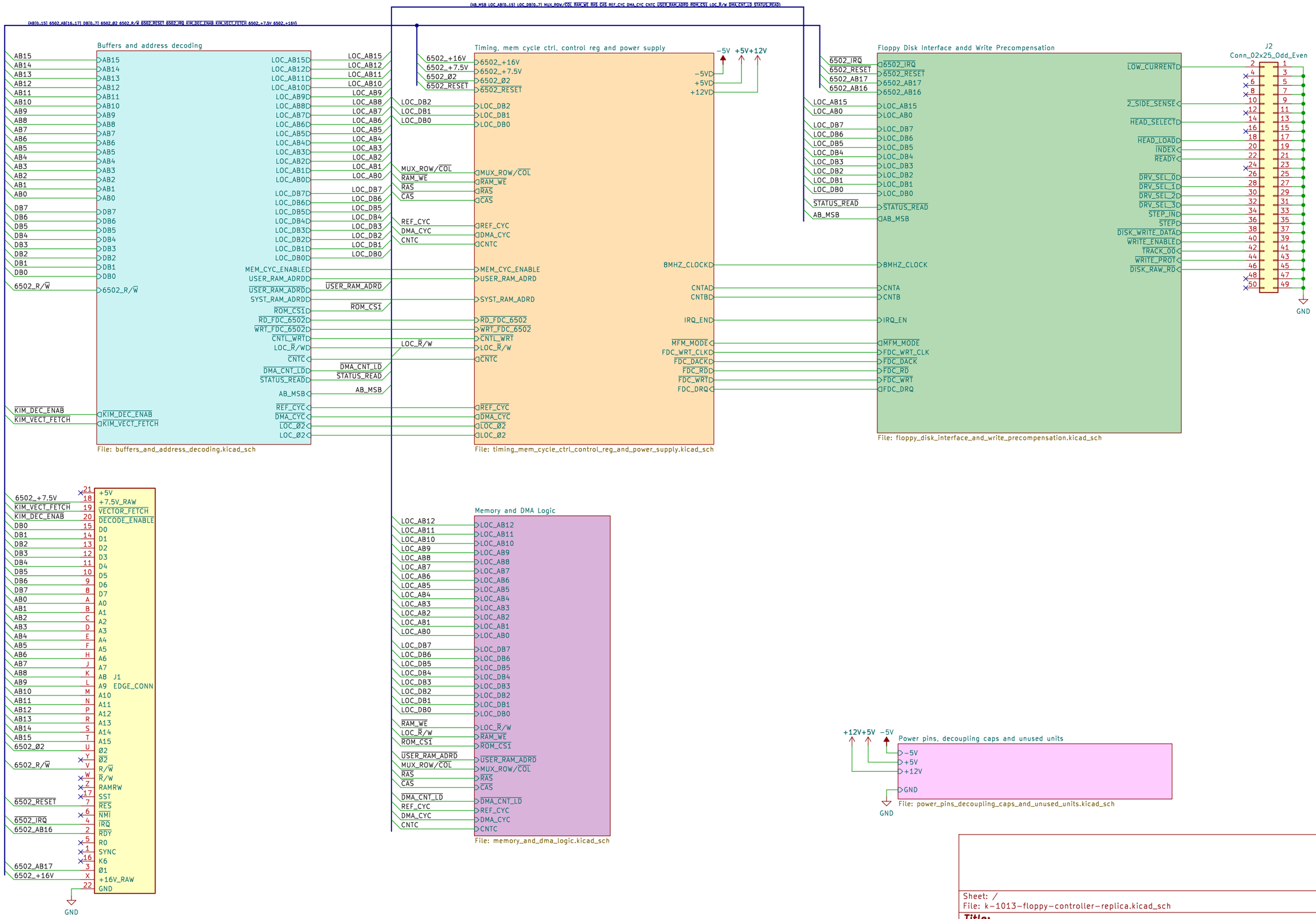
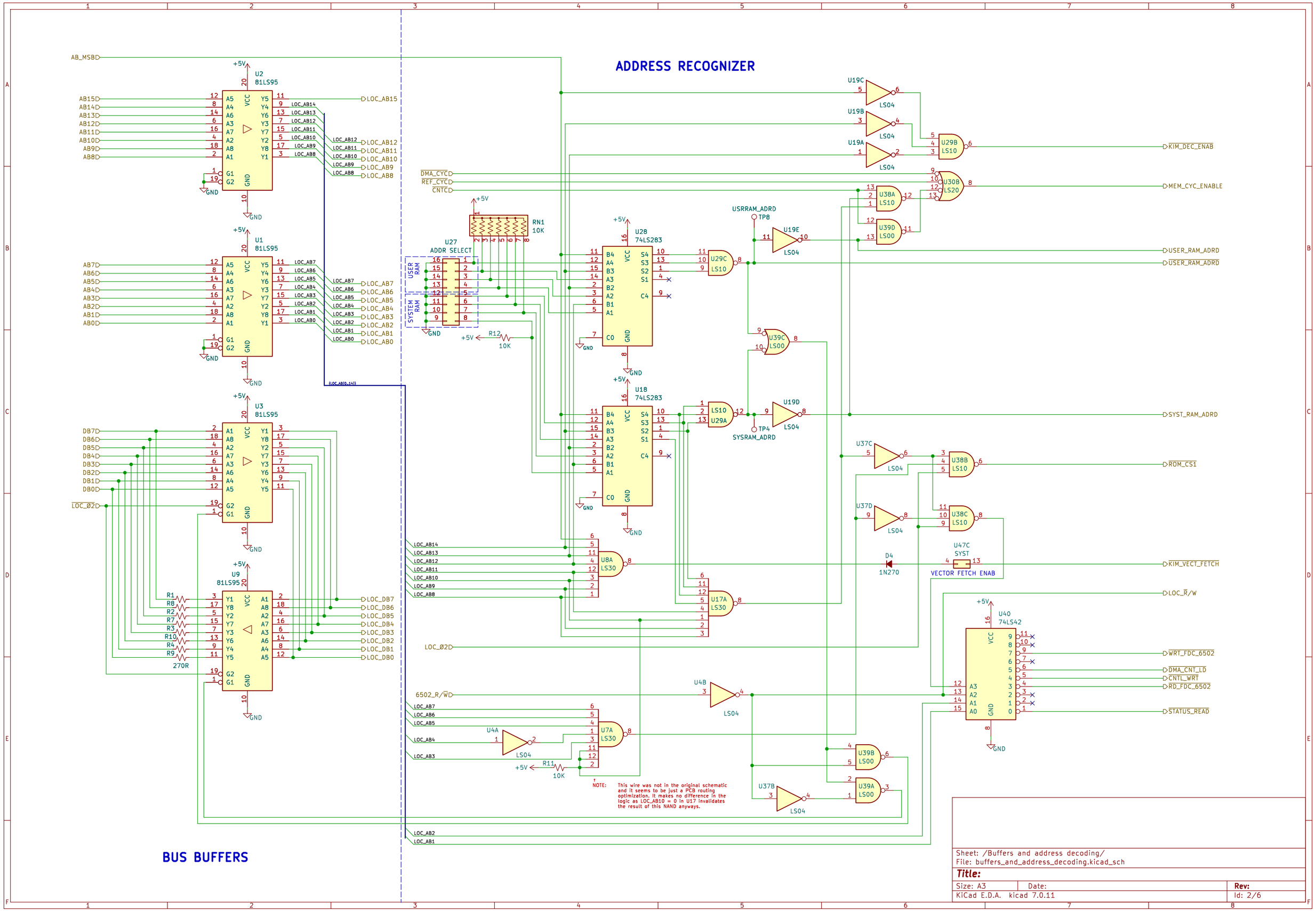
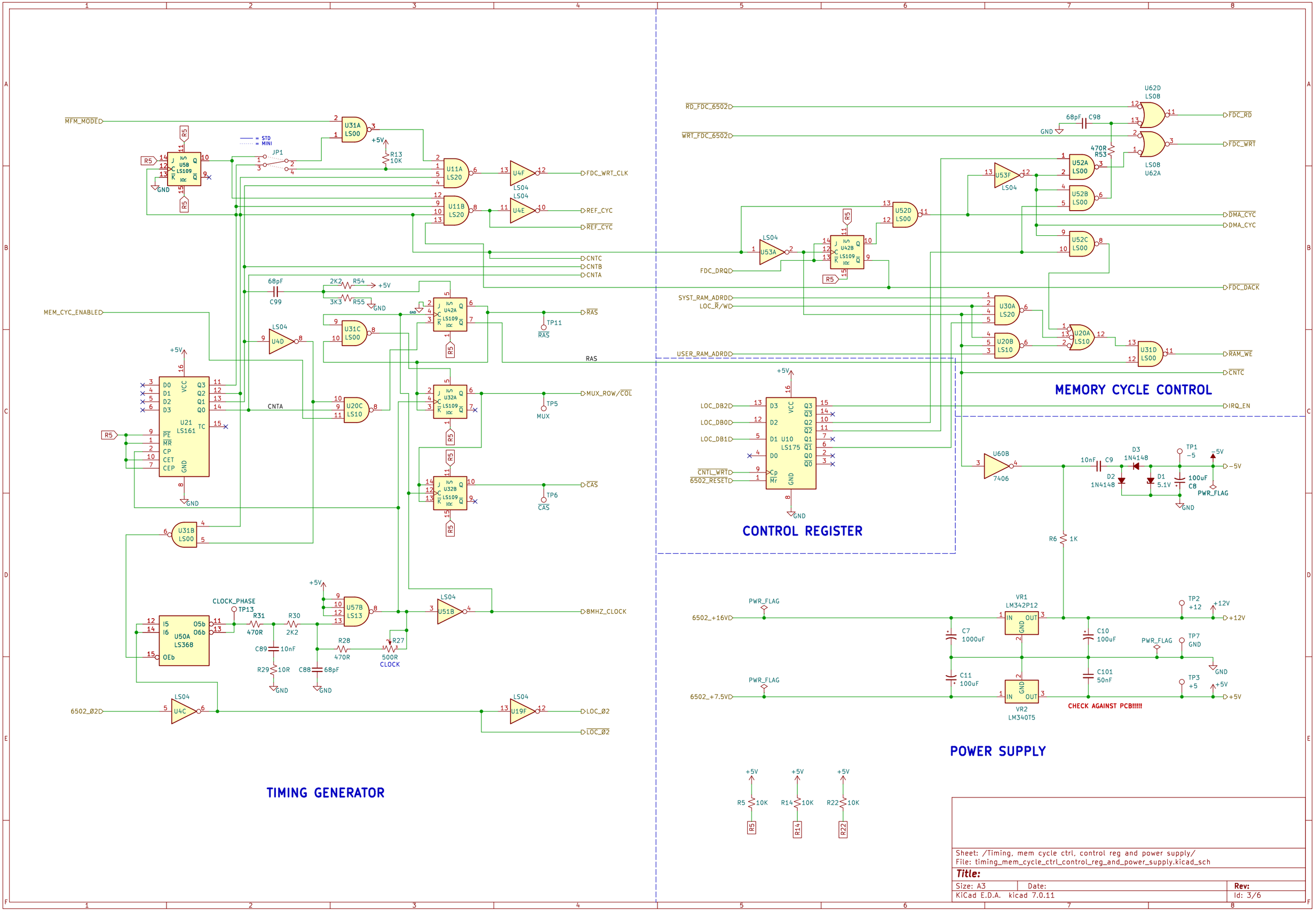

[AB[0..15] 6502_AB[16..17] DB[0..7] 6502_Ø2 6502_R/W 6502_RESET 6502_IRQ KIM_DEC_ENAB KIM_VECT_FETCH 6502_+7.5V 6502_+16V]
[AB_MSB LOC_AB[0..15] LOC_DB[0..7] MUX_ROW/COL RAM_WE RAS CAS REF_CYC DMA_CYC CNTC USER_RAM_ADRD ROM_CS1 LOC_R/W DMA_CNT_LD STATUS_READ]
Buffers and address decoding
File: buffers_and_address_decoding.kicad_sch
Timing, mem cycle ctrl, control reg and power supply
File: timing_mem_cycle_ctrl_control_reg_and_power_supply.kicad_sch
Floppy Disk Interface andd Write Precompensation
File: floppy_disk_interface_and_write_precompensation.kicad_sch
J2
Conn_02x25_Odd_Even
GND
J1
EDGE_CONN
Memory and DMA Logic
File: memory_and_dma_logic.kicad_sch
Power pins, decoupling caps and unused units
File: power_pins_decoupling_caps_and_unused_units.kicad_sch
Sheet: /
File: k-1013-floppy-controller-replica.kicad_sch
Title:
Size: A3
Date:
Rev:
KiCad E.D.A. kicad 7.0.11
Id: 1/6


ADDRESS RECOGNIZER
BUS BUFFERS
U2 81LS95
U1 81LS95
U3 81LS95
U9 81LS95
U27 ADDR SELECT
RN1 10K
U28 74LS283
U18 74LS283
U40 74LS42
U47C SYST VECTOR FETCH ENAB
D4 1N270
USRRAM_ADRD
SYSRAM_ADRD
KIM_DEC_ENAB
MEM_CYC_ENABLE
USER_RAM_ADRD
SYST_RAM_ADRD
ROM_CS1
KIM_VECT_FETCH
LOC_R/W
WRT_FDC_6502
DMA_CNT_LD
CNTL_WRT
RD_FDC_6502
STATUS_READ
NOTE: This wire was not in the original schematic and it seems to be just a PCB routing optimization. It makes no difference in the logic as LOC_AB10 = 0 in U17 invalidates the result of this NAND anyways.
Sheet: /Buffers and address decoding/
File: buffers_and_address_decoding.kicad_sch
Title:
Size: A3
Date:
Rev:
KiCad E.D.A. kicad 7.0.11
Id: 2/6


MEMORY CYCLE CONTROL
CONTROL REGISTER
POWER SUPPLY
TIMING GENERATOR
MFM_MODE
MEM_CYC_ENABLE
RD_FDC_6502
WRT_FDC_6502
FDC_DRQ
SYST_RAM_ADRD
LOC_R/WD
USER_RAM_ADRD
FDC_RD
FDC_WRT
DMA_CYC
FDC_DACK
RAM_WE
CNTC
IRQ_EN
FDC_WRT_CLK
REF_CYC
CNTB
CNTA
RAS
MUX_ROW/COL
CAS
8MHZ_CLOCK
LOC_Ø2
6502_Ø2
LOC_DB2
LOC_DB0
LOC_DB1
CNTL_WRT
6502_RESET
6502_+16V
6502_+7.5V
CLOCK_PHASE
CHECK AGAINST PCB!!!!!
Sheet: /Timing, mem cycle ctrl, control reg and power supply/
File: timing_mem_cycle_ctrl_control_reg_and_power_supply.kicad_sch
Title:
Size: A3
Date:
Rev:
KiCad E.D.A. kicad 7.0.11
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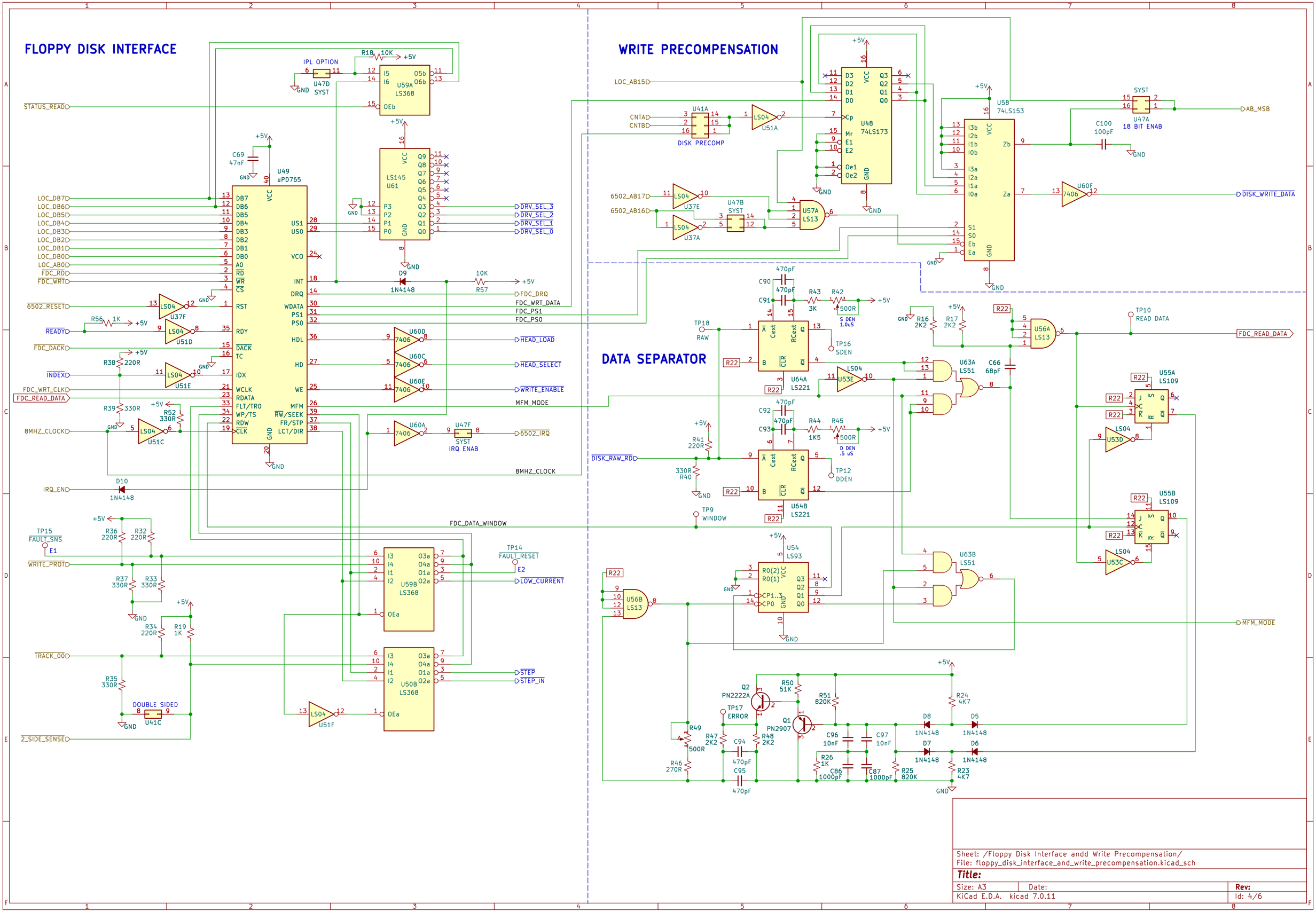
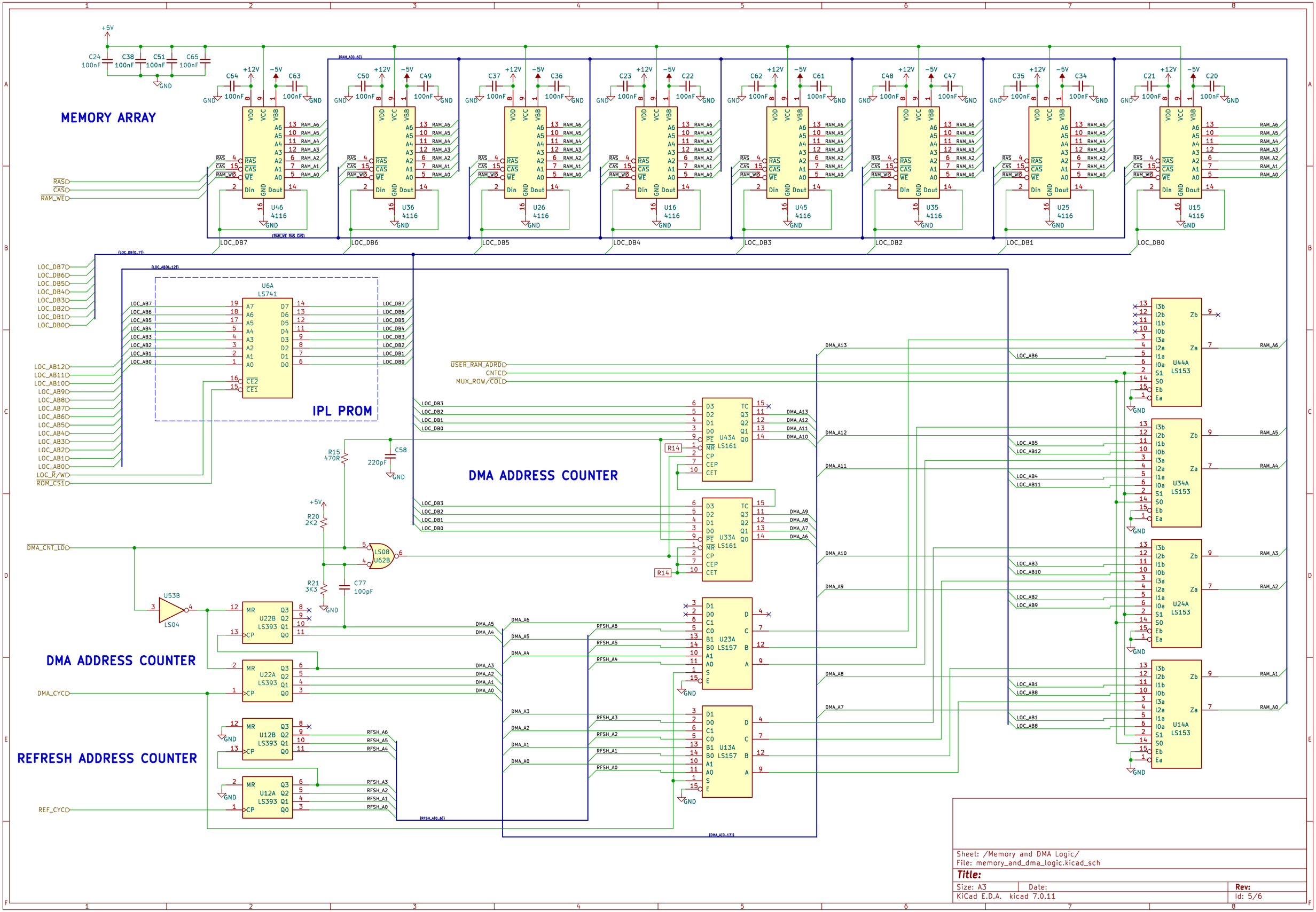
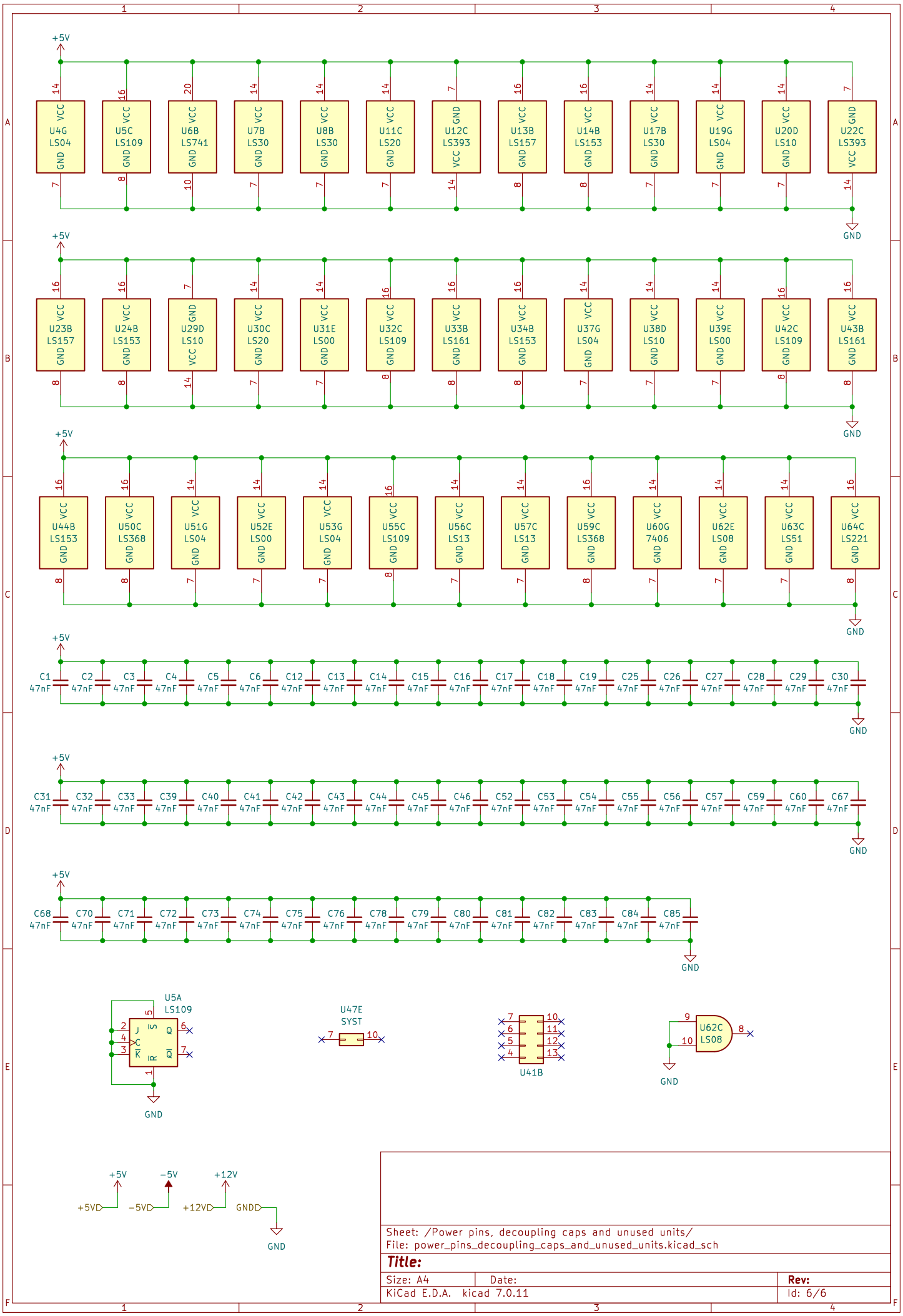

FLOPPY DISK INTERFACE
WRITE PRECOMPENSATION
DATA SEPARATOR
U49 uPD765
U59A LS368
U59B LS368
U50B LS368
U61 LS145
U48 74LS173
U58 74LS153
U54 LS93
U64A LS221
U64B LS221
U41A DISK PRECOMP
U47A 18 BIT ENAB
U47B SYST
U47D SYST
U47F SYST IRQ ENAB
U41C DOUBLE SIDED
U55A LS109
U55B LS109
U63A LS51
U63B LS51
U56A LS13
U56B LS13
U57A LS13
Q1 PN2907
Q2 PN2222A
STATUS_READ
LOC_AB15
CNTA
CNTB
6502_AB17
6502_AB16
LOC_DB7
LOC_DB6
LOC_DB5
LOC_DB4
LOC_DB3
LOC_DB2
LOC_DB1
LOC_DB0
LOC_AB0
FDC_RD
FDC_WRT
6502_RESET
READY
FDC_DACK
INDEX
FDC_WRT_CLK
FDC_READ_DATA
8MHZ_CLOCK
IRQ_EN
TP15 FAULT_SNS
WRITE_PROT
TRACK_00
2_SIDE_SENSE
DRV_SEL_3
DRV_SEL_2
DRV_SEL_1
DRV_SEL_0
FDC_DRQ
FDC_WRT_DATA
FDC_PS1
FDC_PS0
HEAD_LOAD
HEAD_SELECT
WRITE_ENABLE
MFM_MODE
6502_IRQ
8MHZ_CLOCK
FDC_DATA_WINDOW
TP14 FAULT_RESET
LOW_CURRENT
STEP
STEP_IN
AB_MSB
DISK_WRITE_DATA
FDC_READ_DATA
DISK_RAW_RD
TP18 RAW
TP16 SDEN
TP12 DDEN
TP9 WINDOW
TP10 READ DATA
TP17 ERROR
S DEN 1.0uS
D DEN .5 uS
C100 100pF
C66 68pF
R16 2K2
R17 2K2
R57 10K
R18 10K
R56 1K
R38 220R
R39 330R
R52 330R
R36 220R
R32 220R
R37 330R
R33 330R
R34 220R
R19 1K
R35 330R
R41 220R
R40 330R
R43 3K
R42 500R
R44 1K5
R45 500R
R46 270R
R47 2K2
R48 2K2
R49 500R
R50 51K
R51 820K
R24 4K7
R23 4K7
R25 820K
R26 1K
C69 47nF
C90 470pF
C91 470pF
C92 470pF
C93 470pF
C94 470pF
C95 470pF
C96 10nF
C97 10nF
C86 1000pF
C87 1000pF
D9 1N4148
D10 1N4148
D8 1N4148
D5 1N4148
D7 1N4148
D6 1N4148
Sheet: /Floppy Disk Interface andd Write Precompensation/
File: floppy_disk_interface_and_write_precompensation.kicad_sch
Title:
Size: A3
Date:
Rev:
KiCad E.D.A. kicad 7.0.11
Id: 4/6


MEMORY ARRAY
IPL PROM
DMA ADDRESS COUNTER
DMA ADDRESS COUNTER
REFRESH ADDRESS COUNTER
U46 4116
U36 4116
U26 4116
U16 4116
U45 4116
U35 4116
U25 4116
U15 4116
U6A LS741
U43A LS161
U33A LS161
U23A LS157
U13A LS157
U44A LS153
U34A LS153
U24A LS153
U14A LS153
U22B LS393
U22A LS393
U12B LS393
U12A LS393
U53B LS04
LS08 U62B
R15 470R
R20 2K2
R21 3K3
C58 220pF
C77 100pF
R14
USER_RAM_ADRD
CNTC
MUX_ROW/COL
DMA_CNT_LD
DMA_CYC
REF_CYC
LOC_R/W
ROM_CS1
RAS
CAS
RAM_WE
Sheet: /Memory and DMA Logic/
File: memory_and_dma_logic.kicad_sch
Title:
Size: A3
Date:
Rev:
KiCad E.D.A. kicad 7.0.11
Id: 5/6



Sheet: /Power pins, decoupling caps and unused units/
File: power_pins_decoupling_caps_and_unused_units.kicad_sch

Title:

Size: A4	Date:	Rev:
KiCad E.D.A. kicad 7.0.11		Id: 6/6