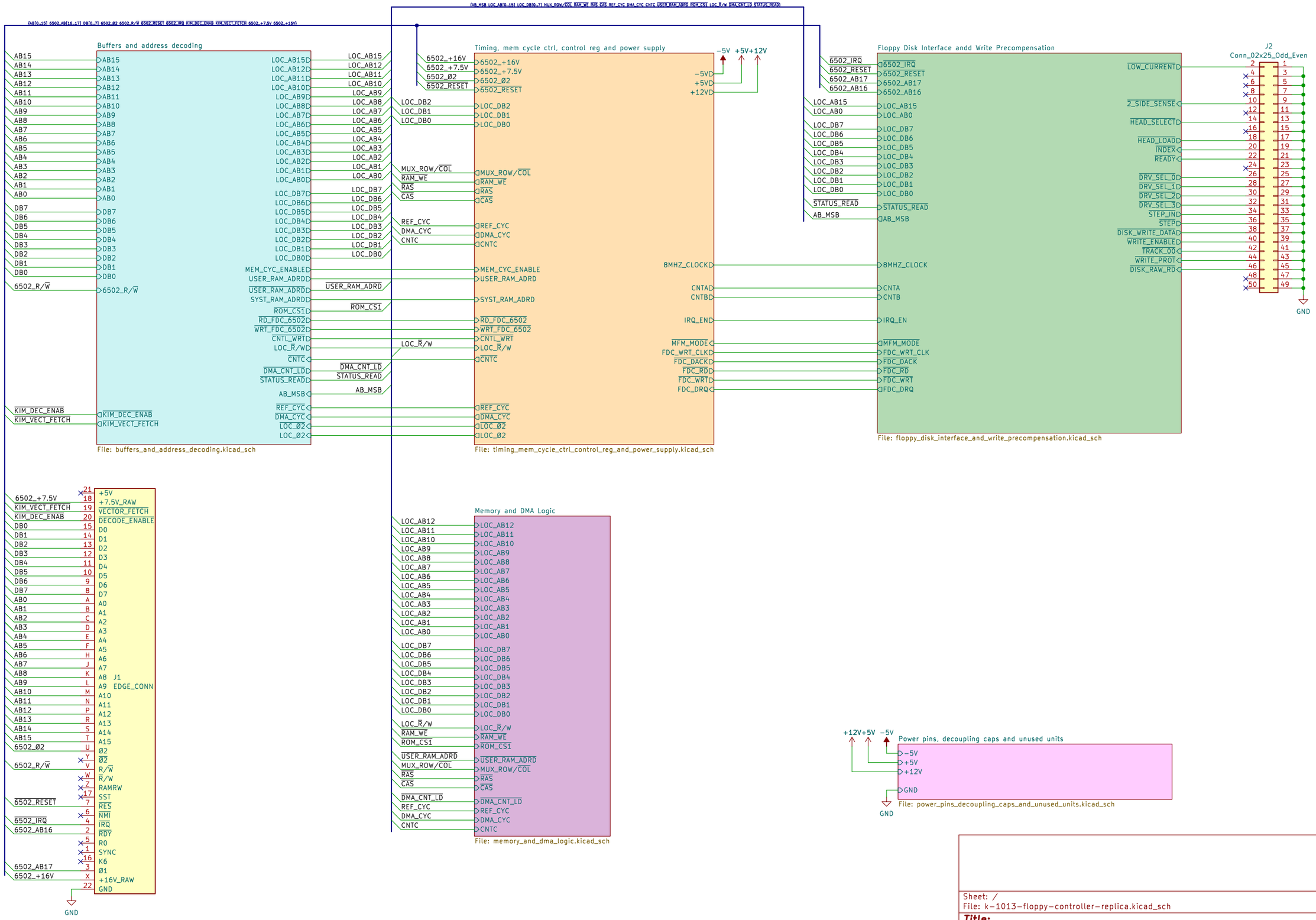
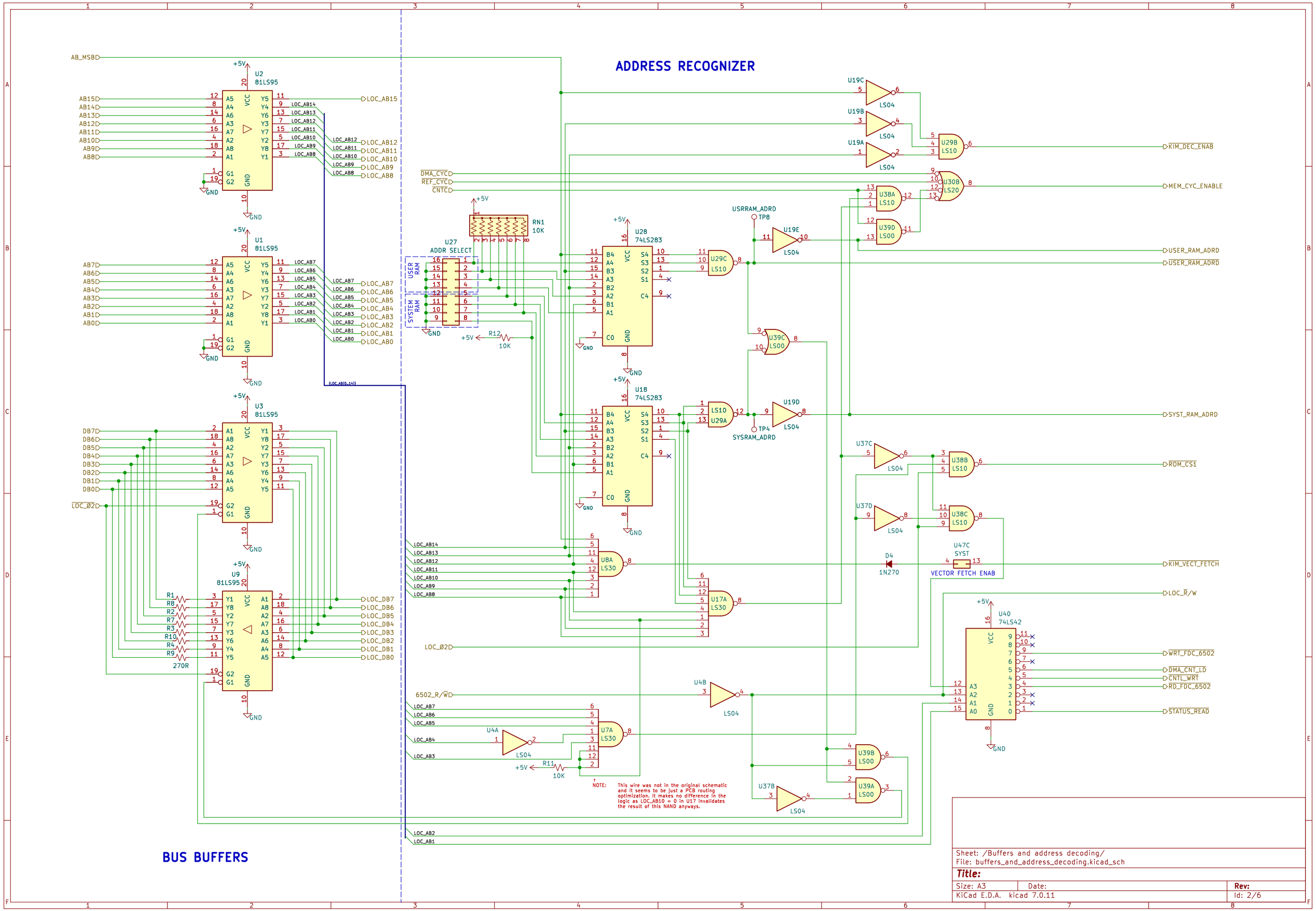
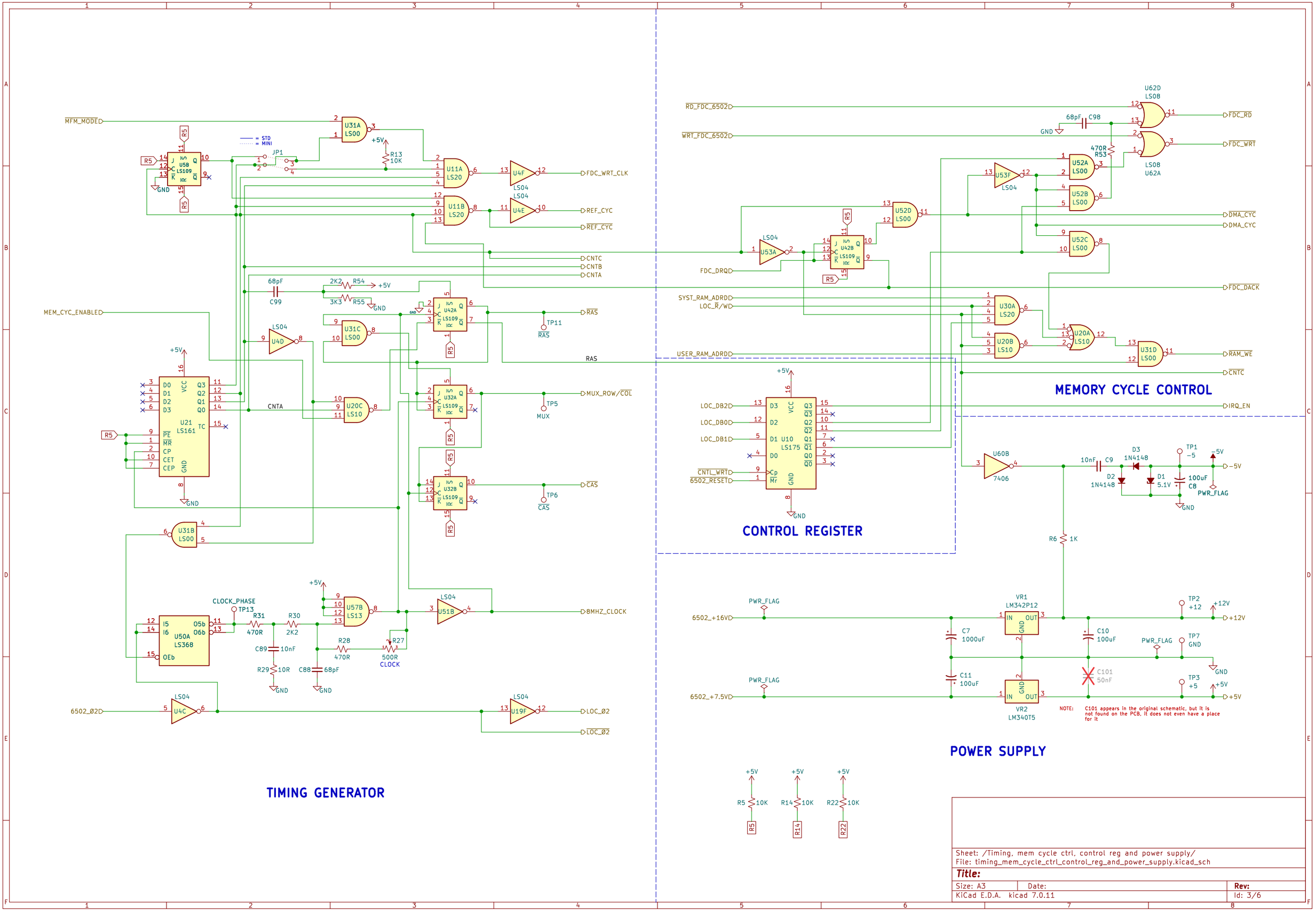
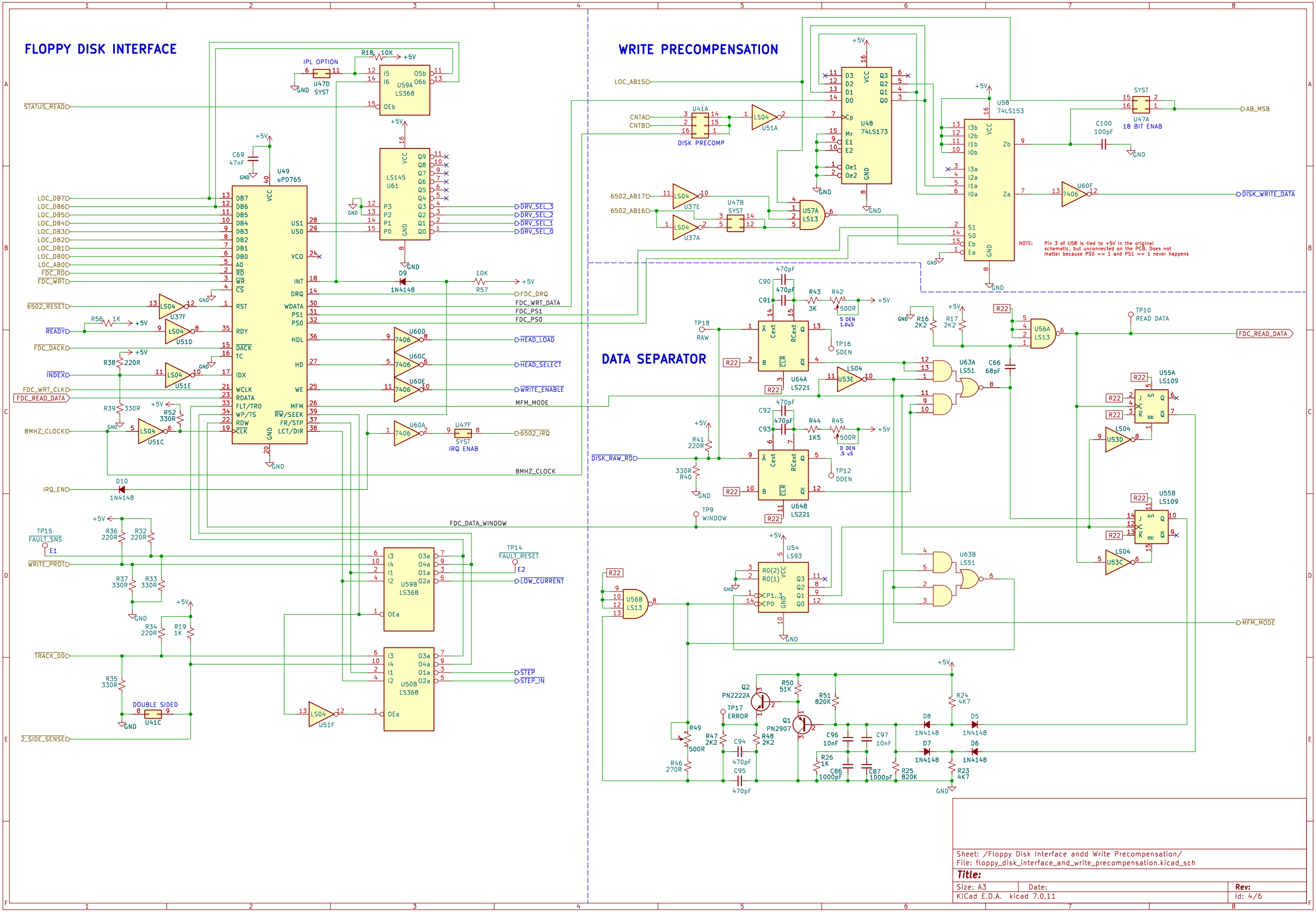

[AB[0..15] 6502_AB[16..17] DB[0..7] 6502_Ø2 6502_R/W 6502_RESET 6502_IRQ KIM_DEC_ENAB KIM_VECT_FETCH 6502_+7.5V 6502_+16V]
[AB_MSB LOC_AB[0..15] LOC_DB[0..7] MUX_ROW/COL RAM_WE RAS CAS REF_CYC DMA_CYC CNTC USER_RAM_ADRD ROM_CS1 LOC_R/W DMA_CNT_LD STATUS_READ]
Buffers and address decoding
File: buffers_and_address_decoding.kicad_sch
Timing, mem cycle ctrl, control reg and power supply
File: timing_mem_cycle_ctrl_control_reg_and_power_supply.kicad_sch
Floppy Disk Interface andd Write Precompensation
File: floppy_disk_interface_and_write_precompensation.kicad_sch
J2
Conn_02x25_Odd_Even
GND
J1
EDGE_CONN
Memory and DMA Logic
File: memory_and_dma_logic.kicad_sch
Power pins, decoupling caps and unused units
File: power_pins_decoupling_caps_and_unused_units.kicad_sch
Sheet: /
File: k-1013-floppy-controller-replica.kicad_sch
Title:
Size: A3
Date:
Rev:
KiCad E.D.A. kicad 7.0.11
Id: 1/6


ADDRESS RECOGNIZER
BUS BUFFERS
U2 81LS95
U1 81LS95
U3 81LS95
U9 81LS95
U27 ADDR SELECT
RN1 10K
U28 74LS283
U18 74LS283
U40 74LS42
U47C SYST VECTOR FETCH ENAB
D4 1N270
USRRAM_ADRD
SYSRAM_ADRD
KIM_DEC_ENAB
MEM_CYC_ENABLE
USER_RAM_ADRD
SYST_RAM_ADRD
ROM_CS1
KIM_VECT_FETCH
LOC_R/W
WRT_FDC_6502
DMA_CNT_LD
CNTL_WRT
RD_FDC_6502
STATUS_READ
NOTE: This wire was not in the original schematic and it seems to be just a PCB routing optimization. It makes no difference in the logic as LOC_AB10 = 0 in U17 invalidates the result of this NAND anyways.
Sheet: /Buffers and address decoding/
File: buffers_and_address_decoding.kicad_sch
Title:
Size: A3
Date:
Rev:
KiCad E.D.A. kicad 7.0.11
Id: 2/6

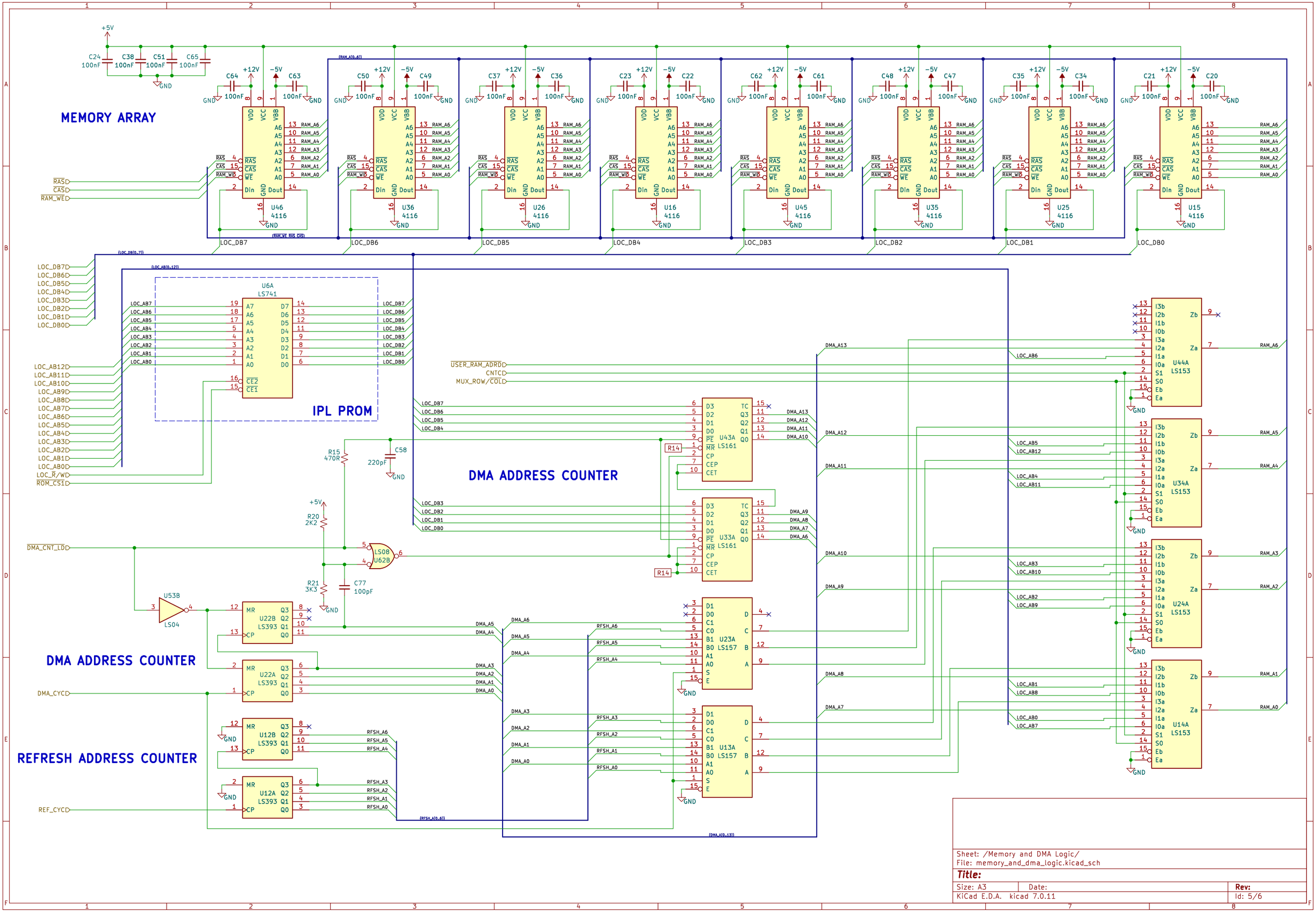

MEMORY CYCLE CONTROL
CONTROL REGISTER
POWER SUPPLY
TIMING GENERATOR
MFM_MODE
MEM_CYC_ENABLED
RD_FDC_6502
WRT_FDC_6502
FDC_DRQ
SYST_RAM_ADRD
LOC_R/WD
USER_RAM_ADRD
FDC_RD
FDC_WRT
DMA_CYC
FDC_DACK
RAM_WE
CNTC
IRQ_EN
FDC_WRT_CLK
REF_CYC
CNTB
CNTA
RAS
MUX_ROW/COL
CAS
8MHZ_CLOCK
LOC_Ø2
6502_Ø2
LOC_DB2
LOC_DB0
LOC_DB1
CNTL_WRT
6502_RESET
6502_+16V
6502_+7.5V
PWR_FLAG
CLOCK_PHASE
NOTE: C101 appears in the original schematic, but it is not found on the PCB, it does not even have a place for it
Sheet: /Timing, mem cycle ctrl, control reg and power supply/
File: timing_mem_cycle_ctrl_control_reg_and_power_supply.kicad_sch
Title:
Size: A3
Date:
Rev:
KiCad E.D.A. kicad 7.0.11
Id: 3/6

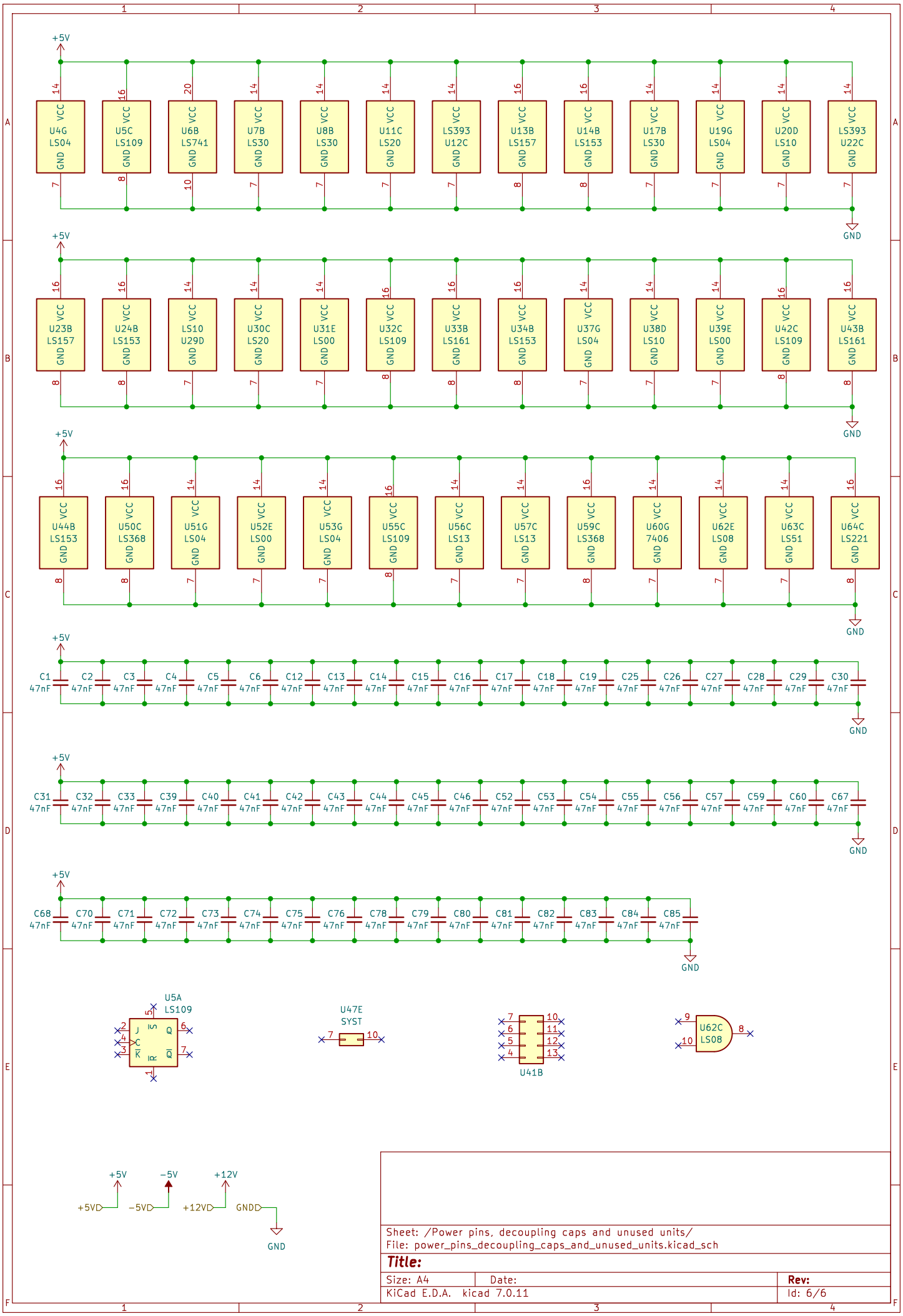


Sheet: /Floppy Disk Interface andd Write Precompensation/
File: floppy_disk_interface_and_write_precompensation.kicad_sch

Title:

Size: A3	Date:	Rev:
KiCad E.D.A. kicad 7.0.11		Id: 4/6


MEMORY ARRAY
IPL PROM
DMA ADDRESS COUNTER
DMA ADDRESS COUNTER
REFRESH ADDRESS COUNTER
U46 4116
U36 4116
U26 4116
U16 4116
U45 4116
U35 4116
U25 4116
U15 4116
U6A LS741
U43A LS161
U33A LS161
U23A LS157
U13A LS157
U44A LS153
U34A LS153
U24A LS153
U14A LS153
U22B LS393
U22A LS393
U12B LS393
U12A LS393
U53B LS04
LS08 U62B
Sheet: /Memory and DMA Logic/
File: memory_and_dma_logic.kicad_sch
Title:
Size: A3
Date:
Rev:
KiCad E.D.A. kicad 7.0.11
Id: 5/6



Sheet: /Power pins, decoupling caps and unused units/
File: power_pins_decoupling_caps_and_unused_units.kicad_sch

Title:

Size: A4	Date:	Rev:
KiCad E.D.A. kicad 7.0.11		Id: 6/6