Eduardo Diaz

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Education

University of California, Berkeley — Berkeley, CA
Bachelor of Science in Electrical Engineering and Computer Sciences — *Expected: Dec. 2021*

Experience

Modern Digital Logic Design Internship — Nov. 2018 – Jan. 2019
Hartnell College Physics Department — *Salinas, CA*

- Developed and designed a 7-segment LED counting display using Verilog and an Altera Cyclone II FPGA.
- Performed analysis of hardware using Quartus II and ModelSim.
- Began to integrate the project with Cosmic Ray Detector to count coincidences.

Organic and Perovskite Photovoltaics Internship — June 2018 – Aug. 2018
Hartnell College Physics Department — *Salinas, CA*

- Created and tested Organic and Perovskite solar cells and compared their respective efficiency.
- Investigated and analyzed the elements present in the Perovskite cell using a spectrometer.

Society of Hispanic Professional Engineers Student Chapter, President — Aug. 2018 – May 2019
Hartnell College — *Salinas, CA*

- Oversaw all SHPE Hartnell Chapter activities.
- Presided over all chapter meetings and gatherings.
- Prepared reports for the SHPE National Report Program.

Projects

Lingua Franca on NRF | *Lingua Franca, C, Git*

- Lingua Franca (LF) is a coordination meta-language, based on an actor model. Code is written in a mix of LF syntax and the host language (in our case, C), compiled to the host language, and then run on the target architecture. Before this project, the C runtime of LF was only supported on Linux, MacOS, and Windows, with no support for embedded platforms. The main goal was to port and demonstrate usage of LF on the nRF52832 SoC.

RISCV151 | *Verilog, VCS, Vivado, Git*

- Designed and implemented a 3-stage pipelined RISC-V CPU with UART for tethering and integrated I/O.
- Programmed the CPU to run on the Xilinx Pynq Platform with a Zynq 7000-series FPGA.
- Optimized the CPU to run at 70MHz while also reducing the FPGA resource utilization for LUTs and SLICE Registers (to about 4% and 0.85% respectively).

BYOW | *Java, Git*

- Designed and implemented an engine for generating 2D tile-based explorable worlds.
- The worlds were pseudorandomly generated using a seed entered by the user.
- Implemented interactivity and a user interface which allowed the user to explore the generated world.
- Added the option to save movements made as well as load and replay a previously saved game.

Relevant Coursework (* = in progress)

EECS 149: Introduction to Embedded Systems *
EECS 151LA: Application Specific Integrated Circuits Lab *
EECS 151: Introduction to Digital Design and Integrated Circuits
EECS 151LB: Field Programmable Gate Array Lab
EE 120: Signals and Systems
CS 194-015: Parallel Programming *
CS 161: Computer Security
CS 61B: Data Structures
CS 61C: Great Ideas in Computer Architecture

Technical Skills

Languages: C/C++, Verilog, RISC-V, Java, Python
Developer Tools: Git, Synopsys VCS, Cadence Genus/Innovus
Libraries: OpenMP, NumPy, Matplotlib
Hardware: nRF52832 SoC, Xilinx FPGA, Arduino