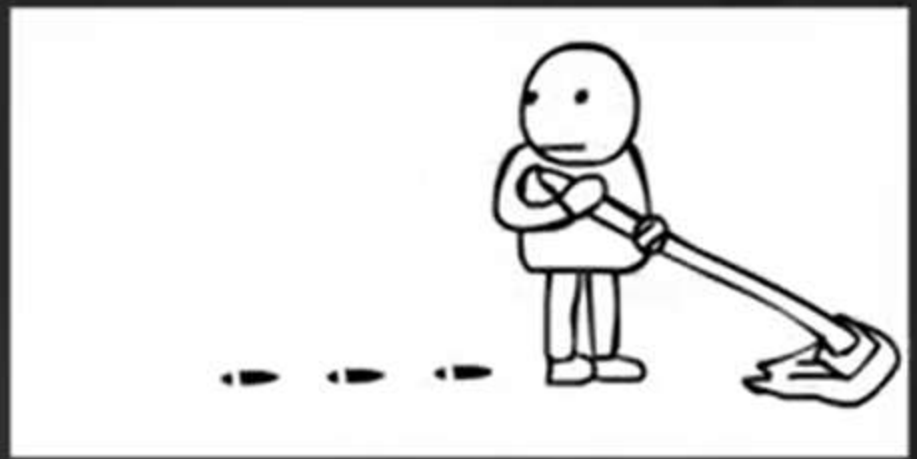
Instituto Tecnológico de Zitácuaro

Tema 6:
Interrupciones

Interrupciones

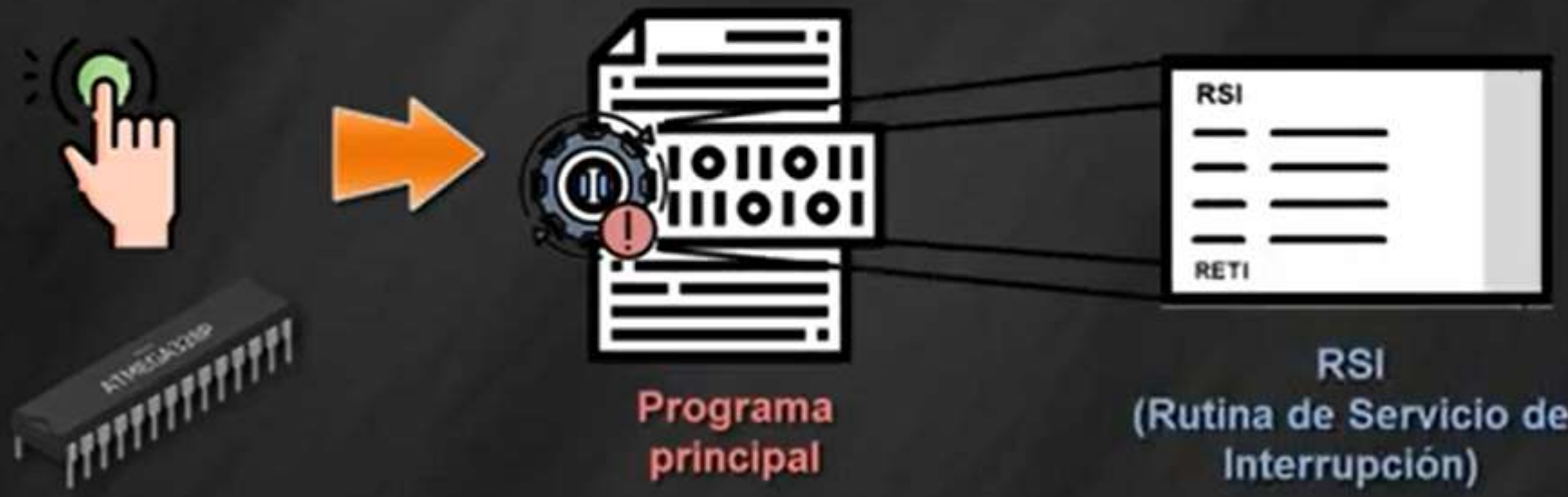
Interrupciones



Interrupciones

Interrupciones

Son eventos que hacen al microcontrolador suspender la ejecución del programa principal y ejecutar un programa secundario conocido como RSI.



Interrupciones

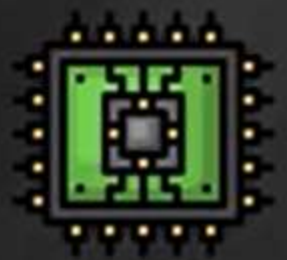
Son eventos que hacen al microcontrolador suspender la ejecución del programa principal y ejecutar un programa secundario conocido como RSI.

Programa principal

Hardware

¿Qué puede provocar una interrupción?

- La forma de trabajo de algunos periféricos.



ADC

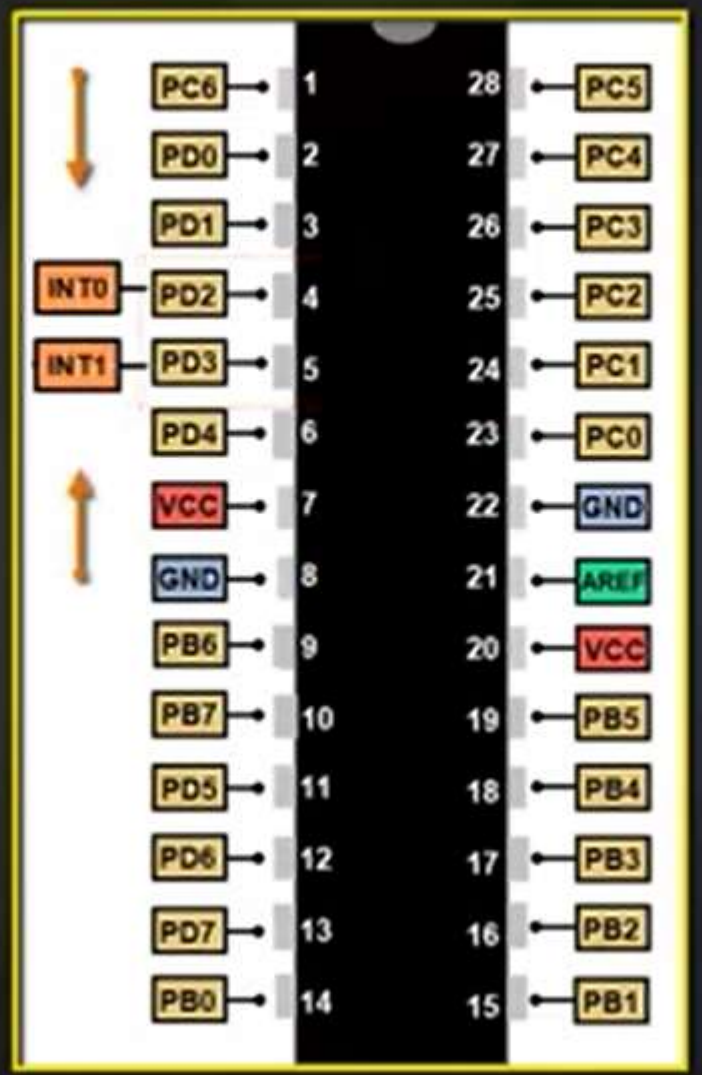
USART

¿Qué puede provocar una interrupción?

- La forma de trabajo de algunos periféricos.

- Eventos externos monitoreados en los pines correspondientes.

Pines para monitorear interrupciones



Instrucciones básicas para trabajar con interrupciones

SEI

Habilita las interrupciones globales.

Cuando se activa pone en uno la bandera I

I

Registro de Estado

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
I	T	H	S	V	N	Z	T
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0

Instrucciones básicas para trabajar con interrupciones

SEI

Habilita las interrupciones globales.

Cuando se ejecuta una interrupción el registro I se pone en cero

Registro de Estado

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
I	T	H	S	V	N	Z	T
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0

Instrucciones básicas para trabajar con interrupciones

SEI

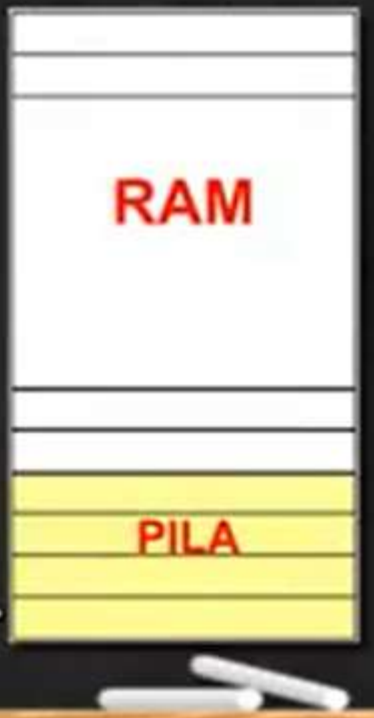
Habilita las interrupciones globales.

I

Vector de interrupción

PC

Dirección de retorno



Instrucciones básicas para trabajar con interrupciones

SEI

Habilita las interrupciones globales.

RETI

Retorno de interrupción.

Table 11-1. Reset and Interrupt Vectors in ATmega328P

Vector No.	Program Address	Source	Interrupt Definition
1	0x0000	RESET	External pin, power-on reset, brown-out reset and watchdog system reset
2	0x0002	INT0	External interrupt request 0
3	0x0004	INT1	External interrupt request 1
4	0x0006	PCINT0	Pin change interrupt request 0
5	0x0008	PCINT1	Pin change interrupt request 1
6	0x000A	PCINT2	Pin change interrupt request 2
7	0x000C	WDT	Watchdog time-out interrupt
8	0x000E	TIMER2 COMPA	Timer/Counter2 compare match A
9	0x0010	TIMER2 COMPB	Timer/Counter2 compare match B
10	0x0012	TIMER2 OVF	Timer/Counter2 overflow
11	0x0014	TIMER1 CAPT	Timer/Counter1 capture event
12	0x0016	TIMER1 COMPA	Timer/Counter1 compare match A
13	0x0018	TIMER1 COMPB	Timer/Counter1 compare match B
14	0x001A	TIMER1 OVF	Timer/Counter1 overflow
15	0x001C	TIMER0 COMPA	Timer/Counter0 compare match A
16	0x001E	TIMER0 COMPB	Timer/Counter0 compare match B
17	0x0020	TIMER0 OVF	Timer/Counter0 overflow
18	0x0022	SPI, STC	SPI serial transfer complete
19	0x0024	USART, RX	USART Rx complete
20	0x0026	USART, UDRE	USART, data register empty
21	0x0028	USART, TX	USART, Tx complete
22	0x002A	ADC	ADC conversion complete
23	0x002C	EE READY	EEPROM ready
24	0x002E	ANALOG COMP	Analog comparator
25	0x0030	TWI	2-wire serial interface
26	0x0032	SPM READY	Store program memory ready

Direcciones para Timer

Table 11-1. Reset and Interrupt Vectors in ATmega328P

Vector No.	Program Address	Source	Interrupt Definition
1	0x0000	RESET	External pin, power-on reset, brown-out reset and watchdog system reset
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11	0x0014	TIMER1 CAPT	Timer/Counter1 capture event
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18	0x0022	SPI, STC	SPI serial transfer complete
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Módulo USART

Table 11-1. Reset and Interrupt Vectors in ATmega328P

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15	0x001C	TIMER0 COMPA	Timer/Counter0 compare match A
16	0x001E	TIMER0 COMPB	Timer/Counter0 compare match B
17	0x0020	TIMER0 OVF	Timer/Counter0 overflow
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Convertidor de Analógico a Digital

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Interrupciones Externas

Table 11-1. Reset and Interrupt Vectors in ATmega328P

Vector No.	Program Address	Source	Interrupt Definition
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15	0x001C	TIMER0 COMPA	Timer/Counter0 compare match A
16	0x001E	TIMER0 COMPB	Timer/Counter0 compare match B
17	0x0020	TIMER0 OVF	Timer/Counter0 overflow
18	0x0022	SPI, STC	SPI serial transfer complete
19	0x0024	USART, RX	USART Rx complete
20	0x0026	USART, UDRE	USART, data register empty
21	0x0028	USART, TX	USART, Tx complete
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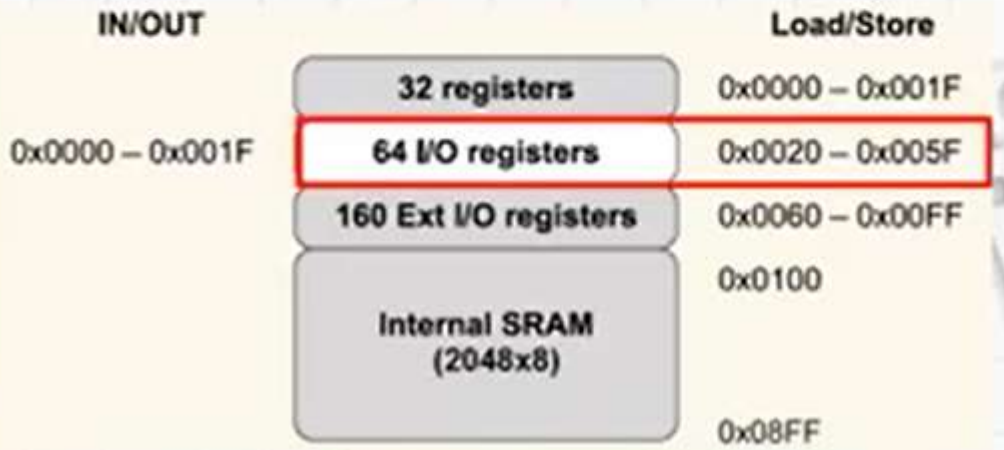
26	0x0032	SPM READY	Store program memory ready

Registros para configurar interrupciones externas

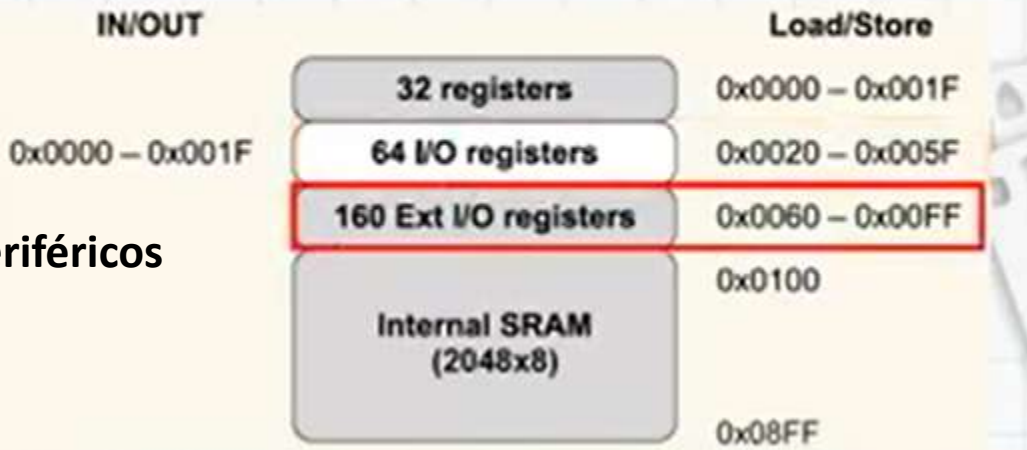
Registro	Dirección
EIFR	0X1C
EIMSK	0X1D
EICRA	0X69

Registro	Dirección
EIFR	0X1C
EIMSK	0X1D
EICRA	0X69



Se debe tomar en cuenta que hay memoria de periféricos de Entrada y Salida con su dirección de memoria

Registro	Dirección
EIFR	0X1C
EIMSK	0X1D
EICRA	0X69



También hay memoria de periféricos extendida

TABLA DE REGISTROS DE CONFIGURACIÓN MAPEADOS EN RAM

I/O Memory

REGISTRO	DIR	REGISTRO	DIR
PINB	0x03	OCR0A	0x27
DDRB	0x04	OCR0B	0x28
PORTB	0x05	GPIOR1	0x2a
PINC	0x06	GPIOR2	0x2b
DDRC	0x07	SPCR	0x2c
PORTC	0x08	SPSR	0x2d
PIND	0x09	SPDR	0x2e
DDRD	0x0a	ACSR	0x30
PORTD	0x0b	SMCR	0x33
TIFR0	0x15	MCUSR	0x34
TIFR1	0x16	MCUCR	0x35
TIFR2	0x17	SPMCSR	0x37
PCIFR	0x1b	SPL	0x3d
EIFR	0x1c	SPH	0x3e
EIMSK	0x1d	SREG	0x3f
GPIOR0	0x1e		
EECR	0x1f		
EEDR	0x20		
EEARL	0x21		
EEARH	0x22		
GTCCR	0x23		
TCCR0A	0x24		
TCCR0B	0x25		
TCNT0	0x26		

Extended I/O Memory

REGISTRO	DIR	REGISTRO	DIR
WDTCSR	0x60	ICR1L	0x86
CLKPR	0x61	ICR1H	0x87
PRR	0x64	OCR1AL	0x88
OSCCAL	0x66	OCR1AH	0x89
PCICR	0x68	OCR1BL	0x8a
EICRA	0x69	OCR1BH	0x8b
PCMSK0	0x6b	TCCR2A	0xb0
PCMSK1	0x6c	TCCR2B	0xb1
PCMSK2	0x6d	TCNT2	0xb2
TIMSK0	0x6e	OCR2A	0xb3
TIMSK1	0x6f	OCR2B	0xb4
TIMSK2	0x70	ASSR	0xb6
ADCL	0x78	TWBR	0xb8
ADCH	0x79	TWSR	0xb9
ADCSRA	0x7a	TWAR	0xba
ADCSRB	0x7b	TWDR	0xbb
ADMUX	0x7c	TWCR	0xbc
DIDR0	0x7e	TWAMR	0xbd
DIDR1	0x7f	UCSR0A	0xc0
TCCR1A	0x80	UCSR0B	0xc1
TCCR1B	0x81	UCSR0C	0xc2
TCCR1C	0x82	UBRR0L	0xc4
TCNT1L	0x84	UBRR0H	0xc5
TCNT1H	0x85	UDR0	0xc6

IN

OUT

TABLA DE REGISTROS DE CONFIGURACION MAPEADOS EN RAM

I/O Memory

REGISTRO	DIR	REGISTRO	DIR
PINB	0x03	OCR0A	0x27
DDRB	0x04	OCR0B	0x28
PORTB	0x05	GPIOR1	0x2a
PINC	0x06	GPIOR2	0x2b
DDRC	0x07	SPCR	0x2c
PORTC	0x08	SPSR	0x2d
PIND	0x09	SPDR	0x2e
DDRD	0x0a	ACSR	0x30
PORTD	0x0b	SMCR	0x33
TIFR0	0x15	MCUSR	0x34
TIFR1	0x16	MCUCR	0x35
TIFR2	0x17	SPMCSR	0x37
PCIFR	0x1b	SPL	0x3d
EIFR	0x1c	SPH	0x3e
EIMSK	0x1d	SREG	0x3f
GPIOR0	0x1e		
EECR	0x1f		
EEDR	0x20		
EEARL	0x21		
EEARH	0x22		
GTCCR	0x23		
TCCR0A	0x24		
TCCR0B	0x25		
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PCMSK1	0x6c	TCCR2B	0xb1
PCMSK2	0x6d	TCNT2	0xb2
TIMSK0	0x6e	OCR2A	0xb3
TIMSK1	0x6f	OCR2B	0xb4
TIMSK2	0x70	ASSR	0xb6
ADCL	0x78	TWBR	0xb8
ADCH	0x79	TWSR	0xb9
ADCSRA	0x7a	TWAR	0xba
ADCSRB	0x7b	TWDR	0xbb
ADMUX	0x7c	TWCR	0xbc
DIDR0	0x7e	TWAMR	0xbd
DIDR1	0x7f	UCSR0A	0xc0
TCCR1A	0x80	UCSR0B	0xc1
TCCR1B	0x81	UCSR0C	0xc2
TCCR1C	0x82	UBRR0L	0xc4
TCNT1L	0x84	UBRR0H	0xc5
TCNT1H	0x85	UDR0	0xc6

IN

OUT

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PORTC	0x08	SPSR	0x2d
PIND	0x09	SPDR	0x2e
DDRD	0x0a	ACSR	0x30
PORTD	0x0b	SMCR	0x33
TIFR0	0x15	MCUSR	0x34
TIFR1	0x16	MCUCR	0x35
TIFR2	0x17	SPMCSR	0x37
PCIFR	0x1b	SPL	0x3d
EIFR	0x1c	SPH	0x3e
EIMSK	0x1d	SREG	0x3f
GPIOR0	0x1e		
EECR	0x1f		
EEDR	0x20		
EEARL	0x21		
EEARH	0x22		
GTCCR	0x23		
TCCR0A	0x24		
TCCR0B	0x25		
TCNT0	0x26		

Extended I/O Memory

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PRR	0x64	OCR1AL	0x88
OSCCAL	0x66	OCR1AH	0x89
PCICR	0x68	OCR1BL	0x8a
EICRA	0x69	OCR1BH	0x8b
PCMSK0	0x6b	TCCR2A	0xb0
PCMSK1	0x6c	TCCR2B	0xb1
PCMSK2	0x6d	TCNT2	0xb2
TIMSK0	0x6e	OCR2A	0xb3
TIMSK1	0x6f	OCR2B	0xb4
TIMSK2	0x70	ASSR	0xb6
ADCL	0x78	TWBR	0xb8
ADCH	0x79	TWSR	0xb9
ADCSRA	0x7a	TWAR	0xba
ADCSRB	0x7b	TWDR	0xbb
ADMUX	0x7c	TWCR	0xbc
DIDR0	0x7e	TWAMR	0xbd
DIDR1	0x7f	UCSR0A	0xc0
TCCR1A	0x80	UCSR0B	0xc1
TCCR1B	0x81	UCSR0C	0xc2
TCCR1C	0x82	UBRR0L	0xc4
TCNT1L	0x84	UBRR0H	0xc5
TCNT1H	0x85	UDR0	0xc6

LDS

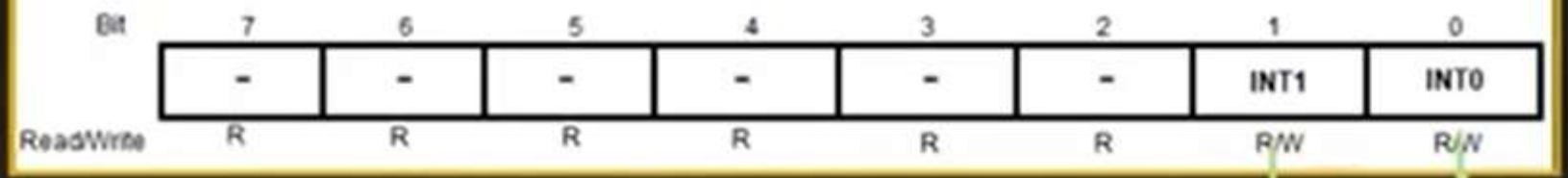
STS

EIMSK - External Interrupt Mask Register

Bit	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	INT1	INT0
Read/Write	R	R	R	R	R	R	R/W	R/W

Analisis bit a bit del registro sólo se tiene INT0 E INT1

EIMSK - External Interrupt Mask Register



1 = INT1 activado.

0 = INT1 desactivado.

1 = INT0 activado.

0 = INT0 desactivado.

EIMSK - External Interrupt Mask Register

Bit	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	INT1	INT0
Read/Write	R	R	R	R	R	R	R/W	R/W

0 0 0 0 0 0 1 1

0 3

0X03

EICRA – External Interrupt Control Register A

Bit	7	6	5	4	3	2	1	0
					ISC11	ISC10	ISC01	ISC00
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W

EICRA - External Interrupt Control Register A

Bit	7	6	5	4	3	2	1	0
	-	-	-	-	ISC11	ISC10	ISC01	ISC00
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W

La interrupción se ejecuta cuando hay un nivel bajo es decir cero

Table 12-2. Interrupt 0 Sense Control

ISC01	ISC00	Description
0	0	The low level of INT0 generates an interrupt request.
0	1	Any logical change on INT0 generates an interrupt request.
1	0	The falling edge of INT0 generates an interrupt request.
1	1	The rising edge of INT0 generates an interrupt request.

EICRA - External Interrupt Control Register A

Bit	7	6	5	4	3	2	1	0
	-	-	-	-	ISC11	ISC10	ISC01	ISC00
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W

Nivel lógico

Table 12-2. Interrupt 0 Sense Control

ISC01	ISC00	Description
0	0	The low level of INT0 generates an interrupt request.
0	1	Any logical change on INT0 generates an interrupt request.
1	0	The falling edge of INT0 generates an interrupt request.
1	1	The rising edge of INT0 generates an interrupt request.

EICRA - External Interrupt Control Register A

Bit	7	6	5	4	3	2	1	0
	-	-	-	-	ISC11	ISC10	ISC01	ISC00
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W

Table 12-2. Interrupt 0 Sense Control

ISC01	ISC00	Description
0	0	The low level of INT0 generates an interrupt request.
0	1	Any logical change on INT0 generates an interrupt request.
1	0	The falling edge of INT0 generates an interrupt request.
1	1	The rising edge of INT0 generates an interrupt request.

EICRA - External Interrupt Control Register A

Bit	7	6	5	4	3	2	1	0
	-	-	-	-	ISC11	ISC10	ISC01	ISC00
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W

Table 12-2. Interrupt 0 Sense Control

ISC01	ISC00	Description
0	0	The low level of INT0 generates an interrupt request.
0	1	Any logical change on INT0 generates an interrupt request.
1	0	The falling edge of INT0 generates an interrupt request.
1	1	The rising edge of INT0 generates an interrupt request.

EICRA - External Interrupt Control Register A

Bit	7	6	5	4	3	2	1	0
	-	-	-	-	ISC11	ISC10	ISC01	ISC00
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W

1 1

Table 12-1. Interrupt 1 Sense Control

ISC11	ISC10	Description
0	0	The low level of INT1 generates an interrupt request.
0	1	Any logical change on INT1 generates an interrupt request.
1	0	The falling edge of INT1 generates an interrupt request.
1	1	The rising edge of INT1 generates an interrupt request.

EICRA - External Interrupt Control Register A

Bit	7	6	5	4	3	2	1	0
	-	-	-	-	ISC11	ISC10	ISC01	ISC00
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W

0 0 0 0 1 1 1 1

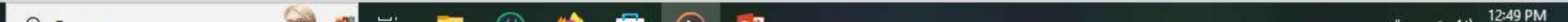
0 F

0X0F

EIFR - External Interrupt Flag Register

Bit	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	INTF1	INTF0
Read/Write	R	R	R	R	R	R	R/W	R/W

Banderas



EIFR - External Interrupt Flag Register

Bit	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	INTF1	INTF0
Read/Write	R	R	R	R	R	R	R/W	R/W

Se pone en 1 cuando hay una interrupción en INTF0

INTF0

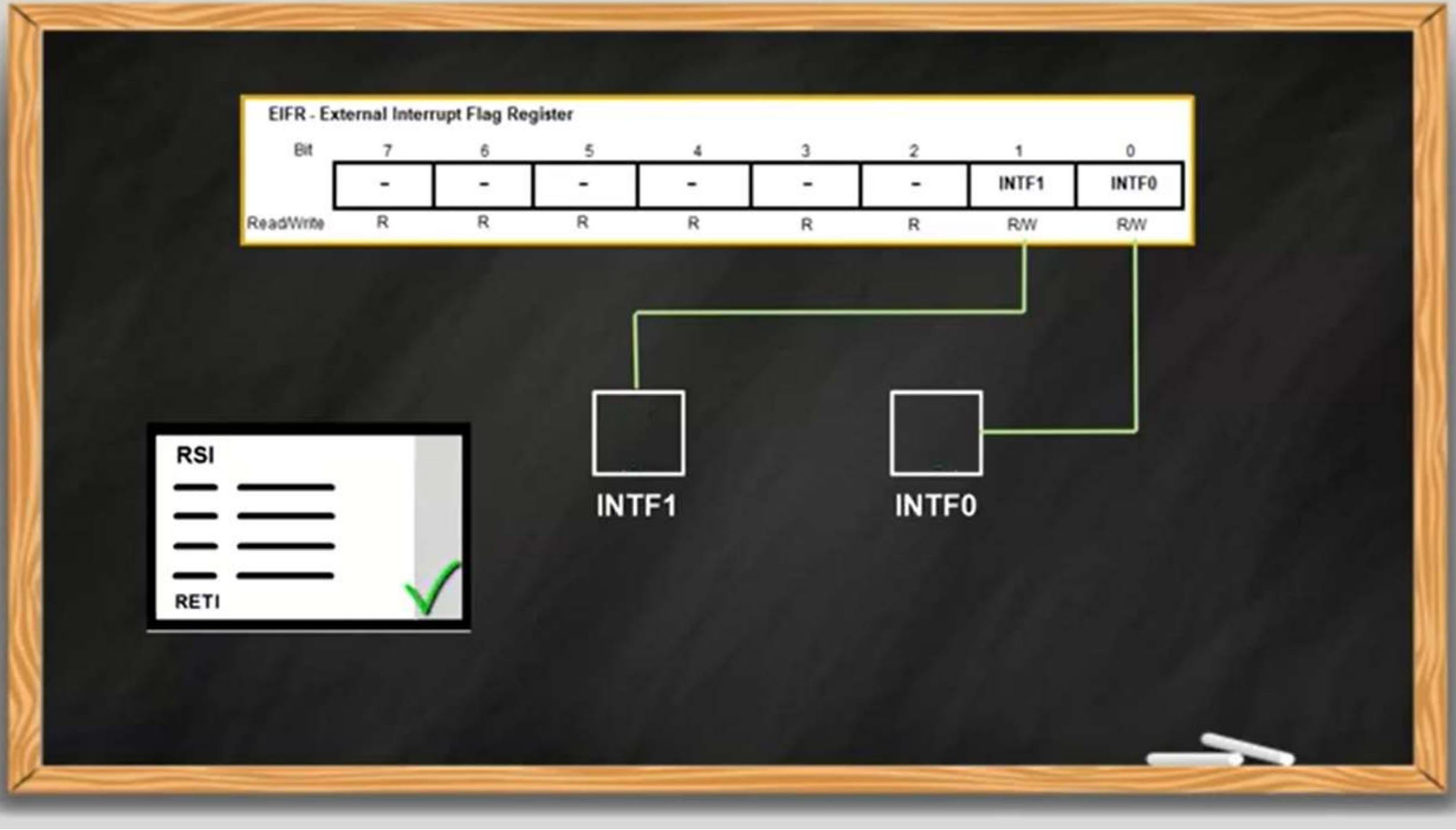
EIFR - External Interrupt Flag Register

Bit	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	INTF1	INTF0
ReadWrite	R	R	R	R	R	R	R/W	R/W

INTF1

INTF0

Se pone en 1 cuando hay una interrupción en INTF1


EIFR - External Interrupt Flag Register
Bit
7
6
5
4
3
2
1
0
-
-
-
-
-
-
INTF1
INTF0
ReadWrite
R
R
R
R
R
R
R/W
R/W
INTF1
INTF0
RSI
RETI

¡Muchas gracias!