Shylaja Ravikumar shylajaravikumar103@gmail.com
PWB Designer : +91 9663950202
LinkedIn: https://www.linkedin.com/in/shylaja-ravikumar

Objective:

Willing to work in a challenging environment where I can utilize my skills and abilities to achieve target set by management and for the enhancement of organization and my career.

Roles and Responsibilities:

- Responsible for complete CAD activities starting from design phase to board delivery.
- Worked on High-speed PCB designs.
- Primary responsibility shall be to lead the team to achieve its objectives and contributing to the business goals of the organization by establishing a high quality, low cost, reliable design environment and on time delivery.
- To implement the requirement of Design engineer into PCB layout.
- Worked on designs standards such as High-Speed Digital, Analog & Mixed signal Design and memory designs.
- Worked on Impedance Controlled Designs and critical constraint driven boards.
- Matched propagation delay / Relative propagation delay.
- Design technology of 4/4 up to 16 layers.
- Designed boards using Blind, buried, via in pad and HDI designs.
- Differential signal frequencies of 4 Gb/s on PCIE signals. Ethernet differential pairs of 100Mb/s.
- Addressing of DFX requirements.
- Taking care of board level Thermal Analysis.
- Knowledge and experience with PCB fabrication process, PCB assembly-Manual and Automated.
- Meets Signal Integrity / EMC requirements.
- Design verification with all design constraints\skills.
- Generating fabrication and assembly drawings.

Designing Tools:

- Cadence Software [Allegro v16X], Altium v14.
- Or CAD Schematic Capture v16X, Altium v14.
- Concept HDL schematic capture, PADS [Basic knowledge]

Skill Set:

Servers/Platforms	**:** Windows 7, XP.
CAD/EDA Packages	**:** Or CAD 16.x ver, Allegro 16.X. Altium v14.
High Level Languages	**:** C

Technologies:

- Ultra-Fine Line Standards (3 mil trace width, 3 mil clearance, with Blind and Buried via)
- Fine Line Standards (4 mil trace width, 4 mil clearances)
- Normal Standards (8 mil trace width, 8 mil clearance)
- High Reliability Standards (10 mil trace width, 10 mil clearance)

JOB DESCRIPTION:

- Involved in schematic capturing, Netlist and Bill of Material Generation.
- Involved in Library creation with IPC standards.
- Board outlines creation as per inputs (DXF files) and importing Net list.
- Mechanicals and Major component placement as per mechanical requirements.
- Involved in stack-up creation.
- Involved in constraint setups like spacing, width, length.
- Worked with Blind, Buried and Back-drill Via Technology.
- Critical signal, differential pair routing and length matching.
- Power plane splitting.
- Design Error checking and clean up.
- Artwork setup and Gerber generation.
- Packaging for Fabrication Release

WORK EXPERIENCE

Sienna Ecad Bangalore, India Jan 2011 – Jan 2015

Position: PCB Designer

Projects Undertaken in Allegro:

- **Project Name** : WSM

  ROLE : Layout Design engineer.

  TOOL : Allegro 16.5

  RESPONSIBILITIES: Footprint creation, Placement, constraint setup, routing, DRC cleanup, Gerber generation.

  DESCRIPTION: The board size is 282x320mm, with a layer count of 16 including 6 signal 8 planes (5 Ground & 3 Power). The board contains 0.8 and 1mm pitches BGA's, Critical interfaces like DDR3, and flash interface and SGMII signals.

- **Project Name** : CBM

  ROLE : Layout Design engineer.

  TOOL : Allegro 16.5

  RESPONSIBILITIES: Placement, constraint setup, routing, length matching DRC cleanup, Gerber generation.

  DESCRIPTION: The board size is 282x320mm, with a layer count of 16 including 6 signal 8 planes (5 Ground & 3 Power). The board contains 0.8 and 1mm pitch BGA's, Critical interfaces like DDR3 SO-DIMM, USB, SGMII and RGMII signal. Blind and buried vias were used for data and address signals.

- **Project Name** **:** VLF Card

  ROLE : Layout Design engineer.

  TOOL : Allegro 16.3

  RESPONSIBILITIES: Placement, constraint setup, routing, length matching DRC cleanup, Gerber generation.

  DESCRIPTION: VLF CARD was designed for communication using MPC (1023 pins DDR2 (BGA 84 pins, 10 No's), Ethernet (364pins, BGA), PCIE (PCIE_EDGE_X4-64, PCIE_EDGE_X8-98), and other interfaces. The major signals involved are 64-bit DDR data signal and 16-bit address signals (two modules of DDR each with 5 DDR), 148 Differential signals (PCIE, DDRCLK, CLK). Placement and length matching was challenging due to space constraints. Even the fanout length was fixed and they were length matched. All the differential signals were length matched with 2.5 mils. Followed High-speed signal routing guidelines, PCI express routing guidelines. The layout was designed using a board size of 233.35mm X 160mm" with 1.6 mm as board thickness. No of components involved are 2200 with 7500 connections, 16 BGA's were used and had controlled impedance signals with 50 ohms for single ended and 100 for differential signal.

- **Project Name**: VSCC CARD.

  ROLE : Layout Design engineer.

  TOOL : Allegro 16.5

  RESPONSIBILITIES: Placement, constraint setup, routing, length matching DRC cleanup, Gerber generation.

  DESCRIPTION : It includes MPC (272 pins, BGA), DDR (84 pins, BGA), Ethernet chip, DAC, PCI, Flash (64 pins, BGA) and Cross point Switch.
  The Placement and routing to Cross point switch was very critical and challenging. Provided 3W spacing and shielding between each RGB signal. The layout was designed using a board size of 233.35mm X 160mm" with 2.1mm as board thickness. No of the components involved are 3000 with 8000 connections.

- **Project Name**: Tactical

  ROLE : Layout Design engineer.

  TOOL : Allegro 16.5

  RESPONSIBILITIES: Placement, constraint setup, routing, length matching DRC cleanup, Gerber generation.

  DESCRIPTION : It Includes IMX6 Processor (624 pin BGA),4DDR3(96 pin BGA),EMMC(Embedded Multi Media Card,169 pin BGA),CPLD,USB Hub, Edge finger, Ethernet and HDMI.The routing of DDR and high speed interface was challenging. . The

layout was designed using a board size of 70mm X 70mm" with 1.6mm as board thickness. No of the components involved are 3000 with 8000 connections.

Academic Qualifications:

- **B.E in Instrumentation and Electronics**
  GSSSIETW, Mysore. VTU
  2006-2010

- **ME in Microelectronics**
  BITS PILANI DUBAI, DUBAI
  2021-2023

Personal Details:

Date of Birth **:** 19th September 1988

Languages Known **:** Kannada, English, Hindi and Tamil

Nationality **:** Indian

Passport no : M7938543

DECLARATION:

I hereby declare that all the details provided above are true to the best of my knowledge. I bear the responsibility for the above-mentioned details.

Place: (Shylaja Ravikumar)