M M SRAVANI ($\overline{Ph.D}$)

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OBJECTIVE

RTL/Physical Design Engineer with close to total of 5 years of Experience, aspiring for challenging career in research as well as product development where I can learn future technologies to enhance my skills to grow up and contribute to the success of the Organization.

Professional Experience

- 5+ Research experience in VLSI designs along with Physical implementation to fabricate an IC Chip

Professional Summary

- Experience in **Netlist 2 RTL** level design implementation.
- Experience in **RTL 2 GDS** Block-Level Physical Design Implementation.
- Strong Experience in **Floorplan, Placement, CTS, Timing Optimization and Routing**.
- Experience in Signoff **Static Timing Analysis.**
- Experience in Timing Closure & ECO Implementation
- Experience in **Verilog/VHDL scripting language**
- Experience in Synthesis/STA
- Knowledge on Physical Verification checks like **DRC, LVS, ERC & ANT**
- Good understanding of UPF & Low Power Implementation
- Trained in **VLSI Mentors** training institute for **Physical design knowledge**
- Knowledge on technology nodes: **180nm,90nm,65nm,28nm, 7nm**
- Published **research papers** in **IEEE transaction of VLSI** & **Biomedical circuits and systems**

TOOLS SKILL -SET

RTL Design	Xilinx ISE/ Vivado, HLS, Model sim, Design complier
FPGA Boards	Virtex, SoC Boards, Spartan
Physical Design	ICC2, Innovus
Timing Analysis	PrimeTime
RC Extraction	Star-RC, Quantus/QRC
Physical Verification	Calibre
Scripting Languages	Verilog/ VHDL , C, Basics of TCL
Operating Systems	Linux, Windows

Educational Qualification

- **Ph.D in VLSI from** VIT university **(2017-2023): Defense is on April 2023**
- **Master of Technology in VLSI DESIGN from** JNTU University (2013 – 2015): ***82%***

- **Bachelor of Technology in Electrical & Electronics Engineering** from JNTU university (2008 - 2012) :***81%***
- **Higher Secondary School** Sri Chaitanya college, Tirupati (2006-2008) : ***94.3%***
- **High School** Teja E/M School, Sullurupeta (2006) : ***88%***

Project Details

Research Project 1 : Design and Implementation of efficiency-enhanced SHA-3 architecture for multi-modal biometrics
Tools Used : Xilinx Ise, Vivado, VIO IP core
Boards : Zed board, virtex 7
Language : Verilog
Challenges : Synchronization with the clock and maximize the frequency in permutation block
Blocks : Synchronized padder block, compact-dynamic round constant (RC) generator.
Publication : IEEE transaction on VLSI

Project Description : Synchronized padder block and a compact-dynamic round constant (RC) generator to achieve highly efficient Keccak architecture are proposed. The proposed design yields high security with an option of 1024 bits as capacity "*c*," while limiting the round count to less than 12 for the base design. Fusion schemes are adapted as a cost-effective approach in the base design to explore and arrive at the best efficient architecture for biometric access control application. The hybrid architecture designed as a pipeline structure with 2 stages eliminated the need for on-chip digital signal processor (DSP) and block random access memory (BRAM) slices. Though fusion schemes might lead to the increase in area, the minimized structural RC design coupled with a low-cost architecture, ensures to achieve moderately low area. This proposed SHA-3 architecture has been implemented in Xilinx ISE &Vivado. Successfully implementation & tested on hardware Zedboard and V7 board.

Research Project 2 : Securing e- Health Record with BIO-HASH key using HMRF key generator
Tools Used : Xilinx Vivado
Boards : Zedboard, virtex 7,
Language : Verilog
Challenges : To synchronous the SHA-3, Random Generation, Fusion blocks
Blocks : Pseudo Cascaded SHA-3, Random compression Logic, Priority compression Logic Fusion using MUX logic along with gates
Publication : IEEE transaction of Biomedical circuits and Systems

Project Description : A novel contribution is proposed by integrating the biometrics data with cryptographic hash for enhancing the security & privacy of access & record of the health care data. Further, a novel hashed minutiae random fusion (HMRF) generator is proposed in this paper for generating the Bio-Hash key which is fed for a crypto AES algorithm for encryption & decryption of patient(citizen) health record. This HMRF includes a minutiae extraction, SHA-3 hashing, bio-skimmer, and fusion process. The morphological biometric fingerprint has been chosen to extract the minutiae a convert it into Hexa value and then given to pseudo cascade SHA-3 architecture. The subsequent bio-skimmer is used to skim the biometric hashed value through 512 to 128 bits with the help of proposed RCL and PCL logic circuit. Then, Fusion modes area help to get fusion the MP and P bio-skim value to generate a Bio-Hash key. Implementation of this HMRF logic on V7 FPGA device achieved 4171 slices which is lowered as 11% compared to reported designs. Further, proposed a design of Write/View/Read only mode to access/ stored the patient health record after medical examination by the medical partitioner (MP). The performance evaluation these modes on V7 with standard 100Mhz clock and achieved as 8.2/8.3/8.0 ns respectively.

Research Project 3 : ASIC implementation of Proposed 14 different designs of SHA-3 to analysis the real power, timing achievable of the block upto 500MHz
Tools Used : Cadence genus / innvous
Technology : TSMC 65nm
Description : The objective is PnR implementation of the architecture from Netlist to GDS. This architecture is critical in congestion. Closing the block at all the Netlist drops was challenging. Done Floor planning, Placement, CTS and Routing and fixed DRC's
Implementation : PnR implementation from Netlist to GDSII
Challenges : Criticality in the blocks is congestion and timing issues. Challenges faced is, it took much iteration to achieve the best floorplan having good timing results and less congestion. Resolved the congestion issue by applying the PD techniques like cell padding and density screens.

Industry project:

Name **: VLSI Mentors Training Institute, Bangalore**
Duration **: 8 months (2022-May to 2023 Feb)**
Position **: Physical Design Trainee**
Tools : ICC2, Prime time, Star-RC
Block Name : ECC_TOP_WRAP
Technology : TSMC 28HPC
Metal Layer Stack : 10+1
Max Clock Freq : 455MHz
Instance Count : 50K
Macro Count : 40
Gate count : 200K

Challenges Handled/learned:

1. Heavy Congestion in the block due to more logic interaction, used bound to guide placement.
2. Multiple floorplan experiments to find the best macro placement
3. Block was having congestion issues due to more complex cells.
4. Tried multiple experiments to accommodate the given area.
5. Created multiple path group& applied weightage.
6. Timing Critical, created multiple path groups & applied more weight
7. Report multiple violated paths using report commands
8. Generated Timing ECO's using PT -DMSA & what if analysis
9. PT -DMSA used unwanted cells in the ECO, applied don't_use
10. Fixed DRC's Manually in the route congested area.

Academic Project

- **M Tech Project :** Design of Compact Implementation Of SHA-3(512) On FPGA
- **BTech Project :** FPGA implementation of SHA-224 Algorithm oriented Digital signature
- **Mini Project :** Asynchronous FIFO with Asynchronous pointers.
- **Other projects :** Di-Automatic Switch, Traffic Clearness for VIP's vehicles Using DTMF.

ACHIEVEMENTS

- Best presenter award in international conference at Malaysia (virtual mode) at 2021.
- Second prize winner of the paper presentation in internal paper presentation during B.Tech
- JNTU university Rank holder in B.Tech.

- Class topper in 10^{th} and 12^{th}
- Has become the class representative during schoolings and in college

Personal Details

- **Name** : Sravani MM
- **Father's Name** : Babu MM
- **Husband Name** : N Bharani kumar
- **Children** : N Hetvik
- **Date of Birth** : 11-08-1991
- **Nationality** : Indian - Hindu
- **Languages known** : Telugu, English, Tamil % Hindi
- **Permanent Address** : Door No :2-114, Nethaji Road Sathyavedu-517588, Chittoor(Dist)

Refernces Details

S.NO	NAME	DESIGNATION	COMPANY /COLLEGE	PHONE
1	Dr. S Ananiah Durai	Associate professor (My supervisor)	VIT- Chennai	9962084407
2	Kumar	VLSI Trainer	VLSI Mentors Training, Bangalore	8310858699
3	Mr. Vijender	Program engineer	Corel technology Bangalore	7259781786

Declarations Details

I hereby declare that the above written Particulars are true and correct to the best of my knowledge and belief.

Place: CHENNAI Signature