Shwetha.M
Mail ID: shwetha.m1691@gmail.com
Phone no: 7892619101 / 9481015738

Work Experience

UST Global Malaysia (Remotely Support)
Associate III - Semiconductor Product Validation, July 2021 till date
Client – Intel Malaysia, July 2021 till date

Faststream Technologies
Analog design Engineer, April 2019 to October 2019.

Gateway2 Silicon Technology
Analog layout engineer, April 2018 to April 2019.

Softcons Innovations India Pvt Ltd
Software developer, March 2017 to April 2018.

Job Responsibility

- Performed Reliability verification (RV) checks such as Interconnect self-heat, static and dynamic IR drop analysis and electro-migration,local thermal heat ,sfactor violations for signal and power nets, post thermal analysis results for average,peak,RMS current for signal nets.
- Report on blocks with IR Drop analysis to be deratable or non deratable
- Block power assignment for filler blocks are decisions based on power usage by neighboring blocks.
- Debugging errors caused after job submission using Redhawk platform.
- Responsible for verifying individual blocks, partitions, or intellectual property as well as verification at the full chip level.
- Reviewing on errors/warnings of Tier 1,2 and 3 resulted while RV run flush completion
- Filed HSD with DA team for errors/warnings waivable or not.
- Release the functional blocks, subsystem, Full chip after RV and DA confirmation on error/warnings using TCL scripts given by Intel DA team.
- Experience in all analog layout concepts matching, shielding, signal flow,floor planning.
- Hands on Experience in fixing Latch-up, Antenna, DRC, and LVS.
- Have worked on Deep N-well cmos process.
- To work with circuit design of inverters, Band gap reference block withlead engineer.
- Research on migration of design from higher node to lower node usingAnalog rail tool. Research on development of IP blocks for Yarra sound system using Zynq -7000 FPGA.
- Experience in UNIX based working platform and capable user Tools Command Language scripting style (TCL)

Technical Skills

- Experience in debugging dropnets, shorts,IR drop analysis,hotnets,sfactor,EM Checks etc using **ANSYS Redhawk tool.**
- **Synopsys C-Compiler, Synopsys IC-Validator, Cadence Virtuoso,eFabless, Analog Rails**: Analog layout, analog circuit designs.

Projects

#Falcon Messa 6 (MS 0.8) 10nm

Role: Testcase on the ASIC RV Spark Flow for job submission tool from ANSYS for the blocks with input output interfaces. Performed Intel RV Sign off conditions. Setting up RV corners,ploc file creation,reviews on log files, error/warnings,report with DA team

#Falcon Park 8 (MS 0.8,1.0) 10nm

Role: Involved in the activities related to RV flow runs and job submission in Intel recommended tool from ANSYS and provide feedback to the Design automation team and successfully completed the RV runs with a fully functional RV flow flush for main functional blocks, sub systems which are functionally input output interfaces, filler blocks. Setting up RV corners,ploc file creation,reviews on log files, error/warnings,report with DA team,Release steps followed for releasing blocks

#Sundance Messa (MS 0.5,0.8) 10nm

Role: RV job submission and debugging on errors using Redhawk, update collaterals required for DEF, SPEF,LEF files. Performed documentation after the signoff of the project.

#Digital Standard Cell Library

Role: Arriving standard cell height and designing of standard cells like INV, NAND, AND, OR and NOR.

#Low dropout Regulator (LDO)

Role

- Designed sub blocks like error amplifier, Bandgap reference and feedback resistor blocks
- Complete floor planning of Blocks, routing and communicating with teamfor top module design.
- Meeting the layout constraints like matching, shielding, Electro Migration and IR drop with physical verification (DRC&LVS).
- Layout / Design Tools: Synopsys C-Compiler
  Synopsys IC-Validator: Design rule check, Layout versus schematic

#Operational Amplifier

Role

- Design of op-amp and layout verification
- Matching techniques to implement differential input pair and current mirrors. Take care of EM and IR drop for high current carrying devices.
- Involved in placement, Matching of MOS devices, routing by taking care of Electro migration, coupling and Layout Verification.
- Layout / Design Tools: Synopsys C-Compiler
  Synopsys IC-Validator: Design rule check, Layout versus schematic

#Current Mirror

Role:

- Designed Current mirror design and verification.
- Involved in placement, Matching of MOS devices, routing by taking care of Electro migration, coupling and Layout Verification.
- Layout / Design Tools: Synopsys C-Compiler
  Synopsys IC-Validator: Design rule check, Layout versus schematic

	Software Developer **#Suiteup:** Office suite web application in which one can manage IT firm. **#Mighty Ads:** Newspaper advertisement web application **Role:** Coding and testing for complete flow of User and Admin side in PHP**.**Design, maintain and deliver applications in C#.
Education	**PhD:** Low Power VLSI Design from Sathyabama institute of science and technology. (Part time –Currently). **M.tech:** VLSI Design and Embedded systems from Srinivas Institute of technology. **B.E:** Electronics and Communication Engineering from KVG Collage of Engineering and Technology.
Publications	• Design and analysis of batteryless cardiac pacemaker through combining thermoelectric generators along with dc-dc converter **Wiley Publications with Impact Factor 2:86** and indexed **in web of science and scopus.** • Design,Simulation and Analysis of a Replacement-free implanted thermoelectric based Pacemaker **Taylor and Francis Publications** with **Impact Factor 3.166** and indexed in **web of science and scopus.** • Paper entitled "**DC-DC Buck Boost converter for Renewable and Bio Medical Applications for Real time IOT**" in Scopus Indexed Journal IJRTE. • Paper entitled "**Self-powered Implantable Device Using Thermo Electric Generator with DC-DC Converter for Elimination of Bradycardia**" in SpringerLecture Notes on Data Engineering and Communications, Vol. 63, Chapter 13. • Paper entitled "**Implementation of I2C/UART master bus controller**" in IJRIT