PALLAVI KAR

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In quest of a challenging position in the organization that offers me generous opportunities to explore & outshine in the field of VLSI Industry as DESIGN or VERIFICATION ENGINEER while accomplishing personal, professional and organizational goals

CAREER SUMMARY

- ≈ Solutions focused, proactive and industrious **Electronics & Communciation Engineering Professional** with **5 months** of experience with excellent academic credentials
- ≈ Good experience in Project Management activities including project scoping, estimation, planning, scheduling, resource administration and quality management
- ≈ Significant knowledge in understanding the process, operation sequences, process parameters required to achieve quality characteristics
- Recognized as a hands-on, proactive professional who can rapidly identify problems, formulate tactical plans, initiate change and implement effective programs in challenging and diverse environments
- ≈ Adroit at learning new concepts quickly, working well under pressure and communicating ideas clearly and effectively
- ≈ Dedicated and highly ambitious to achieve personal goals as well as the organizational goals
- ≈ Superb communication skills with good teamwork spirit and multitasking ability

CORE STRENGTHS

- ≈ Digital Electronics
- ≈ System Verilog
- ≈ UVM, Linux
- ≈ Static Timing Analysis
- RTL Coding using Synthesizable constructs for Verilog
- ≈ FSM based design Simulation & Synthesis
- ≈ Code Coverage, Functional Coverage
- ≈ CMOS Fundamentals

- ≈ Assertion Based Verification using System Verilog Assertion
- ≈ Good team player
- ≈ Analytical & Troubleshooting Ability
- ≈ Positive Attitude
- ≈ Hardworking and quick learner
- ≈ Quick Adaptability
- ≈ Sincerity and Self-Confidence
- ≈ Commitment towards work

TECHNICAL FORTE

- VLSI Skills: HDL: Verilog, HVL: System Verilog, TB Methodology: UVM, Protocols: AXI, AHB, UART, I2C, SPI, EDA Tool: Questasim & Xilinx ISE, Xilinx Vivado, Domain: ASIC/FPGA front- end Design and Verification
- ≈ **Design Skills:** Digital Electronics, Static Timing Analysis, Verilog Programming, Advance Verilog Code Coverage, System Verilog HVL, UVM Methodology
- ≈ Programming Languages: C, C++, Java
 ≈ Operating Systems: LINUX, Windows
 ≈ Scripting Languages: Pearl Scripting

CERTIFICATIONS & TRAININGS

- pprox Advanced VLSI Design and Verifiction course from Maven Silicon in 2023
- ≈ Workshop from TechExploration on ArduinoIDE
- \approx Workshop from Hex n Bit on IoT

ACADEMIA

- ≈ B.Tech. (Electronics and Communication Engineering) from University Institute of Technology, The Burdwan University in 2022 with 78.6%
- ≈ Diploma in Electronics and Telecommunication Engineering from Dr. B.C. Roy Polytechnic, WBSCTE in 2019 with 83.3%
- ≈ **12**th from Bidhan Chandra Institution for Girl's, West Bengal in 2016 with 61%
- ≈ 10th from M.A.M.C Township Modern High School (W.B.S.E), Durgapur, West Bengal in 2014 with 65.8%

PROFESSIONAL EXPERIENCE

ERICSSON INDIA GLOBAL SERVICE, Noida, Sector-62 Domain Support Specialist

(Jul'22 - Nov'22)

Key Deliverables:

- ≈ Responsible for troubleshooting of CS Core RAN network part only
- ≈ Verified 2G, 3G, 4G technology
- ≈ Worked for the Client Virgin Media O2 UK Limited and Client Orange Cameroun South Africa
- pprox Responsible for monitoring the 2G/3G/4G Technology , BSC , RNC and some special sites

Key Highlights:

≈ Received Star Performer of the Month Award (one time achievement)

ACADEMIC PROJECTS

Project#1: ROUTER 1X3
HDL: Verilog

EDA Tools: Questasim and ISE

Description: RTL design and Verification, the router accepts data packets on a single 8-bit port and routes them to

one of the three output channels channel 0, channel 1 and channel 2.

Project#2: WEATHER PREDICTION FOR ECONOMIC GROWTH IN INDIA

Tools: Origin Pro

Data: Meteorological Survey of India

Description: Completed last year project in Weather prediction with the help of data process. The main aim of this

project is to show how much rainfall increases due to climate change all over the country India. Collected all India rainfall and temperature data of past 20 years from Meteorological dept. Every year crops damaged due to excess rainfall, especially Paddy Wheat and Maize is affected and it impacts on Economy of India. If we predict the rainfall then it will save large amount of crops and it

will help to decrease the price.

PERSONAL DATA

Date of Birth: 15th May, 1998

Languages Known: English, Bengali & Hindi Location Preference: Delhi NCR / Bengaluru