A.NIKHILA

Department of Electronic and Communication Engineering, VLSI.
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CAREER OBJECTIVE:

To work with an organization which provides me an opportunity to grow and use my potential and skills to fulfill the organizational goals by acquired knowledge.

ACADEMIC QUALIFICATION:

Course	Institution	Board/ University	Year of Completion	Percentage
M. Tech (VLSI)	Sree Vidyanikethan Engineering College,Tirupathi	Autonomous	2020	83%
B. Tech (ECE)	Sri Padmavati Mahila Visvavidyalayam, Tirupathi	SPMVV	2018	69%
Higher Secondary	NRI Academy, Tirupati	Intermediate	2014	83%
Secondary School	Gautam Talent School, Tirupati	State Board	2012	90%

SKILL SET

- EDA Tools : Mentor graphics, Xilinx ISE, Digital schematic, Microwind tool, PSPICE and basics of HSPICE .
- Hardware Description Languages : VHDL, Verilog.
- Mathematical Tool : MATLAB.
- FPGA : Spartan-3E

STRENGTHS:

- Positive attitude.
- Rapid at learning things.
- Ability to cope up with different situations.

AREA'S OF INTEREST:

- VLSI design

EXTRA-CURRICULAR ACTIVITIES:

- Member of "Indian science congress association".
- Assistant class representative.
- Coordinator in college fest.
- Seminar on "FOOT STEP POWER GENRATION" in college technical fest 2k18 .

WORKSHOP: "ANDROID CONTROL ROBOTICS" : In this robot communicates via Bluetooth. While pressing each button on the application, corresponding commands are sent via Bluetooth to the robot. The commands that are sent are in the form of ASCII. The Arduino checks the command received and controls the servo motors depending on the command received to cause it to move.

PROJECT 1: "FOOT STEP POWER GENRATION" : This project is used to generate voltage using footstep force. This system works as a medium to generate power using force. When force is applied on piezoelectric sensor, then the force is converted into electrical energy. Here we are using AT89S52 to display the amount of battery get charged.

PROJECT 2: "SCALABLE STRUCTURES OF MICROPROGRAMMED DIGITAL FILTER USING CSLA AND WALLACE TREE MULTIPLIER" : All conventional full adders are recouped with XOR based full adder to deduce circuit complexity. A microprogrammed FIR filter is implemented with XOR based full adders, area-efficient CSLA with all redundant logic operations are obliterated which are present in conventional CSLA i.e, the carry select (CS) operation is line up before the calculation of final-sum. and Wallace tree multiplier. A 4-tap FIR filter with parallel and serial architectures are designed to demonstrate the proposed system. The designs are coded in Verilog language and perceived using Xilinx ISE 14.5 technology.

PERSONAL DETAILS:

- Father's Name : A. Elia
- Date of Birth : 09-05-1997
- Languages Known : English and Telugu
- Hobbies : Net surfing

DECLARATION:

I, A.NIKHILA do hereby confirm that the information given above is true to the best of my knowledge.

Place : Tirupati **(A.NIKHILA)**