SARANYA P M

DFT Engineer

CONTACT

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PROFESSIONAL SKILLS

- Self-confidence and interactive person with positive attitude
- Time management skills.
- Good leadership skills.
- Good communication and presentation skills.
- Teamwork.
- Quickly adaptable to any new situation and environment.

A highly motivated and hardworking individual with extensive knowledge of the DFT concepts. A quick learner and team player committed to staying current with emerging trends and Technologies in VLSI design. Detail oriented with strong organizational, problem-solving, and communication skills, and a willingness to take on new responsibilities to contribute to the success of the company. Charismatic and dependable Assistant Professor with 3.6 years' experience in electronics and communication engineering.

PROFESSIONAL TRAINING

ADVANCED VLSI DESIGN AND DFT

Maven Silicon VLSI Design and Training Center, Bangalore

March 2023- Till date

VLSI DOMAIN SKILLS

- HDL: Verilog.
- EDA Tool: Mentor Graphics-ModelSim, Synopsys-DC Compiler.
- Domain: ASIC/FPGA front-end Design and DFT.
- Operating System: Windows and Linux.
- Core Skills: RTL Coding using Synthesizable constructs of Verilog, FSM based design, Simulation, CMOS Fundamentals, Code Coverage, Synthesis, Static Timing Analysis.

ACADEMIC PROJECTS

- M.E PROJECT:
  Construction of Compact High -Throughput S-Boxes and Modified Mixcolumn Implementation for AES.
- B.E PROJECT:
  GSM Based Voting Machine.

CERTIFICATES

- Presented paper on Construction Of Compact High-Throughput S-Boxes And Modified Mixcolumn Implementation For AES in SNS College Of Engineering, Coimbatore (National Conference)
- Participation in Faculty Development Program on Teaching Excellence and Methodology (MEA Engg College)

DFT SKILLS

Experience with multiple aspects of the following

- ATPG, Test Coverage
- JTAG, BSDL, IJTAG
- Memory and Logic BIST
- Synthesis scan stitching
- Memory BIST implementation
- Scan/Jtag/boundary-scan insertion and ATPG pattern generation
- Test coverage and fault coverage analysis
- Knowledge/experience with ATPG / DFT tools: Tessent, System Verilog, RTL

PROJECT UNDERTAKEN

Router 1x3 – RTL design and Verification

- HDL: Verilog.
- EDA Tools: Mentor Graphics - ModelSim, Synopsys-DC Compiler.
- Description: The router accepts data packets on a single 8-bit port and routes them to oneof the three output channels, channel0, channel1 and channel2.

Responsibilities

- Architected the block level structure for the design.
- Implemented RTL using Verilog HDL.

DFT Insertion on RISC-V Core

- EDA Tools: Mentor Graphics -Tessent.
- Description: Insertion of Boundary scan, Scanchain, EDT IP core on this 32bit processor design and implement the ATPG pattern generation using stuck-at-fault model, and the fault coverage is obtained and improved.

LANGUAGE

- English
- Malayalam
- Hindi

INTEREST

- Singing and dancing
- Cooking
- Creative Designing
- Gardening
- Travelling

EXPERIENCE

2013 APRIL - 2016 DEC **ASSISTANT PROFESSOR**
MEA Engineering College Perinthalmanna

- Handled Electronics and Communication Subjects.
- Supports students in creating and presenting Projects & Seminars.

2013 MARCH - 2013 APRIL **LECTURER**
IHRD Perinthalmanna

- Handled Electronics related Subjects.

EDUCATION

ME - ANNA UNIVERSITY OF TECHNOLOGY
2011 – 2013 VLSI Design
CGPA–8.09

BE - ANNA UNIVERSITY OF TECHNOLOGY
2007–2011 Electronics and Communication
CGPA–8.45

HSE - KERALA STATE BOARD
2005–2007 Higher secondary
Percentage–72 %

SSLC - KERALA STATE BOARD
2005–2007 High school
Percentage – 84 %

DECLARATION

I hereby declare that the information given above is true to the best of my knowledge and belief & ready to bear any challenge.

Date:
Place:

Saranya P M