V. Monisha
Current Location - Chennai
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Objectives:

To work in an organization where I can show my talent and enhance my working capacities and professional skills, which would grow and fulfill organizational goals.

Work Experience:

1. FPGA Engineer (17th June 2019 – 31th October 2020(1 year 4 month))
   Axlware Technologies Pvt. Ltd.
   - *Fintech - Ultra Low latency FPGA based High Frequency Trading(HFT) Platform*
     Low latency software based HFT Platform
     - TCP/UDP offload engines
     - Handling market data, order interface, order management & risk controls – at FPGA network card level(Accelerator card). FPGA family worked - Altera Stratix 5, Intel ArriaX, Xilinx Alveo U250.
     - Support for multiple trading applications using a single interface to the exchange, yet providing an individual view of the order books for each application.
     - Created storage of object frames based on the event details using VHDL.
     - Created Platform design by integrating the FPGA components in system level.
     - Test benches in Verilog/SystemVerilog to simulate the design and verify the functionality using modelsim to debug the RTL issues and to check the timing violation which causes data corruption.
     - Created documentation for the modules present in the FPGA design.
     - Worked on Vitis IDE and Vivado HLx Design Suite development platform(RTL kernel and Block design method) with customized IP's .
     - Experienced with Software Altera and Xilinx.

2. Application Engineer (Intern) at "**Mirabilis Design Incorporation**" (Computer Architect & Soc Modeling internship) from 1st October 2019 to 31th March 2019(6 month).

   Projects done by using VisualSim Architect Tool:

   - Micron chip on DDR3
   - HMC Model (Hybrid Memory Cube)
   - Microsemi Smart fusion Soc FPGA
   - ADAS Behavior model

Skills:

- Knowledge in FPGA, RTL, languages such as Verilog, System Verilog, VHDL and C. Interface's worked on Avalon, AXI.
- Knowledge in digital electronics, CMOS circuits and EDA Tools - Altera Quartus II , Xilinx ISE, Xilinx -Vitis IDE & Vivado.
- Well versed in using lab equipment.
- Knowledge in Linux platform.
- Self-motivated, with the ability to work independently as well as in a team.
- Excellent Problem solving skills, with the ability to listen, understand the requirements.

Online Course:

- "VSD Physical Design Flow" and "TCL Programming" online course held by Kunal Gosh (Full time access on Udemy) Started from September 2020 - present.
- "VLSI Design Methodologies" online course held by Maven Silicon (Duration-7 weeks) from 1st October to 25th November 2018.

UG Internship:

- "RASPBERRY PI USING IOT" at Vi Microsystems Pvt. Ltd., Chennai from 25th-30th(5 days) May,2018.

UG Project:

- "Design and analysis of 4:2 compressor in Vedic multiplier using microwind2".

Workshop:

- "Vision controlled robotics" at Tarangg'16 by NIT Puducherry on 5th March, 2016.
- Two days workshop on "Analog and Digital system design using Cadence tool" by Department of ECE, Madurai -Thiagarajar College of Engineering from 18th-19th August, 2017.

Education Qualifications:

Stream	Name of the Institution	University/ Board	Month & Year of Passing	CGPA*/ Percentage
B.Tech (ECE)	Perunthalaivar Kamarajar Institute of Engineering and Technology, Karaikal.	Pondicherry university	May 2018	8.16
HSC	ATGGHSS, Karaikal	State Board	March 2014	86%
SSLC	NRGHSS, Karaikal	State Board	March 2012	85%

PERSONAL DETAILS

Date of Birth	:	09/07/1997
Gender	:	Female
Nationality	:	Indian
Marital Status	:	Single
Residential Address	:	5, Ramaiya Nagar , karaikal-609602
Language Proficiency	:	English, Tamil (First language), French (Beginner)

Place: Karaikal
Date : **V.MONISHA**