**G.BHAGYALAXMI**

**Email:** bhagyalaxmigunjugoori@gmail.com

**Mob:** +91-7997261943

*Analog Layout Design Engineer with 5+ years of experience in Custom*

*Standard cell design, Analog and Mixed Signal Layout Design Engineer.*

**Core Competencies:**

* Worked on various process nodes Technologies namely **3nm, 4nm, 5nm, 7nm, 8nm, 10nm, 14nm, 45nmand 130nm.**
* Efficient in dealing with all verification flow issues DRC, LVS and all parasitic extractions to achieve high quality layout deliveries.
* Good understanding of chip failure mechanisms like Antenna, Latch up, EM.
* Worked at multiple levels of Hierarchy and solved robust checks.
* Proper knowledge in floor planning based on signal flow, distribution of power and ground structures.
* Knowledge in DEF & LEF generation.

**Work Expertise:**

* Worked with Mirafra Technologies, Bangalore from June 2018 to December 2018.
* Currently working with LeadSoc Technologies (Client Samsung R&D) Bangalore from Jan 2020 till date.
* Good knowledge in IC Mask layout flow for Custom Analog, IO & Digital Blocks and custom cells.
* Good understanding of device physics & IC fabrication process.
* Good hands on experience on Layout blocks namely PLL, LDO, OP-Amps, AFC and PWM and digital blocks.

**Projects Undertaken:**

* **Project 1 : LN04LPP(DQ,DQS)**
  + **Technology :** 4nm
  + **Duration :** 6 months
  + **Tool :** Virtuoso.
  + **Roles & Responsibilities:** Floor planning, Routing and Verification.
  + **Challenges:**
    - Floor planning by using LEF.
    - Taken care of the LATCHUP. Need to check density.
    - Need to check robust DFM and GDS checks.
    - Power mesh for the blocks.
* **Project 2 :LN03LPE(PLL)**
  + **Technology :** 3nm
  + **Duration :** 3months
  + **Tool :** Synopsys.
  + **Roles & Responsibilities:** Floor planning, Routing and Verification.
  + **Challenges:**
    - Floor planning, taken care of the LATCHUP. Need to check density.
    - Very difficult to maintain Standard cell height i.e.1.2, need to follow ml track.
    - Power mesh for the blocks.
* **Project 3 : Custom Cell**
  + **Technology :**3nm and 4nm
  + **Duration :** 4 months
  + **Tool :** Virtuoso.
  + **Roles &Responsibilities:** Floor planning, Routing and Verification.
  + **Challenges:**
    - Floor planning by using area. Draw the layout from scratch.
    - Maintained cell height, routing only with lower metal.
    - Power mesh for the blocks.
    - Need to generate LEF .
* **Project 4 : LN05LPE(DECAP Cells, filler cells and signal cells)**
  + **Technology :** 5nm
  + **Duration :** 4 months
  + **Tool :** Virtuoso.
  + **Roles & Responsibilities:** Floor planning, Routing and Verification.
  + **Challenges:**
    - Floor planning by using LEF.
    - Taken care of the LATCHUP. Need to check density.
    - Power mesh for the blocks.
* **Project 5** : **LDO**
  + **Technology :** 10nm
  + **Duration :** 2 months
  + **Tool :** Virtuoso
  + **Roles & Responsibilities:** Floor planning, power planning, Routing and Verification.
  + **Challenges:**
    - Power FET floor planning and placement of ngcon2.
    - Taken care of STI, WPE & LATCH up effect.
    - We need to follow metal width depends upon current rating mentioned.
    - Power mesh for the blocks.
* **Project 6 : pbnand\_v**
  + **Technology :** 7nm FinFET.
  + **Duration :** 3 months
  + **Tool :** Virtuoso
  + **Role & Responsibilities:** Floor planning, power planning, Routing and Verification.
  + **Challenges:**
    - Floor planning of sub blocks and working on verification flows.
    - Placement of blocks based on DRC and power supply to maintain power isolations.
    - Working on verification flows namely DRC/LVS/DFM etc to achieve high quality layout deliveries.
* **Project 7 : OP-AMP**
  + **Technology :** 10nm FinFET
  + **Duration :** 2 months
  + **Tool :** Virtuoso
  + **Roles & Responsibilities:** Floor planning, power planning, Routing and Verification.
  + **Challenges:**
    - Floor planning of sub blocks and working on verification flows.
    - Resistor and capacitor matching techniques and guard rings placed around active sensitive transistors.
    - Taken care of Latchup& Antenna effect.
* **Project 8 : Standard Cells**
  + **Technology :** 14nm
  + **Duration :** 4 months
  + **Tool :** Virtuoso
  + **Roles & Responsibilities:** Floor planning, power planning, Routing and Verification.
  + **Challenges:**
    - Drawing the layouts in optimized way using only metal1, maintained a cell height in terms of metal2 pitches and PR Boundary following strict Layout guidelines and DRC rules for each cell.
    - Adjusting the width of NMOS and PMOS transistors to meet the standard cell size, the issues of standard cells size is resolved by Transistor finger/folding technique.
    - Area of the layout is reduced by proper floorplan, which reduced the parasitic of the device routing.
* **Project 9 : Primitive Cells(Analog)**
  + **Technology :** 4nm
  + **Duration :** 1 month.
  + **Tool :** Virtuoso
  + **Roles & Responsibilities:** Floor planning, power planning, Routing and Verification.
  + **Challenges:**
    - Manually we need to draw layers and there is no XL connectivity for primitive cells.
    - Matching for current mirror and Diffpair.

**Training:**

* + Trained in Institute of Silicon Systems, Hyderabad.
  + **Training:** TSMC 130nm & GF 45nm. (Aug 2017 - Dec 2017)
  + **Learning:** 
    - Designed Standard cells like AND NAND NOR MUX & D-FF in TSMC 130 nm tech.
    - Designed LEVEL SHIFTER OP-AMP, BGR (BAND GAP REFERENCE) DAC (Digital to Analog converter) & PLL in GF 45 nm.

**Role:** Lead the team for PLL design.

**Academic Background:**

* Master of Technology at MEGHA college of Engineering & Technology for women Ghatkesar, JNTUH (2013-2015), Embedded Systems , Aggregated : 75%
* Bachelor of Technology at Jyothishmathi college of Engineering & Technology Shamirpet,JNTUH (2009-2013).Electronics and Communication Engineering, Aggregate: 65%
* 12th at Vijayasai Junior College, Bodhan, Nizamabad (2007-2009). Percentage: 89%
* 10th Standard at ZPHS Kalher, Medak (2007). Percentage: 79%

**Personal Details:**

Date of Birth : 12 July 1992

Father’s name : G.Ramulu

Mother’s name : G.Susheela

Languages Known : English, Hindi, and Telugu.

Present location : Bangalore

Nationality : Indian

Marital status : Married

**Declaration:**

I hereby declare that the above mentioned details are true to the best of my knowledge and belief.

Bhagyalaxmi G