–

UNIVAC, CDC 6600 vs ARM
A Match of Existence

Rhea Mae V. Edwards

CS 472
Fall 2017

——————————— ✦ ———————————

TABLE OF CONTENTS

1 INTRODUCTION

From a programmer's view, there are many similarities and differences between many computer architectures that have been developed throughout the years. This paper will discuss a handful of those many similarities and differences between two computer architectures, the Advanced RISC (Reduced Instruction Set Computer) Machine (ARM) versus the Universal Automatic Computer (UNIVAC), Control Data Corporation (CDC) 6600 series [1][2]. Such similarities and differences can include, but not limited to, "the processor's power, performance and area by determining the pipeline length, levels of cache" and more [3]. Overall, the purpose for all of these varying architectures are pretty much the same, being the basis of it all within a computer, but the story of how these architecture designs go on in reaching that common purpose, is the where such unique creativity shows.

1.1 ARM Architecture

The ARM architecture is found in every ARM processor, where its a "uniform register file load/store architecture, where data processing operates only on register contents, [and] not directly on memory contents". This architecture is more modern being built with transistors. In addition, such an architecture is represented to be more broad in its range of performance, being more efficient and advanced with its implementations and techniques. "Implementation size, performance, and low power consumption" are attributes of the ARM architecture of what it better represents. [4]

1.2 UNIVAC, CDC 6600 Architecture

The UNIVAC, CDC 6600 series architecture is considered more of a historical device, where its first origins data back into 1965. This architecture are built also with transistors and employing the ones-complement concept, which dates back to its previous integrate creations back more than 30 years into the past. Speaking more about the CDC 6600 past, its successor of the CDC 1604 is known to be "one of the first commercial transistor-based computers" and "fastest machines on the market," and in relation to the CDC 6600, being greatly known for in regards to its existence. [2]

1.3 Similarities

Similarities these architectures share are their general implementation and considerations of the memory hierarchy and addressing of physical and logical memory.

In addition, the more well known and purposeful computer architectures were digital rather analog, in other words mechanical, in regards to their general structure of them. Even though the ARM architecture and the CDC 6600 architecture had their physical differences of the uses of transistors versus vacuum tubes, they were digital devices.

The memory hierarchy consist of the levels of L_1 cache, L_n/LLC (Last Level Code) cache, main memory (RAM), and tertiary storage (hard drive), with the addition of registers before these stages.

Also, when it comes to paging and addressing of physical and logical memory with a system, the idea with their page tables are implemented similarly.

1.4 Differences

Differences between the ARM architecture and the CDC 6600 architecture include their implementations of the concepts of a RISC designed architecture and "a ones-complement representation of integers" and their implementation of the CPU pipeline [2].

In regards to the the ARM architecture, the implementation of "the RISC design philosophy" is used, whereas the CDC 6600 ended up employing "a ones'-complement representation of integers" [2]. More in regards to RISC designed architecture, there is more emphasizes on the software side where data processing moves from register-to-register, LOAD and STORE independent instructions [4].

In addition, being somewhat related to this difference, more in relation to just the RISC architecture design itself, (Complex Instruction Set Computers) CISC architecture. Unlike RISC architecture's "low cycles per second, large code size, and spend[ing] more transistors on memory register," the CISC architecture has "small code sizes, high cycles per second, and" uses transistors for storing complex instructions instead. The CISC architecture also has more "emphasis on hardware" being more memory-to-memory with its LOAD and STORE incorporated instructions, along with multi-clock complex instructions whereas RISC architecture is single-clock with reduced instructions only. [4]

In regards to the CPU pipeline, the execution follows with the same concept of parallelism. When it comes to a single instruction, there is a flow, starting with an instruction fetch for a single instruction, followed by decoding the instruction, fetching its correspond operands, executing the instruction, and finally storing those operands. Within the CPU pipeline, there is a form of overlap that more efficiently goes through these general instructions in general. Also, the option of running these processes are the use of p-threads within execution.

There is the RISC I Pipeline that is more practiced by the CDC 6600 architecture, and the the RISC II Pipeline, also known as parallelism which is practiced by the ARM architecture. This difference show a variance in their development and implementations for their flow in flow control, affecting and displaying their performances overall.

1.5 Conclusion

When comparing the ARM architecture and UNIVAC, CDC 6600 architecture, there are similarities and differences that exist between the two, but the common goal of being the basis of a computing device, are met with both of these architectures. When it comes to flow control, physical and virtual memory storage, and how the architecture is constructed and processed in general, there is similar purpose for any of them.

REFERENCES

[1] armDeveloper. (2017). *Arm CPU architecture* . [Online]. Available:
https://developer.arm.com/products/architecture/cpu-architecture

[2] Revolvy. (2017). *CDC 6600* . [Online]. Available:
https://www.revolvy.com/main/index.php?s=CDC%206600&item_type=topic

[3] armDeveloper. (2017). *Overview of The Arm Architecture* . [Online]. Available:
https://developer.arm.com/products/architecture/learn-about-the-arm-architecture

[4] C. Chen, G. Novick, K. Shimano. (2000). *RISC ARCHITECTURE* . [Online]. Available:
https://cs.stanford.edu/people/eroberts/courses/soco/projects/risc/risccisc/