Homework #6

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1) Arithmetic Circuits

5.1 Delay Times for 64-Bit Adders

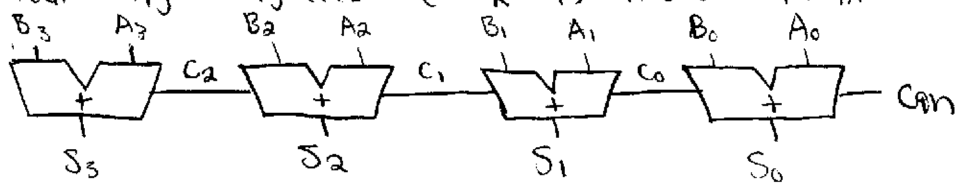
Two-Input Gate Delay = 150 ps
Full Adder Delay = 450 ps

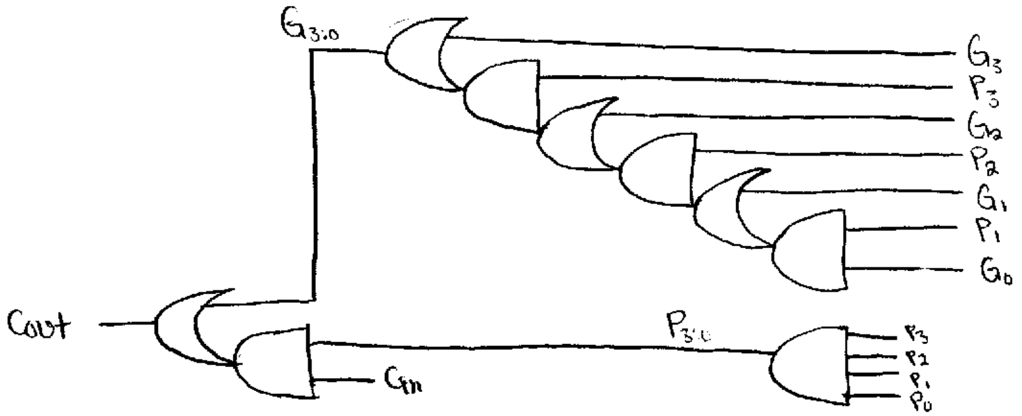
a) A Ripple Carry Adder

$t_{ripple} = N t_{FA}$ $\quad t_{ripple} = 64(450)$ $\quad \boxed{t_{ripple} = 28800 \text{ ps}}$

b) A Carry-Lookahead Adder with 4-Bit Blocks

$t_{CLA} = t_{pg} + t_{pg\text{-}block} + \left(\frac{N}{k} - 1\right) t_{AND\text{-}OR} + k\, t_{FA}$





$t_{CLA} = 150 + 6(150) + (64/4 - 1)(2 \times 150) + 4(450)$

$\boxed{t_{CLA} = 7350 \text{ ps}}$

c) A Prefix Adder

$t_{PA} = t_{pg} + \log_2 N (t_{pg\text{-}prefix}) + t_{XOR}$ ← only have to wait for one of the XOR Gates

↑ rows $\quad$ ↑ 2-Gate Delay Each Row

$t_{PA} = 150 + 6(2 \times 150) + 150$ $\quad \boxed{t_{PA} = 2100 \text{ ps}}$

5.2 Comparing a 64-Bit Ripple Carry Adder and a 64-Bit Carry-lookahead Adder

- only Two Input Gates Used

Static Power Negligible

Two-Input Gate $= 15\,\mu m^2$

$= 50$ ps delay

$= 20$ fF total gate capacitance

<u>64-Bit Ripple-Carry Adder</u>

$64(7 \text{ gates}) = 448$ Gates

<u>64-Bit Carry-Lookahead Adder</u>

$16(47 \text{ gates}) = 752$ Gates

a) Operating at 100 MHz and 1.2V, Area, Delays, Power

Area:

$A_{ripple} = 448(15)$

$A_{ripple} = 6720\,\mu m^2$

$A_{CLA} = 752(15)$

$A_{CLA} = 11280\,\mu m^2$

$$\boxed{A_{ripple} < A_{CLA}}$$

Delay:

$t_{FA} = 3(50) = 150$ ps

$t_{ripple} = 64(150)$

$t_{ripple} = 9600$ ps

$t_{CLA} = 50 + 6(50) + (64/4 - 1)(2 \times 50) + 4(150)$

$t_{CLA} = 2450$ ps

$$\boxed{t_{ripple} > t_{CLA}}$$

Power:

$P = \frac{1}{2} C V^2 f$

$P_{ripple} = \frac{1}{2}\left((448 \times 20 \times 10^{-15})(1.2)^2(100 \times 10^6)\right)$

$P_{ripple} = 0.00064512$ W

$P_{CLA} = \frac{1}{2}\left((752 \times 20 \times 10^{-15})(1.2)^2(100 \times 10^6)\right)$

$P_{CLA} = 0.00108288$ W

$$\boxed{P_{ripple} < P_{CLA}}$$

b) The Ripple-Carry Adder is smaller and requires less power when compared to the Carry-lookahead Adder but it does take longer to process due to its longer delays. The Carry-lookahead Adder may be bigger and requires more power, but it is also faster when compared to the Ripple-Carry Adder.

5.3 Designer Decisions

A designer might choose a ripple-carry adder instead of a carry-lookahead adder bc it requires less space and less power; even though it may take a little bit longer to process due to its longer delay time. Maybe the designer is designing a calculater where physical space and less usage of power consumption may seem more important over the length of time it takes for the device to calculate.

2) Interview Questions

5.1 Largest Possible Result

Multiplying Two Unsigned N-Bit Numbers

$$\begin{array}{r} 111 \\ \times\ 111 \\ \hline 110001 \end{array} \quad \begin{array}{r} 1111 \\ \times\ 1111 \\ \hline 11100001 \end{array} \quad \begin{array}{r} 11 \\ \times\ 11 \\ \hline 1001 \end{array} \quad \begin{array}{r} 11111 \\ \times\ 11111 \\ \hline 1111000001 \end{array}$$

(3-bit) (4-bit) (2-bit) (5-bit)

3 → 49 (7^2) 4 → 225 (15^2) 2 → 9 (3^2) 5 → 961 (31^2)

$$\boxed{\text{Largest Possible Result} = (2^n - 1)^2}$$

What is the largest possible result when adding two unsigned N-bit numbers?

$$\begin{array}{r} 11 \\ +\ 11 \\ \hline 110 \end{array} \quad \begin{array}{r} 111 \\ +\ 111 \\ \hline 1110 \end{array} \quad \begin{array}{r} 1111 \\ +\ 1111 \\ \hline 11110 \end{array} \quad \begin{array}{r} 11111 \\ +\ 11111 \\ \hline 111110 \end{array}$$

(2-bit) (3-bit) (4-bit) (5-bit)

2 → 6 (2·3) 3 → 14 (2·7) 4 → 30 (2·15) 5 → 62 (2·31)

$$\boxed{\text{Largest Possible Result} = 2(2^n - 1)}$$