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ECE 375

LAB 6 PRELAB

1. *Polling Method*: When a processor checks for change in the status.

   Interrupt Method: When an external event send a signal to the processor and makes the processor do something.

   With an anti-lock braking system in a car that constantly checks for inputs, would be a situation when you would use the polling method.

   When a user clicks on the mouse for a computer, would be a situation when you would use the interrupt method, because a mouse click interrupts the processor with a command.

2. *EICRA*:

   The initial value defines INT3:0 as low level interrupts.
   Bits 7…0 – ISC31, ISC30 – ISC00, ISC00: External Interrupt 3 – 0 Sense Control Bits
   3 to 0 are external pins when the SREG I-flag is set, bit 7 – 0 are ISC bits

   EICRB:

   Bits 7…0 – ISC71, ISC70 – ISC41, ISC40: External Interrupt 7 – 4 Sense Control Bits
   Bits 7 – 0 are ISC bits and bits 7 – 4 are sense control bits.
   External interrupts are activated by bits 7 – 4 if the SREG I-flag and interrupt mask is set.

   EIMSK:

   Bits 7…0 – INT7 – INT0: External Interrupt Request 7 – 0 Enable
   Bits 7 – 0 are INT bits and external interrupt bits.

3. An *interrupt vector* is an address in the program memory associated with the interrupt.

   Timer/Counter0 Overflow: $0020
   External Interrupt 5: $000C
   Analog Comparator: $002E

4. a) *Rising Edge Detection*: 5 – 6 and 17 – 18

   b) *Falling Edge Detection*: 2 – 3 and 8 – 9

   c) *Low Level Detection*: 3 – 5 and 9 – 17

   d) *High Level Detection*: 0 – 2 and 6 – 8 and 18 – 21