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                               (b) Convert 101111101.101; to decimal, octal, and hexadecimal.

    (c) Convert 326.5, to decimal, binary, and hexadecimal.
    (d) Convert F3C7 A<sub>26</sub> into binary, octal, and decimal.

                               Show the entire convention process.
           (a) 369.3125<sub>10</sub> comists of a integer part (369) and a fraction part (0.3125).
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(c) To obtain decimal
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    326.5_2 \Rightarrow 11.010.110 : <math>191_2 = 11010110.101_2
    To obtain becadesimal
    326.5_0 \implies 11010110.101_2 \implies 1101.0110 : 1010_2 = 26.4_{16}
(d) There are many ways to do this. To obtain decimal, we do the following
    F3C7.A_{40} \Rightarrow 15*16*3*16*12*16*7*16**10*16***62407.625,
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FAC7.A_m = 1111.0011.1100.0111.1010₁ Once we have binary, we can easily convert it to octal $1.111.001.1111.000.1111.101.0_1 = 171707.5_8$



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EX1: Contents of Rd is read from the register file by providing Rd to rA. The immediate value K is routed to input-B of the ALU by setting MA to 0. Then subtraction is performed but nothing is written back to the register file. The condition flags, N,Z,V,C ect will be set based on the United Higgs, N,Z,V,C etc. will be set based of the outcome of the subtraction operation. All other control signals can be don't cares except DM_w, SP_en, and PC_en which need to be 0 to prevent overwrite. IR_en can be don't care since it's the last execute cycle

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This instruction is nearly identical to condition Branch instruction, except the PC is always updated with the target address. PC+1 in NPC is added with the 7-bit sign-extended PC-relative displacement by setting MUXF to 0, MUXG to 01, and Adder_f to 00. The target address is then latched onto the PC by setting PC to 1 (and setting both PCh and PCI to 0's). All other control signals can be don't cares except SP_en, RF_wA and RF_wb, which are 0 to prevent overwrite. IR_en can be don't care

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EX1: The contents of Yh and Yl are read from the Register File by providing Yh and Yl to rA and rB, respectively. Yh:Yl or Y is routed to DMAR by setting MH to 0. At the same time, Y is incremented by one by the address adder by setting ALU_F to 10 1010 via MUXG and then latched onto YH and YI via MUXC by setting RF_wA and RF_wB to 1s and providing Yh and YI to wA and wB, respectively. Don't cares except DM_w, which is 0, and IR_en, PC_en, and NPC_end to 0 to prevent overwrite.

EX2: DMA is routed through MUXE and used to fetch the operand from data memory. The fetch operand is routed through MUXB and MUXC to the inB of the register file and written by setting RF_wB to 1. All others are don't cares except PC_en and SP_en, which are 0 to prevent overwrite

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EX1: Content of SP is routed to input-A of the address adder by setting MG to 00, and incremented by setting Adder_fto 01.
Incremented PC is then latched onto SP by setting SP_en to 1.
Don't cares, except DM_w, IR_en, and PC_en, set to 0 to prevent overwrite

overwrite

EQ: Content of SP is routed to input-A of the address Adder by setting MG to 00, and incremented by setting MG to 00, and incremented by setting Adder _f to 0.1.

Data memory location pointed to by SP, let, MSP, which is higher byte of the return address, is read by providing SP as an address to data memory by setting ME to 0 and DM, f to 1. Read address to data memory by setting ME to 0 and DM, f to 1. Read with setting MS and address to data memory by setting ME to 0 and DM, f to 1. Read by setting MS and DM and DM, end to 1. Read SM and DM and DM and DM, end to 1. Read DM and by setting MUMUX to 1 and PCL, en to 1 Don't cares except DM, w. IR, en and PCL, en to 1 Don't cares except ER3: Data memory located pointed to by S, P84 (b, MSP) which is the lower byte of the return address, is read by providing SP as an address to the data memory by setting ME to a MOM PC to 1. Read value is their rotted to DEMIX to the lower byte and MDP to 1. Read value is their rotted to DEMIX to the lower byte of PC, is, PC is setting DUMEX to 1 and PC, en to 1. Don't cares, except DM, van dPC, en, which are 9 to represent overwrite.

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EXI	DMAK + SP, SP + SP	1
EX2	M[DMAR] - Rr	

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EX1: rA gets Zh and rB gets Zl to read from register file. This gets latched onto the PMAR register, by setting MH to 0. IR_en, DM_w, PC_en, and SP_en is set to 0 to prevent overwrites. Everything else should be I don't care.

EX2: Program memory gets read to PMAR by setting ML to 1, which is then sent to MDR. IR_en, DM_w, PC_en, and SP_en is set to 0 to prevent overwrites. Everything else is I don't care.

EX3: R0 gets MDR by setting MC to 10 and RF_wB to 1. DM_w, PC_en, and SP_en should be set to 0 to prevent overwrites. Everything else should be I don't care.

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EX1: SP needs to provide the address for data memory, so ME is set to 0. MI is set to 0 because of RAR1. To be written, MD is set to 0 and DM, wis set to 1. Adder f is set to 10 for count, and SP_en is set to 1. IR, en and SP_en is set to 0 for overwrites.

Everything else is I don't care.

EX2: SP needs to provide the address for data memory, so ME is set to 0. Since RARh is selected instead, MI must be 1 but MD and DM_w remains Instead, Mindsu de Dout Markin Own, We thank the same because it still gets written. Again decrement count by setting Adder_f to 10 and SP_en to 1.7 and 27 are read in form the register file, which is sent to PC by setting MH to 0, MJ set to 11, and PC_en to 1. Everything else should be I don't care.

[30 ph]

1. Consider the longitumments of the Lot. onl. — K. (Lond Judeous and Pro-decreesest) instruction on the exchanged, AVS distinguis.

(2) Lot not explain the sequence of numeroparations required to implement Lot 164, —4.

(3) Lot is and explain the terminal signals and the Regional Actions Lapse (RAL) output for file Lot 164, —4.

(4) Lot is and explain the terminal signals and see Regional Actions Lapse (RAL) output for file Lot 164, —4.

Now that the Longoration Science red expense critical (RAL) and TEXE; Cannot signals for the Perth crytic are given feelow. Clearly explain your reasonable.

ETT: DNAR - 30:30 - 1, 30:30 - 10:31 - 1 ETC: Rd = MEMARE

Coutrol	B	28.84	
Signals	4	200	100
MJ	100	88	31
MR	- 0		
ML	.0.		
27,46			
PC_86	-1		6
PGE 46	- 0		
PCL #8	. 0		0
SSC 4s.	_1_	-	1
57,44	- 6		
DEMUX			
MA	1.		
103		1	1
ALU_f	\$1000	REEL	3333
MC	22	183	30.
RF WA			E
Mr. at	.0	1	- 1
MD			
ME	. 1	1.1	
D06.1	1	1	
DOG W	.0.		- 6
MF	1	1.1	
MG	35	-10	.53
Addm_f	44	10	NA.

EAL trape	EX.	1
5.3	- 5	
+3	10	114
16.	- 55	- 4
0.		

EX1: Contents of Xh and Xl are read from the register file by providing Xh and Xl to rA and rB, respectively. Xh:Xl is dcremented by one by the address adder by Xh.XI is deremented by one by the address adder by setting Adder, for 10 via MIXXC by setting bother, for 10 via MIXXC by setting both RF_wA and RF_wB to 15 and providing Xh and XI to wA and vB, respectively. X is routed to DMAR by setting HM to 1. Don't cares except DM_wto 0 and IR_en, PC_en, and NPC_en to 0 to prevent overwrite.

EX2: DMAR is routed through MUXE and used to Etch the operand from data memory. Fetch operand is routed through MUXB and MUXC to the inB of the register file and written by setting RF_wB to 1. Don't cares except PC_en and SP_en to 0 to prevent overwrite.

Consider the implementation of the later wat, we optioned between well Displacement (Displacement (D

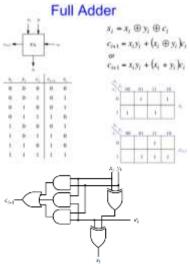
B B + MRL K + K + MC - K - C MA - RC - I

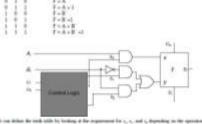
EXX. 2003.8 — Y-q. Setting the papers on pluning the distinct compand by Y-q and the Child.8: EXX. Exx. 100003.40. Limiting the ratios propert in the Y-q and the distribution regime:

Combtd.	-		
Ngodo		170	680
ME	- 1		
IR.mi	1	1	-
R. m	1	- 0	
19°C (20)	1		
105			80
36A		-	1
1-01	. 58	80.	88.
MA MA MB ALU J	-	1850	2500
ИС			
101	28	+	
EF, m.h.		- 4	
87.×8		-	- 1
NE	2		1
142	W		
DNL:	1	-	-
CHE_W_			
Addr. F.		- 10	15.
1401		+	
146	1.		- 1
M)	- 100	86	-m-
29562			-



ESA: To still the question to talking support X on team provise both, values to the 16 feet ALT places in the interpret. The only went't can be one operand to the ALT in the property AUTAL commands to the consensation wate. First the stips (TE) and then COT will become of the properties are parameted to the ALT to the region (TE) and the consensation wate. First the stips (TE) and then COT will become of the properties are parameted to the ALT to the ALT to the stips of the stips of the commands of the ALT to the ALT to the stips of ALT to compare to the stips (TE) and the stips of the ALT the question of the counted in the TE ALT to ALT to expect of the ALT they counted the counted in the TE ALT to ALT to the stips of the ALT they counted the counted in the TE ALT to ALT the ALT TO ALT THE ALT TO the counted in the TE ALT TO ALT THE ALT THE ALT THE ALT THE of the ALT THE ALT THE ALT THE ALT THE ALT THE ALT THE of the ALT THE ALT

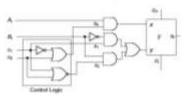




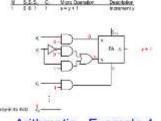
m	•				. 04	7.
ĸ.	-4-		Skettike	- 4-	-1	-4
r			F = A + S	- 1	. 6	-7
۰	٠		FeArkel	. +		. 6
			F+A		4	
ь.	1		Francis			-
ĸ.			Page .			
		1	F-F-L			
ï			F=A+W			п
À.		4.	Fake Will		- 4	- 4



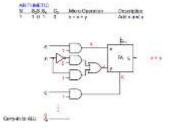




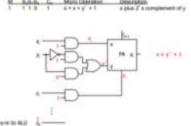
Arithmetic - Example 1



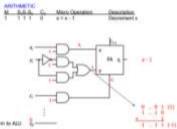
Arithmetic - Example 4



Arithmetic - Example 6



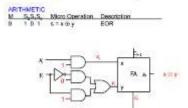
Arithmetic - Example 7



Logic - Example 2

022	Ł.
*TDD-	FR. A
C.D.D	e .
«—D—	

Logic - Example 6



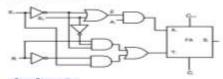
я.	X.	-6.	Dynasiee
			F=A+0
	-	4.	F-A-B-1
ь.			F = A
ь.		4.	F + A + 5
	- 10	-	F = BC
	- 0		$F = B^* = 1$
		46	V = A - D
	100		F = A + B' +1











Carry Propagation

- 2' is complement to the best.
 1' is complement to the best.
 1' is complement to twice 35 long.
 Significant delay reduction using carry look sheet concept.
 Significant is to code: we would have to be gate on eye to be strongly best and on the gate.
 Significant is not concept.

- c, * a, * bc.

 1.8 Sup.

 1, * 4 S. + 6 C.

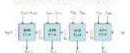
 1, * 4 S. + 6 C.

 1, * 6 Sup.

 1, * 7 Sup.

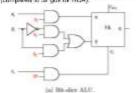
 1, *

- - Cascade CLA Adder



Total dolay:

- count detay: = 1 gd for g is and g is for r = 0, 1, ..., m-1= 2 gd $a \ge 1$ or a_1, a_2, a_3 = 2 gd $a \ge 1$ or a_3, a_4 (other a_3 is excellable) = 2 gd $a \ge 1$ or $a_3 \ge 1$
- For m CLA stages, total delay = 3 + 2m. For m=4, 11, gds (compared to 32 gds for RCA).



M	555	G.	Micro Operation	Department.
.1	0.5 1	9	279+1	incomment y
11	B 1 B	+	8+9+1	Z's complement y
.1	T 8 D	. 9.7	528+5	bionement a
	7.0.1		27279	Add curdy
	1.1.0	100	67479	splay Thousanderself of b
1	1.1.0	1	62849.41	spkip 2's complement of y
	5 1 1	- 80	2-1-1	Decorried si

M. 8-8-8. Micro Operation Description

	0.0.0	2 - 0	in ICall
11	0.0.1	5-Y	transfer y
11	D 1 0	2 - Y	Comp y
11	D 1.1.	a = 1	Seed
0	1 0 0	5-1	Transfer a
11	1.0.1	5 = 300V	±198
.0	1 1 0	5 - 0059//	ENOR
m.	1 1 4		Create w

(e) Logic operations aim to following AVI immedia of

MELIA_ILOSF: is A. A. is the type of A operand is B. Y. the type of B operand is B. Y. The type of B. Y. The The The Type of B. Y. The The The The Type of B. Y. The The The The The Type of B. Y. The
--

(ii) Time all holo and room are 2 cycles each, we only for the requiring instruction

Non-papilinel.
The first and enterior cycles for each instruction are found below. Now for the branch instruction or execute cycle is used regardless if the branch is taken or not. This is because papilinely in and enable any given instruction cannot be feethed each the instruction proceeding it has completed the elector or

And wi	MIN	Pents	EX.	Total
14	L. 11			
14	E, T	15	3.7	- 1
med	4,1		- 2:	
18	A, Tr.	2.	- 2	3.
14	E, 8+			
Add:	630 A	1		- 2
adir	1764 F.			
1.6	A, 1	1.0	- 1	3.
adic .	A, seco			
91.	1, 5	1	3.1	3.
99.	-5, 494		-7	
48.	-l, 111	1 1	2.0	
MICH.	10715, 1			_
fer	ilerg			
N/Am	MOLIA TLICE			- 1

Statution .		Tena	EX.	799
24	4. E-		1	- 3
14	5, T:		1-3	1.2
80.5	1.1			
14	A., E+		- 1	
54	2, 8+	-	1.2	
+01	Alta, A.			
ader	194. 9	17.4		1 1
18	K. T.	-	1.7	1.1
edit	A. seco		- 1	1.1
4/5	1, A	-		
1/1	-E, 151		1.3	1.7
875	-A. 130		- 2	1.7
artice	26-25, 1		- 1	1.2
DNC	Living		- 1	1
brown	MISSA TSONY			

With pipelining, the small estables of system is some \mathcal{D}_{i}

On The performance improvement is 60-27-46 + 121 + 10-99.