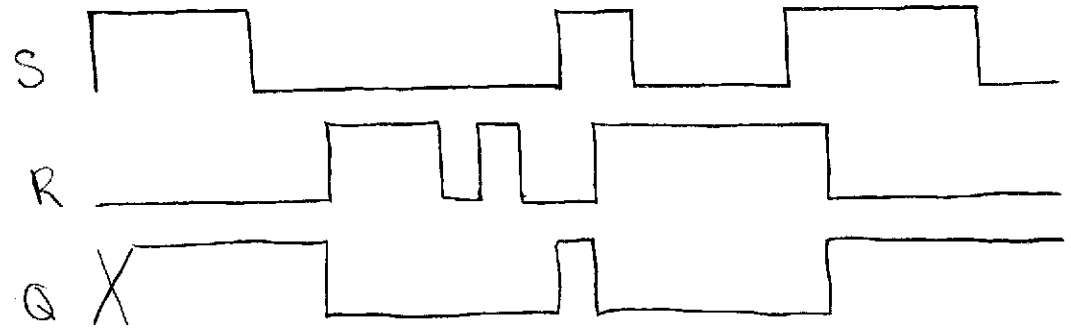
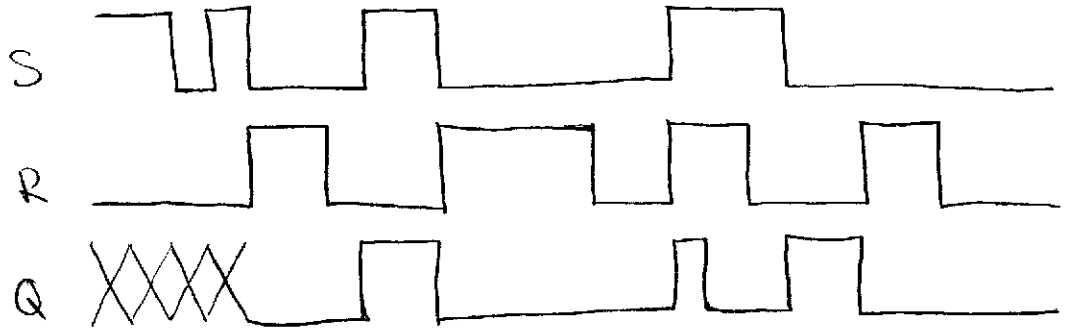
Homework 3

Rhea Mae Edwards
Student ID #
982-389-303

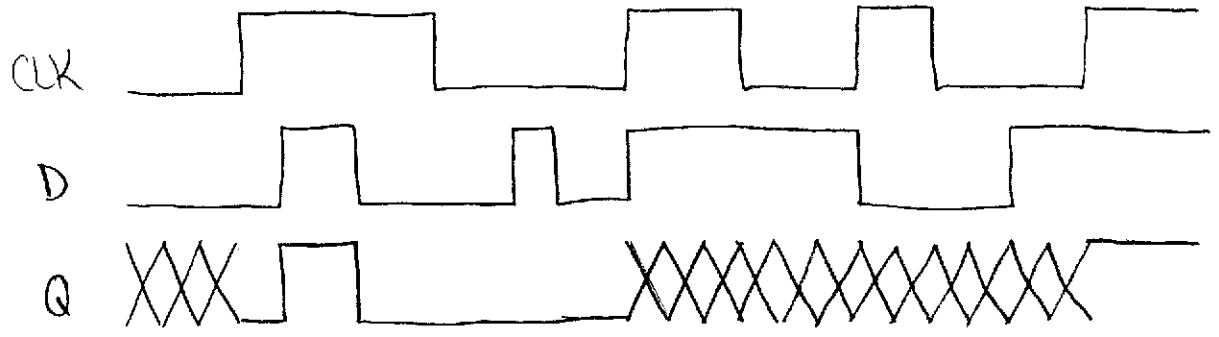
3.1 Figure 3.61 Output Q of an SR Latch



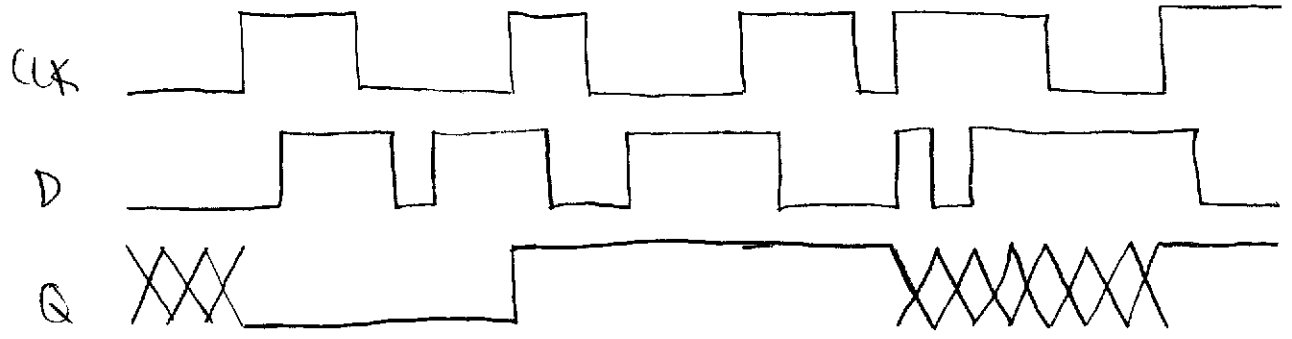
3.2 Figure 3.62 Output Q of an SR latch



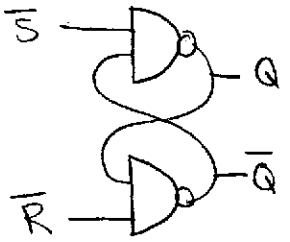
3.3 Figure 3.63 Output Q of a D Latch



3.4 Figure 3.64 Output Q of a D Latch



3.7 Figure 3.65



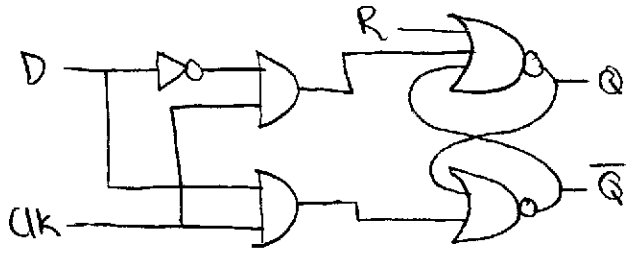
Sequential logic circuit, since the outputs depend on previous inputs.

$\overline{S}=0$ and $\overline{R}=1$ $Q \rightarrow 1$
$\overline{S}=1$ and $\overline{R}=0$ $Q \rightarrow 0$
$\overline{S}=1$ and $\overline{R}=1$ Circuit remembers old value
$\overline{S}=0$ and $\overline{R}=0$ $Q \rightarrow 1$ and $\overline{Q} \rightarrow 1$

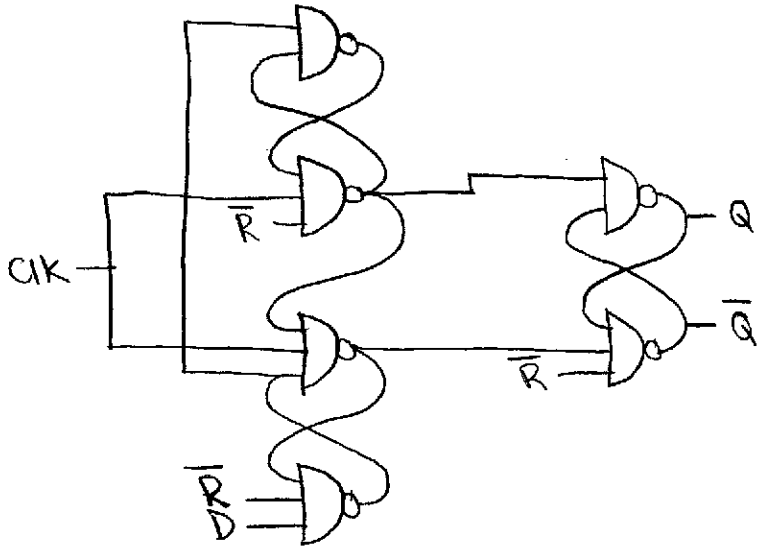
Circuit = Active Low SR Latch

2) Sequential Timing

3.12 Asynchronously Resettable D Latch



3.13 Asynchronously Resettable D Flip Flop



3) Finite State Machines

3.19 Elevator for Building with "25 Floors", No Floor 13...

The elevator controller must have a minimum of 5 bits of state to represent the 24 floors that the elevator might be on.

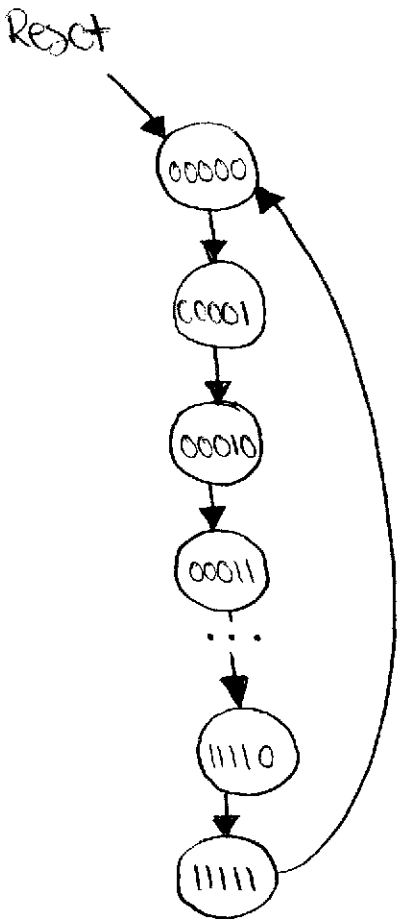
4) Interview Questions

3.3 A Latch Versus A Flip-Flop

The difference between a latch and a flip-flop depends on what triggers the hardware and its size.

A latch is preferable in two-phase clocking systems, with two clocks.
A flip-flop is preferable in systems with a single clock.

3.4 5-Bit Counter Finite State Machine



$$S_4 = S_4 \oplus S_3 S_2 S_1 S_0$$

$$S_3 = S_3 \oplus S_2 S_1 S_0$$

$$S_2 = S_2 \oplus S_1 S_0$$

$$S_1 = S_1 \oplus S_0$$

$$S_0 = \overline{S_0}$$

$$Q_{4:0} = S_{4:0}$$