Homework 4

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1) Latches and Flip-Flops

3.35 Xilinx Spartan 3 FPGA

$t_{PD} = 0.61$ ns
$t_{CD} = 0.30$ ns
(for each CLB)

$t_{PD} = 0.72$ ns
$t_{CD} = 0.50$ ns
(for each flip-flop)

$t_{setup} = 0.53$ ns
$t_{hold} = 0$ ns

a.) How many consecutive CLBs between two flip-flops?

$f = 40$ MHz

$f = \frac{1}{T}$ $T = \frac{1}{f}$

No clock skew and no delay through wires between CLBs

$T = T_{CCQ} + T_{PD} + T_{setup}$

$T = \frac{1}{40} = 25$ ns

$25 \geq 2(0.72) + x(0.61) + 0.53$

$25 \geq 0.61x + 1.97$

$-1.97 \quad -1.97$

$\frac{23.03}{0.61} \geq \frac{0.61x}{0.61}$

$x < 37.75$

37 CLBs

b.) How much clock skew can FPGA have w/out violating hold time?

All paths between flip-flops pass through at least one CLB

$t_{HOLD} > t_{CCQ} + t_{CD}$

$t_{SKEW} < (t_{CCQ} + t_{CD\_CLB}) - t_{HOLD}$

$t_{SKEW} < (0.5 + 0.3) - 0$

$t_{SKEW} < 0.8$ ns

$t_{SKEW} = 0.8$ ns

3.38 The Unfortunate Encounter in the Metastable State

$P = e^{-t/T}$ (probability of remaining in state)

T = Response Rate = 20s (due to lack of sleep)

a) Time to resolve from metastability?

Until 99% certainty of resolution

$P = 0.01$

$0.01 = e^{-t/20}$

$\ln(0.01) = \ln(e^{-t/20})$

$\ln(0.01) = -t/20 \cdot -20$

$t = -20 \cdot \ln(0.01)$

$t = 92.1\ s$

$\boxed{t = 92\ s}$

b) Probability lab partner drag you to the morgue?

$t = 3\ \text{mins} = 180\ s$

$P = e^{-180/20}$

$P = 1.23 \times 10^{-4} = 0.000123$

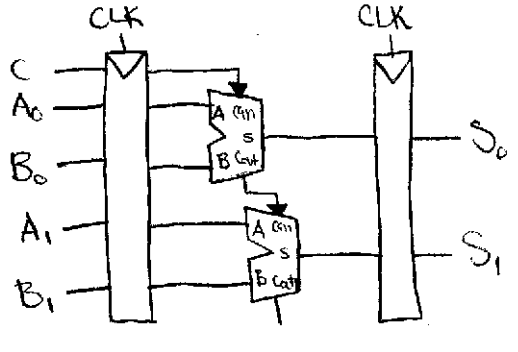
$\boxed{P = 0.0123\%}$

2) Sequential Timing

3.34 An Adder for the Blindingly Fast 2-Bit Pentium Processor

$C_{in} \rightarrow C_{out}$	$t_{PD} = 20$ ps	$t_{CD} = 15$ ps	$t_{setup} = 30$ ps	
$C_{in} \rightarrow Sum$	$t_{PD} = 20$ ps	$t_{CD} = 15$ ps		
$A \rightarrow C_{out}$	$t_{PD} = 25$ ps	$t_{CD} = 22$ ps	$t_{Hold} = 10$ ps	
$B \rightarrow C_{out}$	$t_{PD} = 25$ ps	$t_{CD} = 22$ ps		
$A \rightarrow Sum$	$t_{PD} = 30$ ps	$t_{CD} = 22$ ps	$t_{PCQ} = 35$ ps	
$B \rightarrow Sum$	$t_{PD} = 30$ ps	$t_{CD} = 22$ ps	$t_{CCQ} = 21$ ps	

(For the Adder) (For Each Flip-Flop)



a) No clock skew, maximum operating frequency of circuit

$f = \frac{1}{T}$ $T = t_{PCQ} + t_{PD} + t_{setup}$

- slowest path through logic (2 Stage Delay)

$A_0, B_0 \rightarrow C_{out} = 25ps$ $t_{PD} = 45ps$
$C_{in} \rightarrow Sum = 20ps$

$T = 35 + 45 + 30 = 110\,ps$
$f = \frac{1}{110} = 0.0091 = 9.1 \times 10^{-3}$

$\boxed{f = 9.1 \times 10^{-3}\ MHz}$

b) Clock skew circuit can tolerate at 8 GHz

$t_{skew} < T - t_{PCQ} - t_{PD} - t_{setup}$

$f = 0.008\ MHz$ $T = \frac{1}{0.008} = 125ps$

$t_{skew} < 125 - 110$ (calculation shown in previous part)

$t_{skew} < 15ps$ $\boxed{t_{skew} = 15ps}$

c) Clock skew circuit can tolerate before might experience hold violation

$t_{skew} > (t_{CCQ} + t_{CD}) - t_{Hold}$ = Experience Hold Violation

- Fastest path through logic

$C_{in} \rightarrow Sum = 15ps$ $t_{CD} = 15ps$

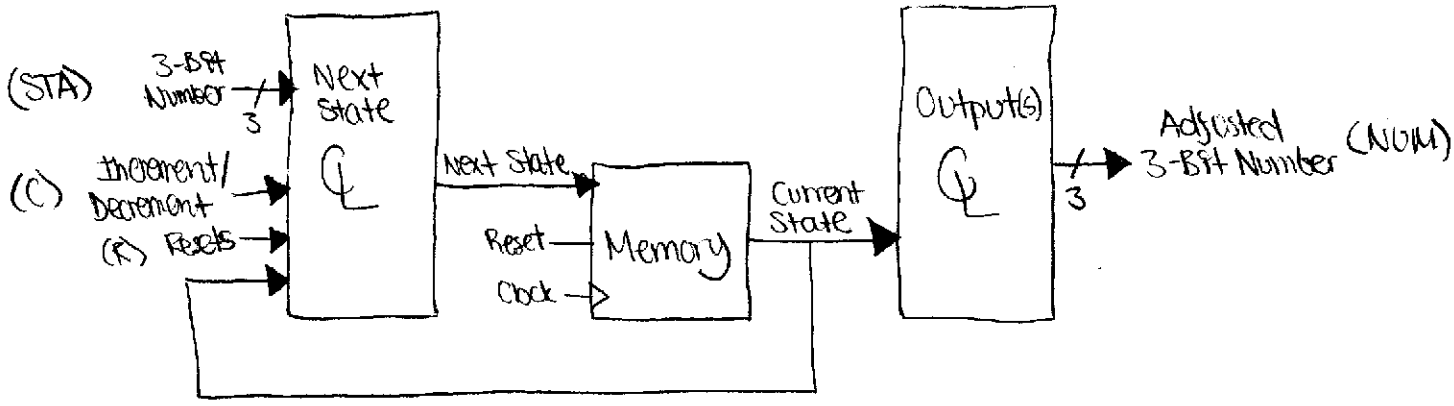
$t_{skew} > (21 + 15) - 10$

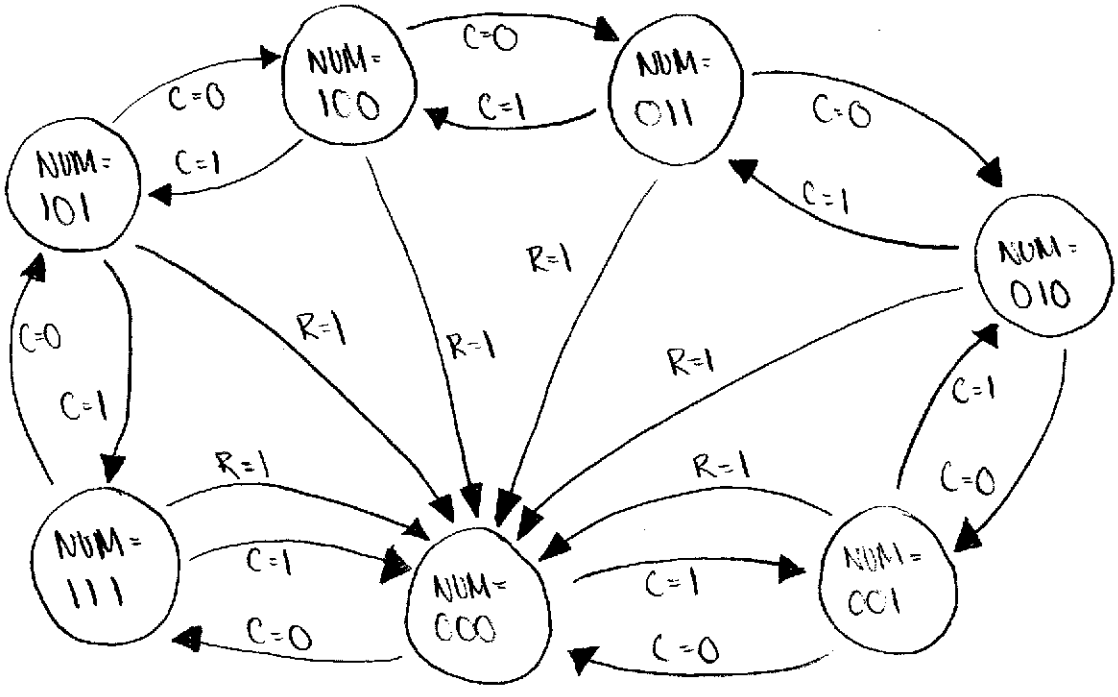
$t_{skew} > 26\,ps$

$\boxed{t_{skew} = 26\,ps}$

3) Finite State Machine

Develop State Machine for a 3-Bit Up Down Counter.
Include all 7 Steps State Machine Process
One Input controls whether counter ingrements or decrements.
An Asynchronous Reset to clear count to zero

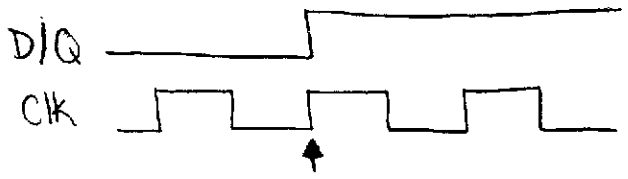


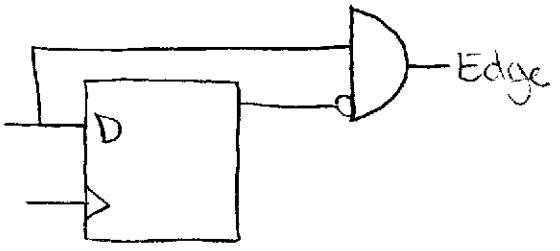


4) Interview Questions

3.5 Design an Edge Detector Circuit

Output HIGH for one cycle after Input makes a 0 → 1 transition





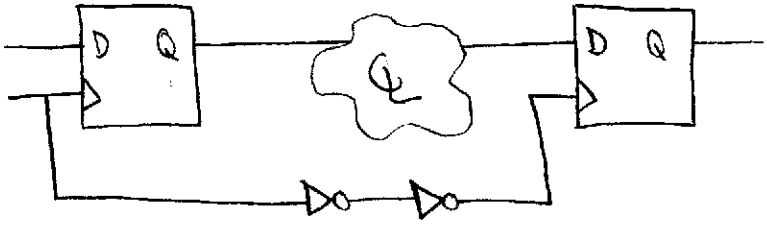
- Pick a rising edge (0 → 1 transition)

Don't need a full state machine neccessary, just a small device

3.6 Concept of Pipelining

Overall, pipelining in a while is just (or is) an assembly line, where data through the process moves at the same time perfectly. There are blocks of combinational logic in series where between each block there is a block/section of memory, which ideally contains and moves the data along the process correctly and efficiently. It is used for the overall sake of sequential timing for a given logically process. It makes the overall process run efficiently and quickly as each block of combinational logic specializes in a certain line of thinking/reason. Data to run smoothly and quickly.

3.9 A Block of Logic Between Two Registers



$$t_{PD} \leq T - (t_{PCQ} + t_{setup}) \rightarrow t_{PD} \leq T + t_{CD\_BUFFER} - (t_{PCQ} + t_{setup})$$

Setup time gets better since not much more time is needed for the device to setup without qualifying for a setup violation. The skew is induced, giving more time for t_{PCQ} logically also.