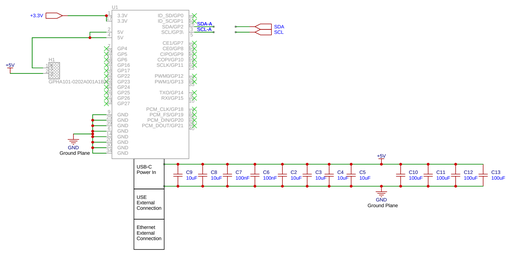

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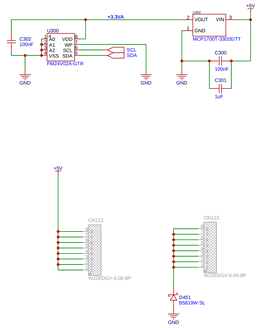


* This sheet provides power input, decoupling, and I2C connection to the Raspberry Pi.

* Power is supplied via USB-C and externally accessible +5V net.
  - Local filtering includes multiple decoupling capacitors across +5V and GND.
  - Capacitor values include 10uF, 100nF, and 100uF types for a wide frequency response.
  - All capacitors are referenced to a solid ground plane.

* The +3.3V I2C bus is connected to the Raspberry Pi header.
  - Pull-up resistors (3.3kΩ) are provided on SDA and SCL lines.
  - I2C lines connect to GPIO2 (SDA) and GPIO3 (SCL) on the Pi.

* Raspberry Pi 40-pin header is used.
  - Only essential pins are shown connected (power, I2C, GND).
  - Remaining pins are left unconnected for clarity.

* External +5V is routed through header H1 (pin 1 = +5V, pin 2 = GND).

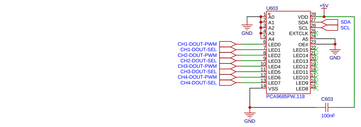
* All unused GPIO and power pins on the Pi header are shown unconnected (crossed).

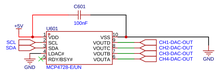
* Decoupling capacitor placement is designed to minimize voltage ripple on the +5V rail.

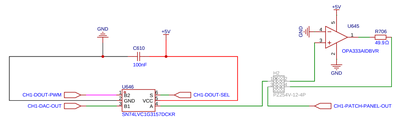
* GND is a shared plane for I2C, decoupling, and Pi ground connections.

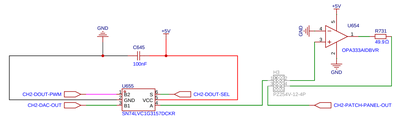
* Series resistor placeholder. Populate with 0Ω or 33 – 68Ω if signal integrity issues arise.

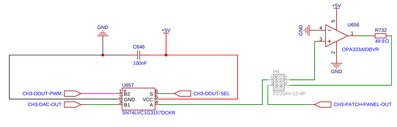
Schematic	Schematic1	Create at	2025-08-18
		Update at	2025-09-07
Board	Main	Page	Main
Drawn		Practice 4 layer	
Reviewed			
	Version	Size	Page 1 Total 5
EasyEDA	V1.0	A4	EasyEDA.com

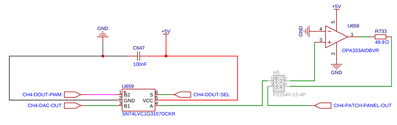












* This schematic defines four analog output channels with flexible signal selection, op-amp buffering, and ESD protection routed to a labeled patch panel.

* The MCP4728 DAC (U601) provides four independent analog voltage outputs (CH1 – CH4).
  - I2C-controlled; fixed address default is 0x60 (EEPROM can be used to reassign).
  - Output range: 0 to 5V referenced to GND.
  - Local bypass capacitor (C601 = 100nF) stabilizes the supply.

* The PCA9685 PWM controller (U603) supplies four PWM outputs and four select lines.
  - I2C address set to 0x40.
  - Channels LED0,2,4,6 provide PWM signals (CHx-DOUT-PWM).
  - Channels LED1,3,5,7 control signal selection (CHx-DOUT-SEL).
  - Duty cycles can be set to 0% or 100% for use as digital outputs.
  - Decoupling capacitor (C603 = 100nF) placed at VDD.

* Each channel includes an SPDT analog switch (U646 – U649, SN74LVC1G3157DCKR).
  - B1 input receives CHx-DAC-OUT.
  - B2 input receives CHx-DOUT-PWM.
  - S input is driven by CHx-DOUT-SEL (from PCA9685).
  - S = 0 selects DAC (analog), S = 1 selects PWM (digital).
  - Local decoupling capacitors (C610 – C613, 100nF) stabilize each switch.

* The selected signal is buffered by a precision op-amp (U645 – U648, OPA333) configured for unity gain.
  - Provides low-impedance drive suitable for analog or digital outputs.
  - Series resistor (49.9Ω) on each output adds protection and improves signal integrity.
  - H2 - H5 Provide an option to include the op amp or bypass it.
    - Jumping 1-2 & 3-4 will include the op amp in the output circuit
    - Jumping 1-3 will bypass the op amp entirely

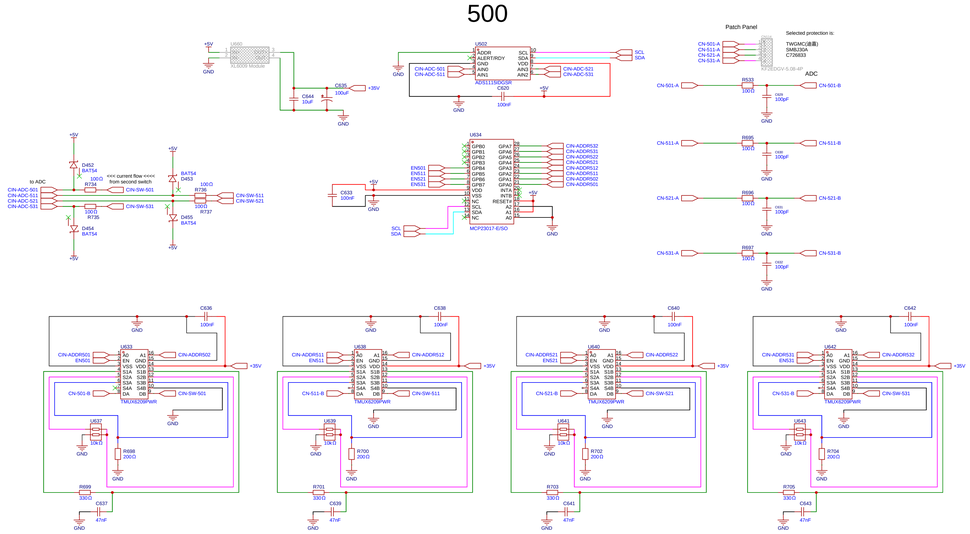
* Outputs are routed to a 4-pin patch panel connector (CN111).
  - Each channel output is labeled CHx-PATCH-PANEL-OUT.
  - Connector part: KF2EDGV-5.08-6P, labeled “ Analog Out Patch Panel ”.

* ESD protection is provided on each output using unidirectional TVS diodes (D441 – D444, PESD5V0S1UL).
  - Designed for ESD transient suppression to IEC 61000-4-2.
  - Clamping behavior protects against brief high-voltage events.
  - Diodes are placed near the connector to suppress external transients.

* Ground is shared across DAC, PWM, switching, and analog output stages.
  Proper layout isolation is recommended to minimize cross-domain noise coupling.

* This design enables software-defined analog output routing:
  - Use DAC for stable analog voltage output.
  - Use PWM or static logic for digital control signals.
  - Outputs are selectable per channel, with seamless runtime switching.

Schematic	Schematic1	Create at	2025-08-27
		Update at	2025-09-07
Board	Main	Page	Analog Out
Drawn		Practice 4 layer	
Reviewed			
		Version	Size	Page 2 Total 5
EasyEDA		V1.0	A4	EasyEDA.com



DRAWING NOTES – SHEET 500 (INPUT PROTECTION AND SWITCH ROUTING)

* This circuit protects and routes 4 analog input channels from a patch panel through a selectable analog conditioning path and into a shared ADC.

* Signals enter from the patch panel at headers CN-501, -511, -521, and -531.

* Each signal passes through a 100Ω series resistor to limit inrush and fault current.

* Schottky diodes (D452 – D455, BAT54) clamp each signal to the +5 V rail:
  - Diodes are placed after the 100Ω resistor to safely shunt overvoltage events.
  - Forward voltage is ~0.3 V, providing early clamping around 5.3 V max.

* Clamped signals continue through labeled nets CIN-SW-501 through CIN-SW-531 to analog switches (TMUX6209).

* Signals are routed via the selected switch to a signal conditioning circuit:
  - Options include direct voltage, 2:1 divider, 4 – 20 mA loop, or ground sense.
  - Only one path is active per input channel at a time.

* After conditioning, signals are routed through a second switch stage and finally into the ADC (ADS1115) for digitization.

* The 100Ω series resistors:
  - Limit current into the BAT54 clamp during faults.
  - Provide high-frequency damping.
  - Have negligible effect on signal quality at ADC sampling rates.

* This configuration protects the ADC and muxes from accidental overvoltage, miswiring, or unexpected signal conditions.

* Clamp strategy assumes inputs remain above GND; reverse protection is not implemented.

PROGRAMMER NOTES – SHEET 500: ANALOG INPUT SYSTEM

* The TMUX6209 (U633) is controlled via 3 digital signals: A0, A1, and EN.
  - These are driven by GPIO pins from the I²C GPIO expander \(MCP23017, U634\).
  - The EN signal should be deasserted (LOW) before changing A0/A1 to avoid glitches or mid-switch artifacts.
  - Wait at least 10 µs after switching before sampling to allow analog settling.

* Only one signal conditioning path should be active at a time per channel.
  - Valid selections: 00, 01, 10, or 11 (see conditioner map in software).
  - EN must be HIGH to activate the selected signal path.

* The ADS1115 \(U502\) is configured over I²C and supports 4 single-ended inputs \(AIN0 – AIN3).
  - Address is fixed at 0x48.
  - Use single-shot mode unless fast continuous conversion is required.
  - Default full-scale range is ±6.144 V; set to ±4.096 V or lower for best resolution with 0 – 5 V inputs.
  - Configure MUX bits to select the correct AINx channel.
  - Use 860 SPS for quick response or 128 SPS for higher noise immunity.

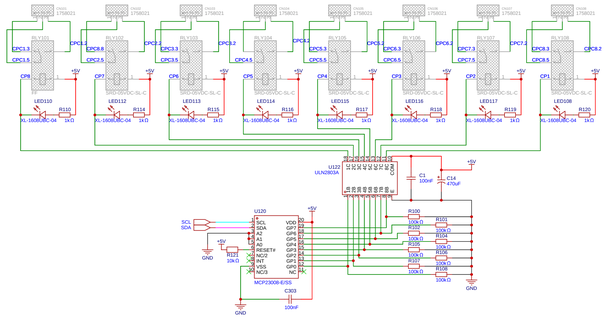
* Current loop inputs (4 – 20 mA path):
  - Use software scaling: 4 mA = 0 V; 20 mA = V_burden (typically 2 V).
  - Apply calibration factors in firmware to correct for resistor tolerances.

* Calibration and Filtering:
  - Optional RC filters (~10 kHz cutoff) are present at analog outputs of conditioner paths.
  - Additional digital filtering (e.g. IIR or EMA) is recommended in firmware to reject noise or jitter.

* Power-On State:
  - Ensure all EN signals are LOW at power-on.
  - Do not leave multiple conditioning paths active simultaneously — this may cause signal contention or distortion.

Schematic	Schematic1	Create at	2025-08-30
		Update at	2025-09-07
Board	Main	Page	P4
Drawn		Practice 4 layer	
Reviewed			
		Version	Size	Page 3 Total 5
EasyEDA		V1.0	A4	EasyEDA.com

Subsystem 100



Drawing Notes — Relay Driver Circuit

* This sheet defines the relay driver circuit, including relay control, flyback protection, indicator LEDs, and I²C interface to the MCP23008 GPIO expander.

MCP23008 GPIO Expander (U120)
* The MCP23008 provides 8 GPIO lines via the I²C interface.
* I²C address is set to 0x20 via address pins A2, A1, A0 \(all tied LOW\).
* External 10kΩ pull-ups on SDA and SCL are required if not already provided elsewhere on the bus.
* A 100nF decoupling capacitor (C303) is placed near VDD.
* GPIOs default to Hi-Z input mode at power-up. Until firmware configures the pins as outputs, they are not actively driven.

Relay Driver and Inversion Behavior
* GPIO outputs from the MCP23008 are connected to the ULN2803A Darlington array (U122), which drives eight 5V relay coils.
* The ULN2803A is electrically inverting:
  - Input HIGH → Output LOW (GND)
  - Input LOW → Output floating (open)
* In this configuration, the relay coils are connected between +5V and ULN outputs, so the circuit behaves logically non-inverting:
  - MCP output HIGH → Relay ON
  - MCP output LOW → Relay OFF

Startup Behavior and Pull-Down Resistors
* At startup, the MCP23008 GPIOs are not yet configured, and remain in Hi-Z state.
* 100kΩ pull-down resistors (R100 – R108) are placed on the inputs of the ULN2803A, ensuring that the ULN inputs are held LOW during this time.
* This prevents unintended relay activation before firmware takes control and ensures relays are OFF at boot.

Firmware Programming Requirements
* Firmware must:
  1. Configure MCP23008 GPIOs as outputs: IODIR = 0x00
  2. Optionally initialize output latch register: OLAT = 0x00 to start with all relays OFF
  3. Use GPIO writes to control relays:
     - Write 1 (HIGH) → Relay ON
     - Write 0 (LOW) → Relay OFF

Relay and LED Circuitry
* Relay Type: SRD-05VDC-SL-C
  - 5V coil
  - SPDT contacts
  - Coil resistance: ~70Ω
* Each relay drives an indicator LED (LED110 – LED117) in parallel with the coil, via a 1kΩ series resistor (R110 – R117), illuminating when the relay is ON.
* The ULN2803A includes internal flyback diodes, protecting against inductive spikes from the relay coils.

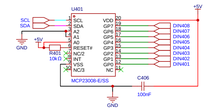
Terminal Blocks and Contact Isolation
* Each relay ’ s output is routed to a 3-pin terminal block (CN101 – CN108).
* Relay contacts are electrically isolated from control and logic sections.
* Contact naming follows the CPCx.y convention:
  - Example: CPC1.3 = Relay 1 NC contact

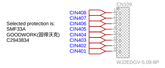
Power and Decoupling
* Relay coils are powered from +5V via ULN2803A.
* Local decoupling:
  - C1 = 100nF ceramic
  - C14 = 470µF electrolytic
  - Both placed near U122 to ensure supply stability during relay switching

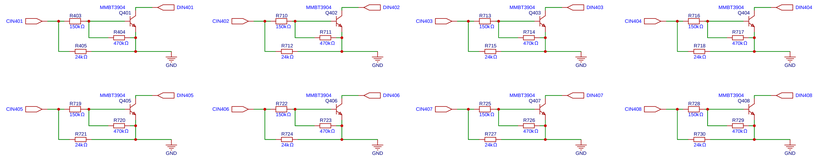
Grounding and Power Plane Notes
* Logic, relay drivers, and relay coils share a common GND.
* PCB layout should isolate high current relay paths from noise-sensitive logic and I²C traces.
* If needed, use local copper fills or stitching vias to create a return path with low inductance near the ULN outputs.

Schematic	Schematic1	Create at	2025-09-03
		Update at	2025-09-05
Board	Main	Page	P5
Drawn		Practice 4 layer	
Reviewed			
	Version	Size	Page 4 Total 5
EasyEDA	V1.0	A4	EasyEDA.com

400







* This sheet defines 8 isolated digital input channels, protected and level-shifted for monitoring via I2C.

* Input connector CN109 receives 8 external digital signals (CIN401 – CIN408).
  - Each input line is protected with a SMF33A TVS diode to ground.
  - TVS clamps only above ~36V, suitable for 24V or higher industrial systems.
  - Inputs are filtered and routed through individual level-shift circuits.

* Each input line (CIN401 – CIN408) is processed by a discrete NPN transistor stage (Q401 – Q408).
  - Transistor type: MMBT3904
  - Input resistor: 150kΩ (limits input current)
  - Base divider: 150kΩ / 24kΩ to set logic threshold near 5V
  - Pull-down resistor: 470kΩ ensures input goes low when unconnected
  - Outputs (DIN401 – DIN408) are open-collector logic-level signals

* Processed outputs (DIN401 – DIN408) feed into the MCP23008 GPIO expander (U401).
  - MCP23008 address pins (A0, A1, A2) are configured via hard-wired levels to address 0x21
  - I2C interface connects to SDA/SCL and is pulled up externally
  - Decoupling capacitor (C406 = 100nF) is placed near VDD
  - Internal RESET is pulled up via 10kΩ resistor (R401)

* The MCP23008 digitizes the input states for I2C monitoring.
  - Outputs are active-low, reflecting the collector state of each NPN stage
  - 5V logic compatible, shared with host I2C bus

* GND is the reference for all comparator stages and is assumed shared with the incoming signal ground.

* This circuit provides robust overvoltage protection, signal conditioning, and digital isolation for interfacing field-level signals with a microcontroller or embedded system via I2C.

* Programming Notes:
  - Each input pin (DIN401 – DIN408 → GP0 – GP7) should be configured as an **input**:
    - `IODIR = 0xFF`
  - Enable **internal weak pull-ups** (typical 100kΩ, ~25 µs rise time with 50pF\):
    - `GPPU = 0xFF`
  - Input logic is **active-low**:
    - `0 = active/high input`, `1 = inactive/low input`
    - Software should **invert logic** when interpreting input state

Schematic	Schematic1	Create at	2025-09-03
		Update at	2025-09-07
Board	Main	Page	P6
Drawn		Practice 4 layer	
Reviewed			
	Version	Size	Page 5 Total 5
EasyEDA	V1.0	A4	EasyEDA.com