OS Performance Analysis on Intel® Core™2 Duo Processors

- Software and Solutions Group

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Precise Events Based Sampling (PEBS) on Core2

- **Mechanism:**
  - counter overflow arms pebs
  - Next event gets captured and raises PMI
  - Pebs mechanism captures architectural state information at completion of critical instruction
- **Including EIP (+1), even when OS defers PMI**
  - Accurate inst_retired profile

inst_retired.any_p
x87_ops_retires.any
Br_inst_retired.mispred
simd_inst_retired.any
mem_load_retired.dtlb_miss
mem_load_retired.l1d_line_miss
mem_load_retired.l1d_miss
mem_load_retired.l2_line_miss
mem_load_retired.l2_miss

PEBS BUFFER

DS Buffer Managment

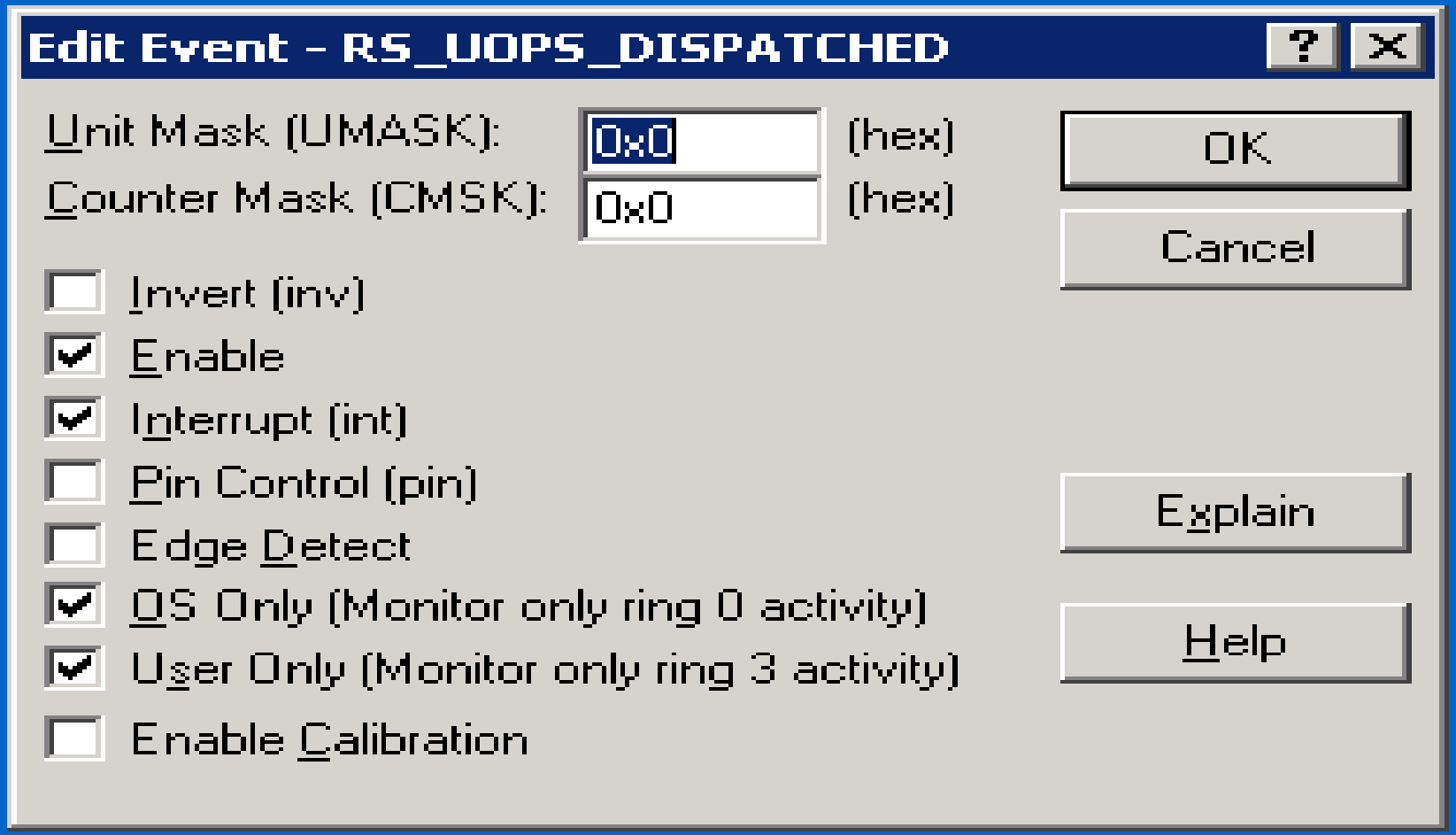
63	BTS Buffer Base	0	0H
BTS Index			8H
BTS Absolute Maximum			10H
BTS Interrupt Threshold			18H
PEBS Buffer Base			20H
PEBS Index			28H
PEBS Absolute Maximum			30H
PEBS Interrupt Threshold			38H
PEBS Counter Reset		0	40H

PEBS Record

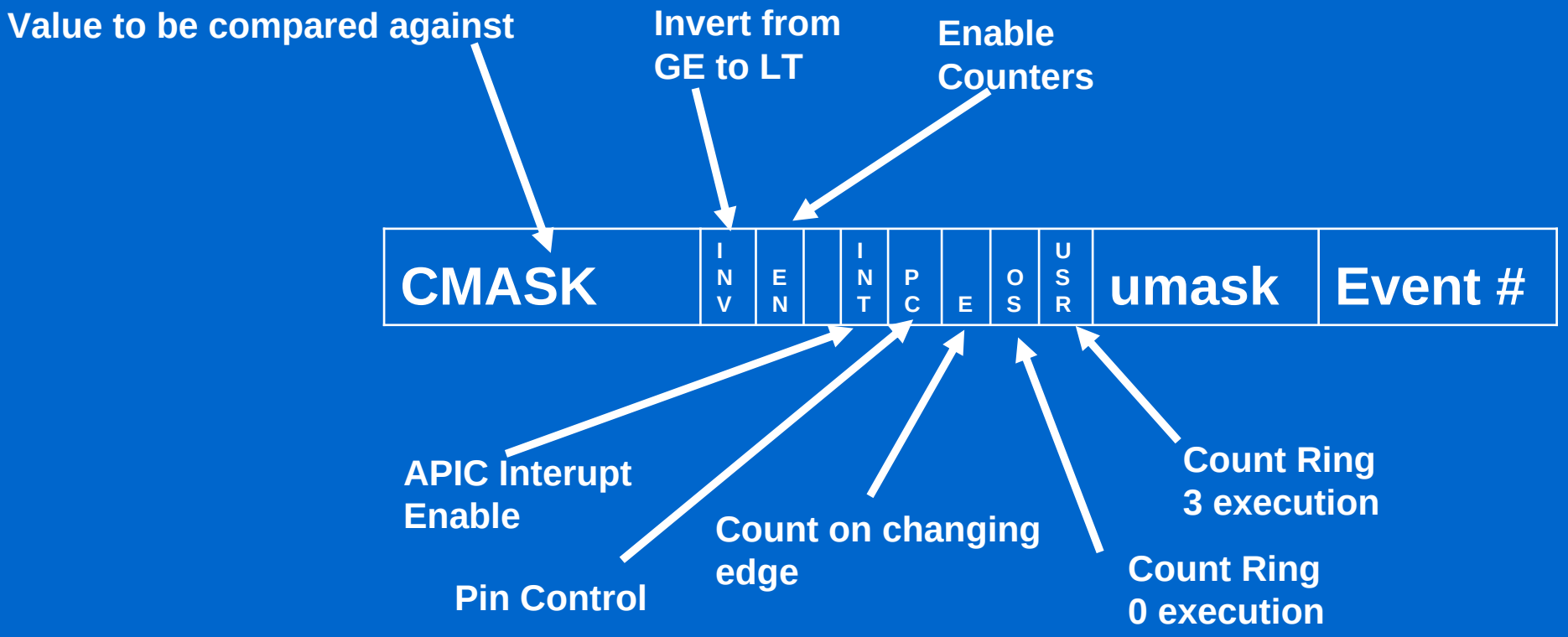
63	RFLAGS	0	0H
RIP			8H
RAX			10H
RBX			18H
RCX			20H
RDX			28H
RSI			30H
RDI			38H
RBP			40H
RSP			48H
R8			50H
~			
R15			88H

Merom/Penryn - Format 0000b

VTune™ Analyzer Edit Event

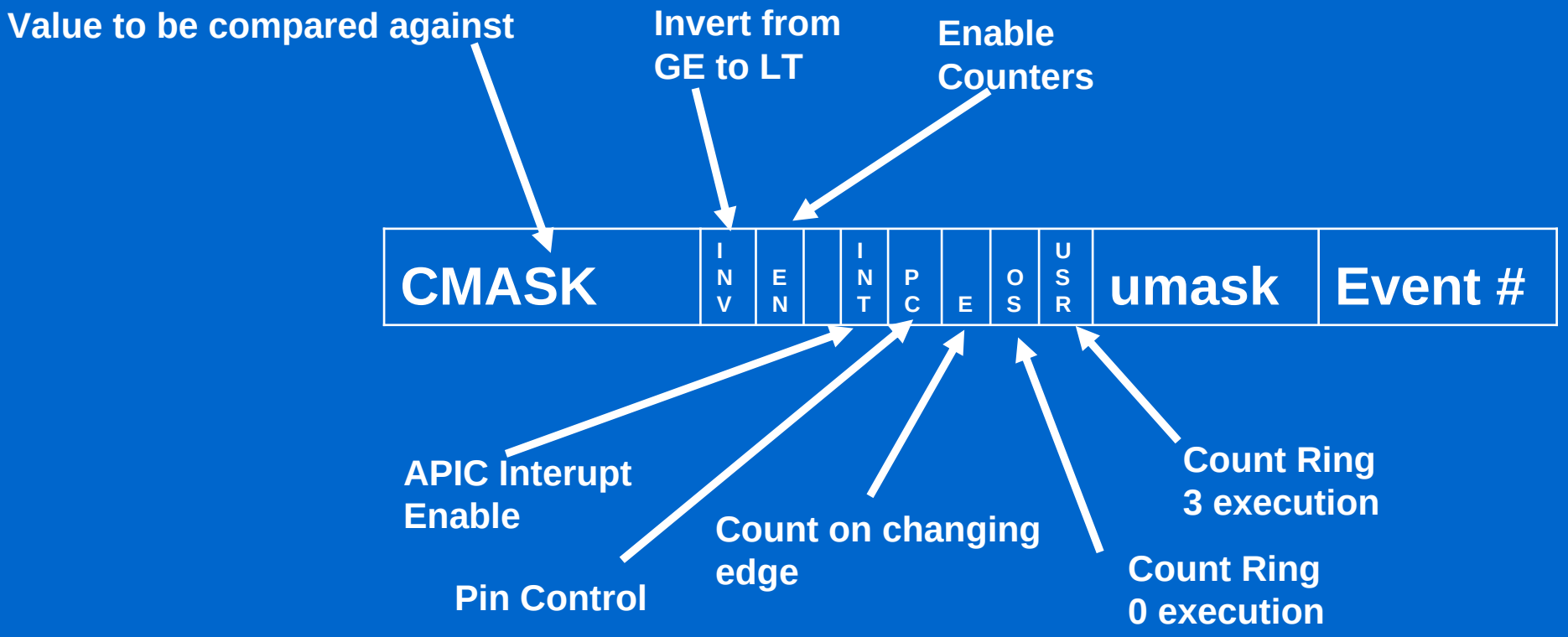


Some Features of the PMU



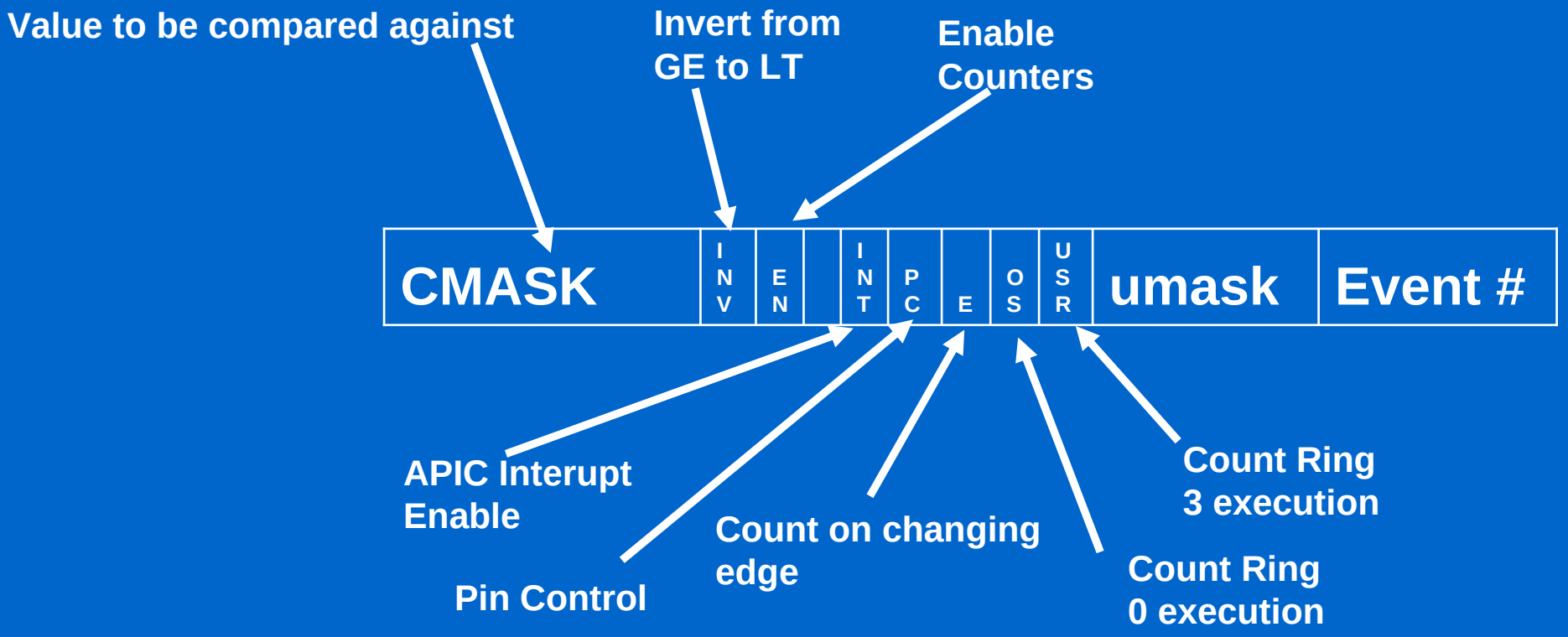
Setting CMASK = 1 and INV = 1 for INST_RETIRED.ANY_P
Counts Cycles Where
no instructions were retired
Even in OS "Critical Sections" where PMI is deferred

Some Features of the PMU



Setting CMASK = 8 and INV = 1 for INST_RETIRED.ANY_P
Counts ALL Cycles
Accurate CPU Cycle Profile for entire OS

Some Features of the PMU



Setting CMASK = 8, INV = 1, OS=1, USR=0 for INST_RETIRED.ANY_P Counts All Cycles in Ring0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