Verification and Validation Report: Measuring Microstructure Changes During Thermal Treatment

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 $March\ 8,\ 2023$

1 Revision History

Date	Name	Notes
Mar 8 2023 Mar 8 2023		Added usability test results Added Traceability matrices

2 Symbols, Abbreviations and Acronyms

change capacity to size

symbol	description
Т	Test

[symbols, abbreviations or acronyms – you can reference the SRS tables if needed —SS]

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This document ... Section 11 Code Coverage Metrics is removed.

- 3 Functional Requirements Evaluation
- 4 Nonfunctional Requirements Evaluation

In the section

4.1 Usability

The table below shows the results of our usability tests based on the tests in the V&V plan based on the requirements mentioned in the SRS. Each requirement can be traced to multiple unit tests and the usability survey used can be found in the Appendix.

Usability Tests					
Test Requirement	Related Unit Tests	Description	Expected Result	Result	
NF-UT1	AF	Completing tasks without additional assistance.	User will be complete tasks successfully	PASS	
NF-UT2	AX	Interact with interace to modify parameters.	User will be able to modify the parameters accurately and quickly.	PASS	
NF-UT3	AL	Completing all tasks with limited number of mistakes	User will be able to complete all tasks with MAX_MISTAKE	PASS	
NF-UT3	AL	Verifying if interacting with the application previously improves ease of use (learnability)	User will be able to complete the tasks more quickly and accurately the second time	PASS	
NF-UT5	AS	Verifying how calculations are performed is hidden	User will not know how calculations are performed after doing the set of tasks	PASS	
NF-UT6	AS	Verifying appropriate application size upon installation	User will install application onto computer and verify that the application size is less than or equal to MAX_SIZE	PASS	

- 4.2 Performance
- 4.3 etc.

5 Comparison to Existing Implementation

This section will not be appropriate for every project.

6 Unit Testing

6.1 Calculation Module

	Unit Tests for Calculation Module					
Unit Test ID	Description	Input	Expected Output	Output	Result	
UT-C1	Testing the getResistance Method	From Hard-wareInput ADT: Voltage = 5, Current = 1	5.000	5.000	PASS	
UT-C1	Testing the getResistance Method	From Hard-wareInput ADT: Voltage = 4, Current = 0.6	6.667	6.667	PASS	
UT-C2	Testing the getResistance Method	From Hard-wareInput ADT: Voltage = -5, Current = 1	Invalid	Invalid	PASS	
UT-C2	Testing the getResistance Method	From Hard-wareInput ADT: Voltage = -4, Current = 0.6	Invalid	Invalid	PASS	
UT-C3	Testing the getResistivity Method	$\begin{array}{rcl} \text{Resistance} & = \\ 3, & \text{Area} & = 2.5, \\ \text{Length} & = 2 \end{array}$	3.750	3.750	PASS	
UT-C3	Testing the getResistivity Method	Resistance = 2, Area = 2.8, Length = 1	5.600	5.600	PASS	
UT-C4	Testing the getResistivity Method	Resistance = A, Area = 2.8, Length = 0	Invalid	Invalid	PASS	
UT-C4	Testing the getResistivity Method	Resistance = 1, Area = 0, Length = BC	Invalid	Invalid	PASS	
UT-C5	Testing the calcResistance Method	$ \begin{array}{rcl} \text{Voltage} &=& 2.6, \\ \text{Current} &=& 2 \\ & 5 \\ \end{array} $	1.300	1.300	PASS	
UT-C5	Testing the calcResis-tance Method	Voltage = 3.6, Current = 2	1.800	1.800	PASS	

	Unit Tests for Calculation Module (Continued)					
Unit Test ID	Description	Input	Expected Output	Output	Result	
UT-C6	Testing the calcResistance Method	$ \begin{aligned} \text{Voltage} &= \text{AB,} \\ \text{Current} &= 0 \end{aligned} $	Invalid	Invalid	PASS	
UT-C6	Testing the calcResistance Method	$\begin{array}{ccc} Voltage &=& 0, \\ Current &=& DR \end{array}$	Invalid	Invalid	PASS	
UT-C7	Testing the calcResistivity Method	Resistance = 2, Area = 1.5, Length = 2	1.500	1.500	PASS	
UT-C7	Testing the calcResistivity Method	Resistance = 1.8, Area = 1.3, Length = 1.5	1.560	1.560	PASS	
UT-C8	Testing the calcResistivity Method	Resistance = AB, Area = 1, Length = 2	Invalid	Invalid	PASS	
UT-C8	Testing the calcResistivity Method	Resistance = 2, Area = 2, Length = NT	Invalid	Invalid	PASS	

6.2 User Input Validation Module

	Unit Tests for User Input Validation Module					
Unit Test ID	Description	Input	Expected Output	Output	Result	
UT-UI1	Testing the ge- tUserInput Method	N/A	UserInput (Samplin- gRate: 60, Sample- Length: 4, Sam- pleWidth:2)	UserInput (Samplin- gRate: 60, Sample- Length: 4, Sam- pleWidth:2)	PASS	
UT-UI2	Testing the validate- FileData Method	FileName: Test, Date: 03/01/2023, Name: Test	TRUE	TRUE	PASS	
UT-UI2	Testing the validate- FileData Method	FileName: Output, Date: 03/01/2023, Name: John	TRUE	TRUE	PASS	
UT-UI3	Testing the validate- FileData Method	FileName: Output, Date: Someday, Name: Tester	FALSE	FALSE	PASS	
UT-UI3	Testing the validate-FileData Method	FileName: 0, Date: 03/01/2023, Name: 0	FALSE	FALSE	PASS	

1	Unit Tests for User Input Validation Module (Continued)					
Unit Test ID	Description	Input	Expected Output	Output	Result	
UT-UI4	Testing	SamplingRate:	TRUE	TRUE	PASS	
	the vali-	50, Sample-				
	dateSam-	Length:2,				
	pleData	Sam-				
	Method	pleWidth:5				
UT-UI4	Testing	SamplingRate:	TRUE	TRUE	PASS	
	the vali-	60, Sample-				
	dateSam-	Length:1.5,				
	pleData	Sam-				
	Method	pleWidth:3				
UT-UI5	Testing	SamplingRate:	FALSE	FALSE	PASS	
	the vali-	-7, Sample-				
	dateSam-	Length:1.5,				
	pleData	Sam-				
	Method	pleWidth:3				
UT-UI5	Testing	SamplingRate:	FALSE	FALSE	PASS	
	the vali-	60,				
	dateSam-	SampleLength:	-			
	pleData	5, Sam-				
	Method	pleWidth:3				

6.3 Hardware Input Validation Module

	Unit Tests for Hardware Input Validation Module					
Unit Test ID	Description	Input	Expected Output	Output	Result	
UT-HI1	Testing the getHard- wareInput Method	-	HardwareInput (Voltage: 5, Cur- rent: 3)	HardwareInput (Voltage: 5, Cur- rent: 3)	PASS	
UT-HI2	Testing the val- idatePa- rameters Method	Voltage: 3.0 , Time: 5:31 PM , Current: 1.0	TRUE	TRUE	PASS	
UT-HI2	Testing the validate- FileData Method	Voltage: 3.2 , Time: 5:45 PM , Current: 1.2	TRUE	TRUE	PASS	
UT-HI3	Testing the validate- FileData Method	Voltage: 10 , Time: 5:48 PM , Current: NY	FALSE	FALSE	PASS	
UT-HI3	Testing the validate- FileData Method	Voltage: YT , Time: 5:51 PM , Current: 0.5	FALSE	FALSE	PASS	

7 Changes Due to Testing

8 Automated Testing

9 Trace to Requirements

Traceability Matrix to Non Functional Requirements						
Requirement	Requirement(SRS)	Test Requirement	Related Unit Tests			
Type						
Non Functional	NFR-U1	NF-UT1	U			
Non Functional	NFR-U2	NF-UT2	U			
Non Functional	NFR-U3	NF-UT3	U			
Non Functional	NFR-U4	NF-UT4	U			
Non Functional	NFR-U5	NF-UT5	U			
Non Functional	NFR-U6	NF-UT6	U			

Traceability Matrix to Functional Requirements						
Requirement	Requirement(SRS)	Test Requirement	Related Unit Tests			
Type						
Functional	FR1	FR-T1	U			
Functional	FR2	FR-T2	U			
Functional	FR3	FR-T3	U			
Functional	FR4	FR-T4	U			
Functional	FR5	FR-T5	U			
Functional	FR6	FR-T6	U			

10 Trace to Modules

References

Appendix — Reflection

The information in this section will be used to evaluate the team members on the graduate attribute of Lifelong Learning. Please answer the following questions:

- 1.
- 2.