Instruction	Details	State	IR_Enable	PC_Enable
Reset	Clear PC	0	0	0
	Get 4	1	0	0
	Npc enable	2	0	0
	NPC disable	3	0	0
Fetch	Get PC in Alu	4	0	0
	MAR enable and RAM Op	5	0	0
	Enable Ram	6	0	0
	Enable IR (Waiting MFC)	7	1	0
	Disable IR	8	0	0
Sethi	Initialize R input and Mux	9	0	0
	Enable Register File	10	0	0
	Disable Register File	11	0	0
Branch	Init for branch	12	0	0
BA_O Anulled	Mux selection PC	13	0	0
	Npc enable	14	0	0
	Npc disable. PC enable	15	0	1
	PC disable	16	0	0
	Npc enable, Mux Select for NPC	17	0	0
	Disable NPC	18	0	0
BA_O	PC_In_Mux	19	0	0
	Pc enable	20	0	1
	PC disable, change ALU Muxes	21	0	0
	Npc enable	22	0	0
	Npc disable	23	0	0
BN_O Anulled	Mux Select for NPC	24	0	0
	Npc enable	25	0	0
	Npc disable. PC enable	26	0	1
	PC disable, NPC enable, Mux Select for NPC	27	0	0
	Disable NPC	28	0	0
BX TRUE	PC_In_Mux	29	0	0
	Pc enable	30	0	1
	PC disable, Mux select	31	0	0
	Npc enable	32	0	0
	Npc disable	33	0	0
BX FALSE Anulled	Alu Mux select	34	0	0
	Npc enable	35	0	0
	Npc disable, pc enable	36	0	1
	Pc disable	37	0	0
	Npc enable	38	0	0
	Npc disable	39	0	0
BX FALSE	PC_In_Mux	40	0	0
	Pc enable	41	0	1
	Pc disable, Alu Mux select	42	0	0
	Npc enable	43	0	0
	Npc disable	44	0	0

Call	Init reg and muxes	45	0	0
	Enable Register File and PC	46	0	1
	Disable reg, do jump	47	0	0
	Npc enable	48	0	0
	Npc disable	49	0	0
Jmpl	Saving PC	50	0	0
	Reg enable	51	0	0
	Reg disable	52	0	0
	PC_In_Mux	53	0	0
	Pc enable	54	0	1
	Pc disable, get rs1	55	0	0
if() Immediate	B immediate	56	0	0
else Register	B register	57	0	0
	Npc enable	58	0	0
	Npc disable	59	0	0
SAVE	Init reg and muxes	61	0	0
if() Immediate	B immediate	62	0	0
else Register	B register	63	0	0
	MDR_Mux	64	0	0
	MDR_enable	65	0	0
	MDR disable, mux select	66	0	0
	PSR_enable	67	0	0
	PSR_disable	68	0	0
	Reg enable	69	0	0
	Reg disable	70	0	0
Restore	Init reg and muxes	71	0	0
	B immediate	72	0	0
	B register	73	0	0
	MDR_Mux	74	0	0
	MDR_enable	75	0	0
	MDR disable, mux select	76	0	0
	PSR_enable	77	0	0
	PSR_disable	78	0	0
	Reg enable	79	0	0
	Reg disable	80	0	0
Arithmetic	Init reg and muxes	81	0	0
if() Immediate	B immediate	82	0	0
else Register	B register	83	0	0
	PSR_mux	84	0	0
	Reg enable	85	0	0
if()Modify Flag	PSR_enable	86	0	0
	Disable PSR & Reg	87	0	0
load	Init reg and muxes	89	0	0
	B immediate	90	0	0
	B register	91	0	0
	Mar enable	92	0	0
	Emable Ram and MDR Mux	93	0	0

	Disable ram	94	0	0
	MDR enable	95	0	0
	Load datum to register	96	0	0
	register enable	97	0	0
	register disable	98	0	0
store	Init reg and muxes	100	0	0
	B immediate	101	0	0
	B register	102	0	0
	Mar enable	103	0	0
	Mar disable, Init MDR	104	0	0
	MDR enable	105	0	0
	MDR disable, store value	106	0	0
	RAM Disable	107	0	0
RDWIM	Check S, (S = 1) Init MuxB	127	0	0
	Enable reg	110	0	0
	Disable	111	0	0
RDTBR	Check S, (S = 1) Init MuxB	112	0	0
	Enable reg	113	0	0
	Disable	114	0	0
RDPSR	Check S, (S = 1) Init MuxB	115	0	0
	Enable reg	116	0	0
	Disable	117	0	0
WRTBR	Check S, Init reg and muxes	118	0	0
if() Immediate	B immediate	118A	0	0
else Register	B register	118B	0	0
	TBR enable	119	0	0
	TBR Disable	120	0	0
WRPSR	Check S, Init reg and muxes	121	0	0
if() Immediate	B immediate	121A	0	0
else Register	B register	121B	0	0
	PSR enable	122	0	0
	PSR Disable	123	0	0
WRWIM	Check S, Init reg and muxes	124	0	0
if() Immediate	B immediate	124A	0	0
else Register	B register	124B	0	0
	WIM enable	125	0	0
	WIM Disable	126	0	0
Trapicc	Check ET, higher priority, and codition	133	0	0
	B immediate	134	0	0
	B register	135	0	0
modifying tt	TBR enable	136	0	0
	TBR Disable, Set PS	137	0	0
	PSR enable	138	0	0
	PSR Disable, enter superivisor	139	0	0
	PSR enable	140	0	0
	PSR disable, disable traps	141	0	0
	PSR enable	142	0	0

	PSR disable, decrement CWP	143	0	0
	PSR enable	144	0	0
Save PC and nPC	PSR disable, Saving PC	145	0	0
	Enable reg	146	0	0
	Disable reg, Saving nPC	147	0	0
	Enable reg	148	0	0
Jump to trap	Disable, PC - > Trap	149	0	0
	Enable PC	150	0	1
	Disable PC, nPC + 4	151	0	0
	Npc enable	152	0	0
	Npc disable	153	0	0
Priority Manager	Ifs and elses	154	0	0
Rett	Check window underflow	155	0	0
	Pc enable	156	0	1
	Pc disable, get opernads	157	0	0
	Enable register, nPC	158	0	0
	Disable registers, decrement CWP	159	0	0
	PSR enable	160	0	0
	Restore S from PS	161	0	0
	PSR enable	162	0	0
	PSR disable, enable traps	163	0	0
	PSR enable	164	0	0
	PSR disable	163	0	0

NPC_Enable	MDR_Enable	MAR_Enable	register_file_enable	RAM_Enable	TBR_enable
0	0	0	0	0	0
0	0	0	0	0	0
1	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	1	0	0	0
0	0	0	0	1	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	1	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
1	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
1	0	0	0	0	0
0	0	0	0	0	0
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1	0	0	0	0	0
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0	0	0	0	0	0
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1	0	0	0	0	0
0	0	0	0	0	0
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0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
1	0	0	0	0	0
0	0	0	0	0	0

0	0	0	0	0	0
0	0	0	1	0	0
0	0	0	0	0	0
1	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
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0	0	0	0	0	0
0	0	0	0	0	0
0	0	1	0	0	0
0	0	0	0	1	0

0	0	0	0	0	0
0	1	0	0	0	0
0	0	0	0	0	0
0	0	0	1	0	0
0	0	0	0	0	0
0	0	0	0	0	0
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0	1	0	0	0	0
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0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	1
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
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0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0

0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	1	0	0
0	0	0	0	0	0
0	0	0	1	0	0
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1	0	0	1	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0

PSR_enable	PSR_Enable	Temp_enable	WIM_enable	TR_PR_enable	extender_select
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	3'b100
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	3'b101
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	3'b101
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
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0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0

0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	2'b11
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
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0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	2'b00
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	2'b00
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	1	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	2'b00
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	1	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	2'b00
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
1	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	2'b00
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0

0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	2'b00
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
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0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	2'b00
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	2'b00
0	0	0	0	0	0
1	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	2'b00
0	0	0	0	0	0
0	0	0	1	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	2'b00
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	1	0	0	0	0
0	0	0	0	0	0
0	1	0	0	0	0
0	0	0	0	0	0
0	1	0	0	0	0

0	0	0	0	0	0
0	1	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
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0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
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0	0	0	0	0	0
0	0	0	0	1	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	1	0	0	0	0
0	0	0	0	0	0
0	1	0	0	0	0
0	0	0	0	0	0
0	1	0	0	0	0
0	0	0	0	0	0

Outputs				
PC_Clear	TR_PR_Clear	PSR_Clear	ALUA_Mux_select	ALUB_Mux_select
1	1	1	0	0
0	0	0	2'b00	3'b110
0	0	0	0	0
0	0	0	0	0
0	0	0	2'b00	3'b011
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	2b'00	3'b001
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	2'b10	3'b110
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	2b'10	3b'110
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	2'b01	3'b001
0	0	0	0	0
0	0	0	0	0
0	0	0	2b'10	3b'110
0	0	0	0	0
0	0	0	0	0
0	0	0	2b'10	3b'110
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	2'b01	3b'b001
0	0	0	0	0
0	0	0	0	0
0	0	0	2'b10	3'b110
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	2'b9	3'b109
0	0	0	0	0
0	0	0	0	0

0	0	0	2'b00	3'b011
0	0	0	0	0
0	0	0	2'b00	3'b001
0	0	0	0	0
0	0	0	0	0
0	0	0	2b'00	3'b011
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	0	3'b001
0	0	0	0	3'b000
0	0	0	0	0
0	0	0	0	0
0	0	0	2'b00	0
0	0	0	0	3'b001
0	0	0	0	3'b000
0	0	0	0	0
0	0	0	0	0
0	0	0	2'b11	2'b111
0	0	0	0	0
0	0	0	2'b00	3'b010
0	0	0	0	0
0	0	0	0	0
0	0	0	2'b00	0
0	0	0	0	3'b001
0	0	0	0	3'b000
0	0	0	0	0
0	0	0	0	0
0	0	0	2'b11	2'b111
0	0	0	0	0
0	0	0	2'b00	3'b010
0	0	0	0	0
0	0	0	0	0
0	0	0	2'b00	0
0	0	0	0	3'b001
0	0	0	0	3'b000
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0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	2'b00	0
0	0	0	0	3'b001
0	0	0	0	3'b000
0	0	0	0	0
0	0	0	0	0

0	0	0	0	0
0	0	0	0	0
0	0	0	0	3'b010
0	0	0	0	0
0	0	0	0	0
0	0	0	2'b00	0
0	0	0	0	3'b001
0	0	0	0	3'b000
0	0	0	0	0
0	0	0	0	3'b000
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	2'b00	4'b1000
0	0	0	0	0
0	0	0	0	0
0	0	0	2'b00	4'b1001
0	0	0	0	0
0	0	0	0	0
0	0	0	2'b00	4'b1010
0	0	0	0	0
0	0	0	0	0
0	0	0	2'b00	0
0	0	0	0	3'b001
0	0	0	0	3'b000
0	0	0	0	0
0	0	0	0	0
0	0	0	2'b00	0
0	0	0	0	3'b001
0	0	0	0	3'b000
0	0	0	0	0
0	0	0	0	0
0	0	0	2'b00	0
0	0	0	0	3'b001
0	0	0	0	3'b000
0	0	0	0	0
0	0	0	0	0
0	0	0	2'b00	0
0	0	0	0	3'b001
0	0	0	0	3'b000
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0

0	0	0	2'b11	4'b0111
0	0	0	0	0
0	0	0	2'b00	4'b0011
0	0	0	0	0
0	0	0	0	4'b0100
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	2'b10	4'b0110
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	2'b11	4'b0111
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0

MDR_Mux_select	PC_In_Mux	TBR_Mux	PSR_Mux	in_PC	in_PA	in_PB
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	IR_Out[29:25]	5'b00000	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	2'b00	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	2'b00	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	2'b00	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0

0	2'b00	0	0	5'b01111	5'b00000	0
0	0	0	0	0	0	0
0	0	0	0	0	5'b00000	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	IR_Out[29:25]	5'b00000	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	2'b00	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	IR_Out[18:14]	0
0	0	0	0	0	0	0
0	0	0	0	0	0	IR_Out[4:0]
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	IR_Out[29:25]	IR_Out[18:14]	0
0	0	0	0	0	0	0
0	0	0	0	0	0	IR_Out[4:0]
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	2'b11	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	5'b00000	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	IR_Out[29:25]	IR_Out[18:14]	0
0	0	0	0	0	0	0
0	0	0	0	0	0	IR_Out[4:0]
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	2'b11	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	5'b00000	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	IR_Out[29:25]	IR_Out[18:14]	0
0	0	0	0	0	0	0
0	0	0	0	0	0	IR_Out[4:0]
0	0	0	2'b00	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	IR_Out[29:25]	IR_Out[18:14]	0
0	0	0	0	0	0	0
0	0	0	0	0	0	IR_Out[4:0]
0	0	0	0	0	0	0
1	0	0	0	0	0	0

0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	5'b00000	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	IR_Out[18:14]	0
0	0	0	0	0	0	0
0	0	0	0	0	0	IR_Out[4:0]
0	0	0	0	0	0	0
0	0	0	0	0	IR_Out[29:25]	5'b0000
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	1b'0	0	IR_Out[29:25]	IR_Out[18:14]	0
0	0	0	0	0	0	0
0	0	0	0	0	0	IR_Out[4:0]
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	3'b101	IR_Out[29:25]	IR_Out[18:14]	0
0	0	0	0	0	0	0
0	0	0	0	0	0	IR_Out[4:0]
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	IR_Out[29:25]	IR_Out[18:14]	0
0	0	0	0	0	0	0
0	0	0	0	0	0	IR_Out[4:0]
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	1'b1	0	0	IR_Out[18:14]	0
0	0	0	0	0	0	0
0	0	0	0	0	0	IR_Out[4:0]
0	0	0	0	0	0	0
0	0	0	3'b100	0	0	0
0	0	0	0	0	0	0
0	0	0	3'b001	0	0	0
0	0	0	0	0	0	0
0	0	0	3'b010	0	0	0
0	0	0	0	0	0	0

0	0	0	3'b011	0	0	0
0	0	0	0	0	0	0
0	0	0	0	5'b10001	5'b00000	0
0	0	0	0	0	0	0
0	0	0	0	5'b10010	0	0
0	0	0	0	0	0	0
0	2'b10	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	2'b00	0	0	0	0	0
0	2'b00	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	3'b011	0	0	0
0	0	0	0	0	0	0
0	0	0	3'b001	0	0	0
0	0	0	0	0	0	0
0	0	0	3'b010	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0

ALU_op	RAM_OpCode	Cond	Overflow	Underflow	PS	S	ET
0	0	0	0	0	0	0	0
6'b000000	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	6'b001000	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
6'b000000	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
6'b000000	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0

6'b000000	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
6'b000000	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
6'b000000	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
6'b000000	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
6'b000100	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
IR_Out[24:19]	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
6'b000000	IR_Out[24:19]	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0

0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
6'b000000	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
6'b000000	IR_Out[24:19]	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
6'b000000	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
6'b000000	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
6'b000000	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
6'b000011	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
6'b000011	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
6'b000011	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
6'b000000	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	PSR_out[7]	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0

6'b000100	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
6'b000000	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0
0	0	0	0	1	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	PSR_Out[6]	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0