Mixed Analog/Digital ASIC Emulator

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I. Introduction

This report presents the design of a mixed analog/digital ASIC emulator circuit. The emulator is designed to facilitate conversion into an ASIC using standard library cells provided by ASIC manufacturers. Key components of the design include power supply supervisors and clock generator circuits.

II. Input Voltage Monitor

The final schematic is shown in Figure 1. It features circuits that scale input voltages to the range allowed by the ASIC, alongside five comparators, one for each scaled input. Each comparator outputs a high signal if the input is within the allowable range and a low signal otherwise. The outputs from all five comparators are combined using an AND gate, which generates a signal, Vok, that goes high only when all inputs are within the acceptable range.

A. Inputs

Due to the voltage limitations of the ASIC, input voltages higher than 5V had to be scaled down, while negative voltages were shifted into a positive range.

12V Input: This was scaled down to 3V using a voltage divider (see Figure 2). Figure 3 shows the original signal and the scaled signal along with its tolerances and output of the comparator.

Negative Inputs: Summing amplifiers were used to level-shift negative inputs into a positive range by adding 5V from the ASIC power supply. This is illustrated in Figure 4. Figure 5 shows the simulation of the level shifter circuit for one of the negative inputs.

For all inputs, 5% tolerance calculations were performed on the shifted values to ensure accuracy.

B. Window Comparators

Each input voltage is monitored by a window comparator.

The window comparator for the +3.3V input is shown in Figure 6. Upper and lower bounds were calculated, and voltage dividers were used to derive these thresholds from the 5V power supply.

Figure 7 shows a simulation where the input voltage (blue) was modeled as a triangular wave for testing purposes. The upper and lower bounds are represented in red and green, respectively. The comparator output is high when the input is within the bounds and low otherwise.

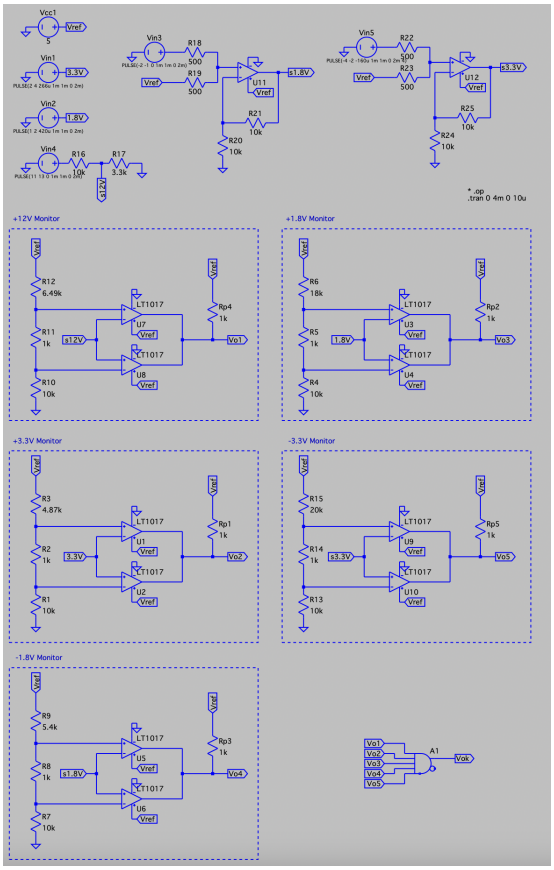

Fig. 1. Input Voltage Monitor Schematic

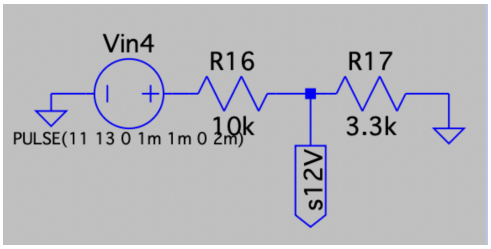

Fig. 2. Voltage divider for 12V input

C. Output

The outputs of all window comparators are fed into an AND gate, which generates the Vok signal. This signal goes

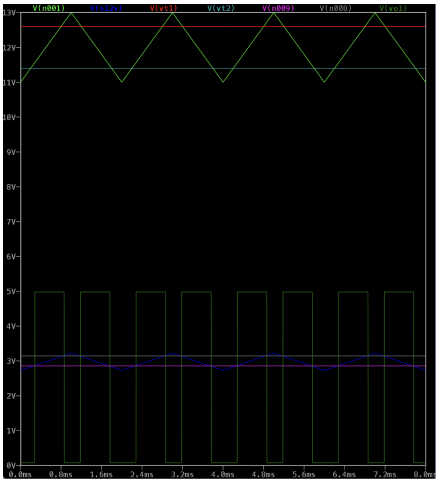

Fig. 3. Simulation of the scaling of the 12V input

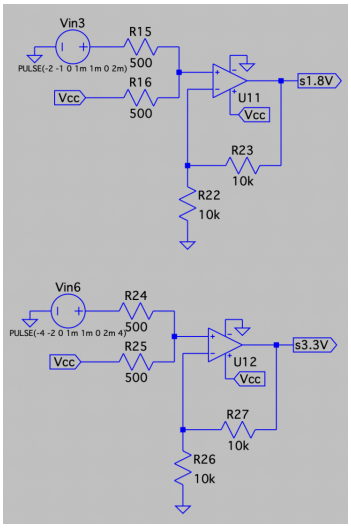

Fig. 4. Level shifters using summing amplifiers for negative inputs

high only when all inputs are within their respective allowable ranges.

Figure 8 illustrates a simulation where all inputs oscillate. Figure 9 shows a simulation where only the +3.3V input oscillates while other inputs remain constant and within their allowable ranges. In both scenarios, Vok goes high only when all input conditions are satisfied.

III. Synchronous Powergood Output

The overall schematic for the synchronous powergood output phase is shown in Figure 10. The schematic is broken into four sections: 10ms Detection, 100ms Stabilization Delay, Powergood Logic, and Convert to HIGH/LOW. The Vok signal generated by the Input Voltage Monitor is the same as the input Vok signal for this circuit. If Vok is high, then its value is 5V. In addition, Vcc and Vref are both set to 5V. All comparators in this circuit are powered by Vcc.

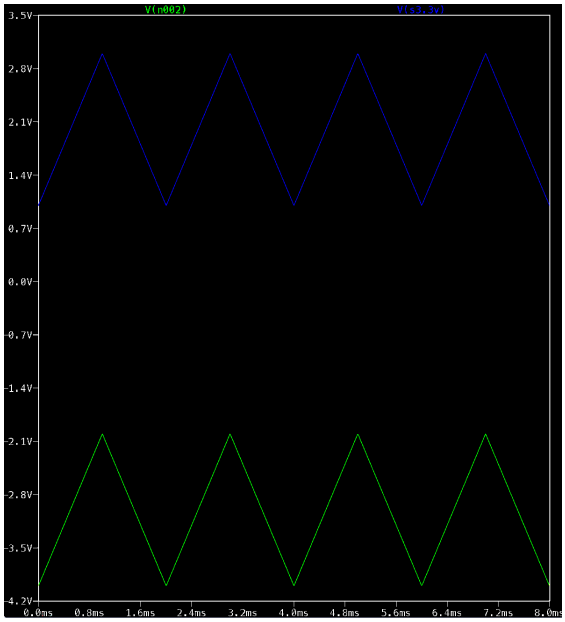

Fig. 5. Simulation of the scaling of the -3.3V input

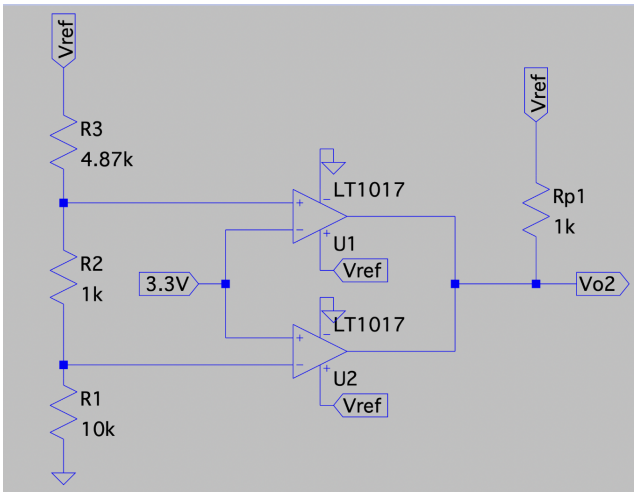

Fig. 6. Window Comparator for 3.3V input

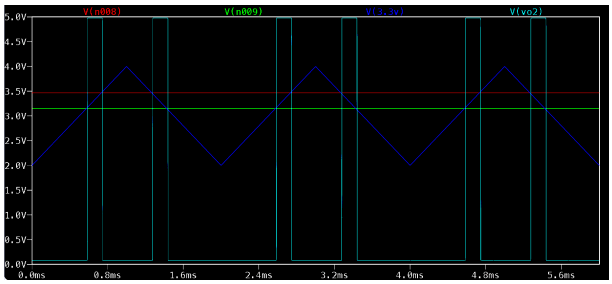

Fig. 7. Simulation results of window comparator for 3.3V input

A. Powergood Logic

For the comparator U1, its non-inverting input takes the signal Vref2, its inverting input takes in Vok3, and its output

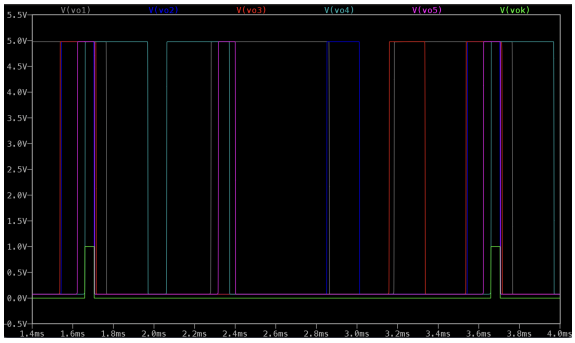

Fig. 8. Simulation where all inputs oscillate

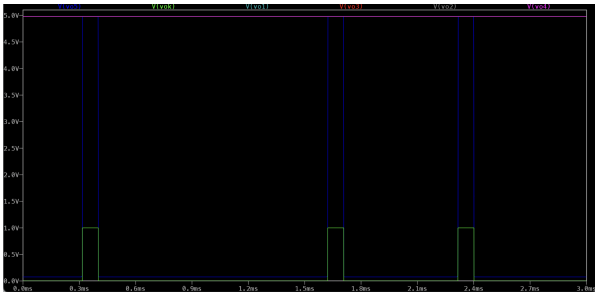

Fig. 9. Simulation with 3.3V oscillating

is the node U1_output. U1_output gets passed into the base of the NPN Q2. A2 is an inverter which flips the value of U1_output. This inverted U1_output gets passed into the base of the NPN Q1.

When U1_output is high, the NPN Q2 gets switched on, which means PWRGOOD2 has a direct path to ground and becomes low. When U1_output is low, the NPN Q1 gets switched on, which means PWRGOOD2 has a direct path to VCC and becomes high.

B. 100ms Stabilization Delay

For this phase, once all the input voltages reach their operating levels (i.e. Vok is high), a 100ms delay is initiated. At the end of the 100ms delay interval, the PWRGOOD output is set to high.

The voltage divider formed by R5 and R6 makes Vref2 around 4.8V, which is standard for modern data processing systems. The current source I1 allows the capacitor C1 to be charged. The stabilization delay t_{pg} depends on the time C1 gets charged up by the current source I1. The capacitor charging time can be determined by Equation 1:

$$t_{pg} = \frac{\text{C1} * \text{Vref2}}{\text{I1}} \tag{1}$$

To get a t_{pg} of 100ms, given that C1 is set to 1μF and Vref2 is 4.8V, the corresponding value of I1 is 48μA.

Vok3 depends on how much C1 has been charged. At 100ms, Vok3 equals Vref2 at 4.8V. Before 100ms has passed, Vref2 is higher than Vok3. The output of the comparator U1, U1_output, is high, so PWRGOOD2 is low. After 100ms has passed, Vok3 is higher than Vref2. U1_output is low, so PWRGOOD2 is high.

In Figure 11, Vok is set to high starting from 0ms. Vok3 increases linearly as C1 is being charged. At 100ms, Vok3 intersects with Vref2. The PWRGOOD voltage then becomes high after 100ms. This demonstrates that PWRGOOD is not set to high until after at least 100ms.

In Figure 12, Vok is set to high starting from 50ms. Like before, Vok3 increases linearly as C1 is being charged. At around 140ms, Vok3 intersects with Vref2. The PWRGOOD voltage then becomes high. This also demonstrates that PWRGOOD is not high until after the stabilization delay.

When the diode D1 is forward-biased (i.e. Vok2 is less than Vok3), the capacitor C1 gets discharged rapidly. Vok3 drops and becomes lower than Vref2. U1_output becomes high, so PWRGOOD2 becomes low.

C. 10ms Detection

For this phase, if any of the inputs drops below its operating range more than 10ms (i.e. Vok is low for more than 10ms), PWRGOOD should be driven low to indicate a fault condition.

When Vok is in the high state (5V), the capacitor C2 is charged. When Vok suddenly becomes low, the capacitor C2 is quickly discharged. This part of the circuit detects if Vok has become low for more than 10ms.

To calculate the voltage of C2 after it has been discharged for 10ms, Equation 2 can be used:

$$\text{Vfault\_ref} = \text{Vok} \cdot \exp\left(-\frac{t_{fault}}{\text{R9} \cdot \text{C2}}\right) \tag{2}$$

Given that Vok = 5V, R9 = 10kΩ, and C2 = 1μF. For t_{fault} = 10ms, Vfault_ref needs to be around 1.84V. This value for Vfault_ref is obtained with the voltage divider formed by R7 and R8.

The comparator U4 has a non-inverting input of Vfilter, an inverting input of Vfault_ref, and an output of Vok2. If Vok is set to 0V for less than 10ms, then Vfilter will be higher than Vfault_ref, so Vok2 is high. The diode D1 is reversed-biased, so C1 doesn't get discharged. The PWRGOOD output stays high.

If Vok is set to 0V for more than 10ms, then Vfault_ref is higher than Vfilter, so Vok2 is low. The diode D1 is forward-biased, so C1 gets discharged rapidly. The PWRGOOD output becomes low.

In Figures 13 and 14, at 120ms, Vok is set to low for 10ms. Vok then returns to high after 10ms passes. This is an edge case because Vok is low for exactly 10ms. It is shown from the simulations that the PWRGOOD output still remains high in this edge case.

In Figure 13, Vfilter shows C2 being discharged until it becomes equal to Vfault_ref at 130ms. At this point, Vok becomes high again, so Vfilter is being charged up again. Since Vfilter does not drop below Vfault_ref, C1 does not get discharged: Vok3 in Figure 14 still remains high from 120ms to 130ms. Therefore, the PWRGOOD output also remains high.

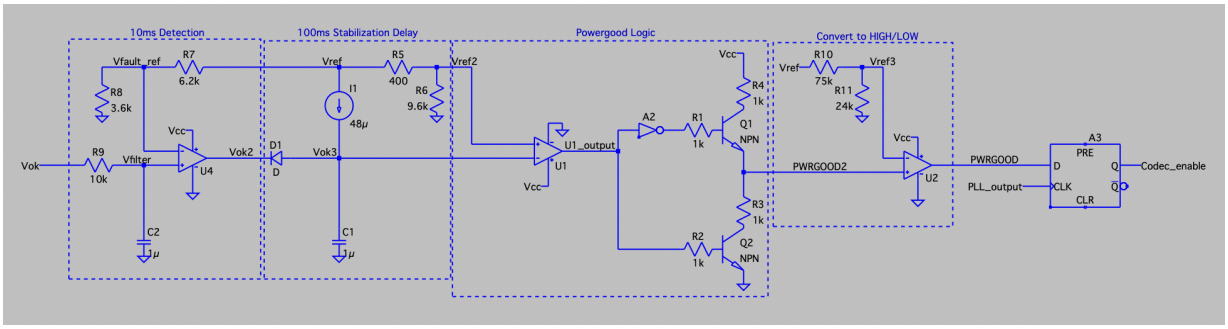

Fig. 10. Synchronous Powergood Output Schematic

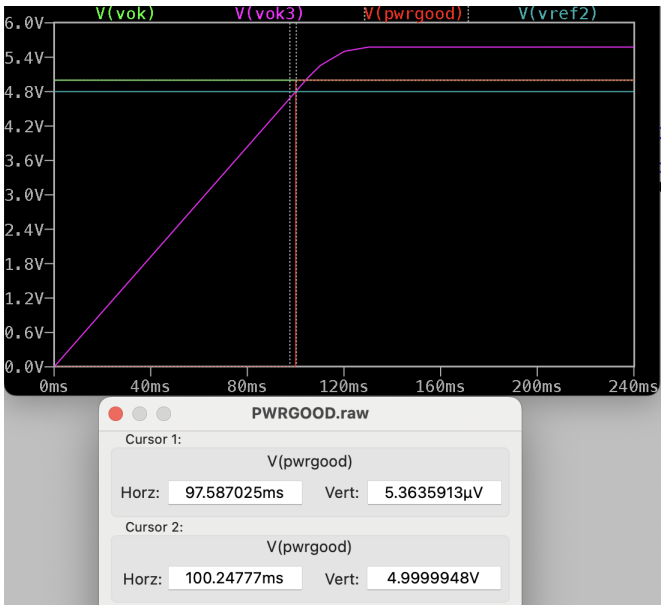

Fig. 11. 100ms delay in Powergood output

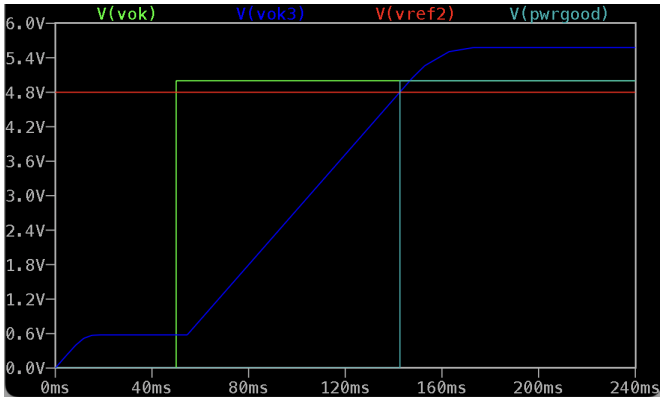

Fig. 12. More than 100ms delay in Powergood output

In Figures 15 and 16, at 120ms, Vok is set to low for 5ms. Vok then returns to high after 5ms passes. This is the case where Vok is low for less than 10ms. The PWRGOOD output should still remain high.

In Figure 15, Vfilter shows C2 being discharged. But at

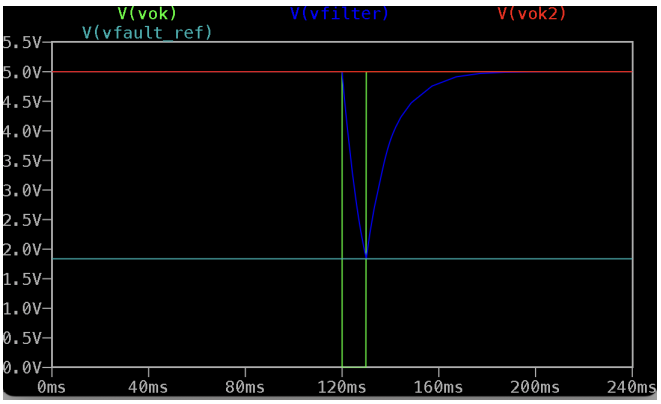

Fig. 13. Vok becomes low for 10ms

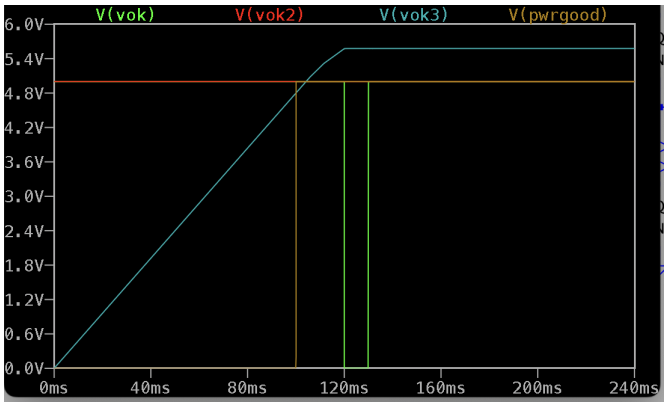

Fig. 14. Vok becomes low for 10ms, with other intermediate signals.

125ms, when Vok becomes high again, Vfilter is still above Vfault_ref. Since Vfilter does not drop below Vfault_ref, C1 does not get discharged: Vok3 in Figure 16 still remains high from 120ms to 125ms. Therefore, the PWRGOOD output also remains high.

In Figures 17 and 18, at 120ms, Vok is set to low for 15ms. Vok then returns to high after 15ms passes. This is the case where Vok is low for more than 10ms. The PWRGOOD output should become low afterwards.

In Figure 17, Vfilter shows C2 being discharged. At 135ms, when Vok becomes high again, Vfilter drops below Vfault_ref.

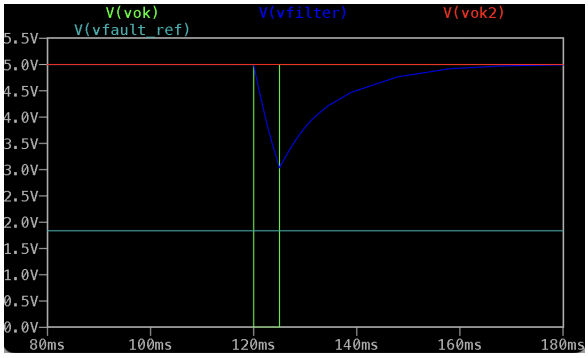

Fig. 15. Vok becomes low for 5ms

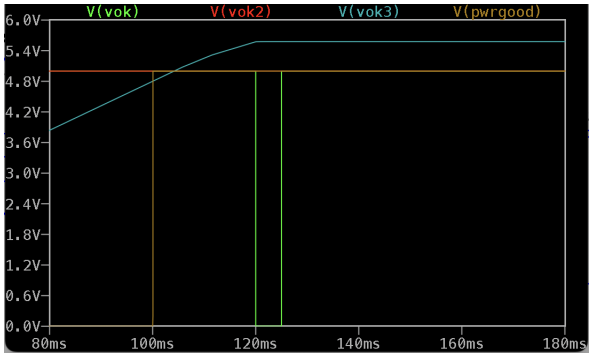

Fig. 16. Vok becomes low for 5ms, with other intermediate signals.

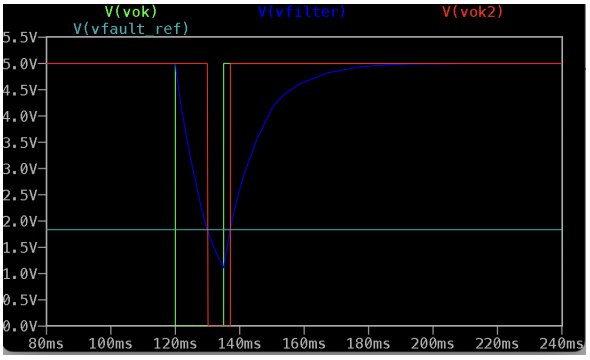

Fig. 17. Vok becomes low for 15ms

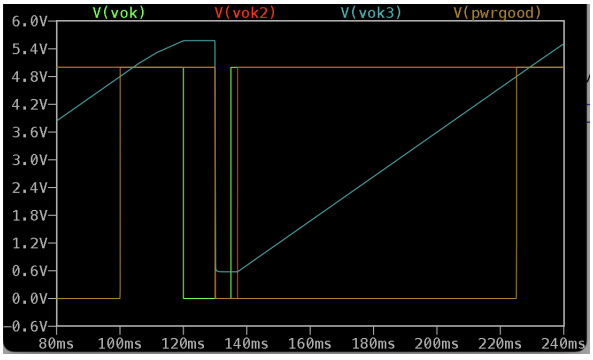

Fig. 18. Vok becomes low for 15ms, with other intermediate signals.

C1 gets discharged: Vok3 in Figure 18 drops at 130ms, when Vok2 also becomes low. Therefore, the PWRGOOD output becomes low at 130ms.

Vok is set back to high after 135ms. C1 is being charged up again, as shown in the linearly-increasing Vok3 curve. Due to the 100ms stabilization delay, the PWRGOOD output does not become high again until after 100ms, at around 230ms.

D. Convert to HIGH/LOW

In Figure 19, note that the output of PWRGOOD2 swings between a HIGH value of 2.5V and a LOW value of 17.93mV. Depending on the D Flip Flop used, these values may not be treated as a digital HIGH or LOW.

To resolve this, the comparator U2 is added, with a non-inverting input of PWRGOOD2, an inverting input of Vref3, and an output of PWRGOOD. Using a voltage divider formed by R10 and R11, Vref3 is set to around 1.21V. This is approximately halfway between 2.5V and 17.93mV. (Standard resistor values were used for R10 and R11. The large resistance values can also reduce power consumption.)

After this stage of the circuit, the PWRGOOD HIGH is 5V and the PWRGOOD LOW is 0V. This matches the HIGH and LOW voltages of Vok and ensures sound digital logic.

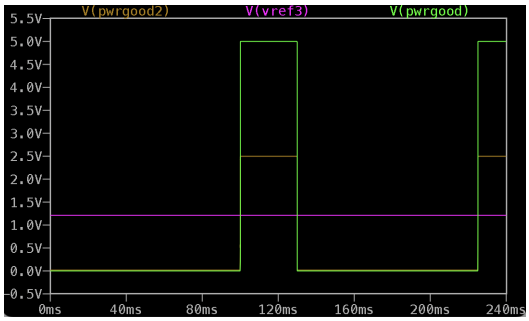

Fig. 19. PWRGOOD2 output

Finally, the PWRGOOD output is passed into the D input of a D flip flop. The CLK is the PLL's output described in Section IV below. In Figure 20, the Q output is codec_enable, which is passed into the audio codec's enable line.

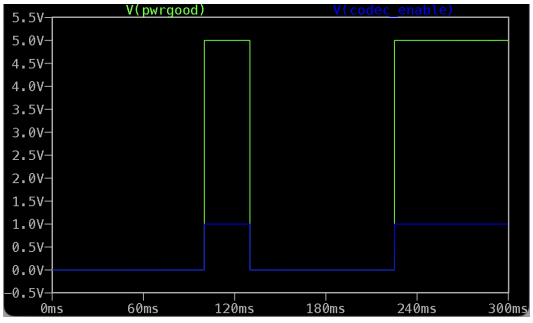

Fig. 20. D Flip Flop output

IV. Phase-Locked Loop

The PLL consists of a phase detector that compares a reference clock with a feedback clock and outputs two signals indicating the phase difference, a charge pump that adjusts the control voltage based on the output of the phase detector, a loop filter that stabilizes the PLL, a voltage-controlled oscillator (VCO) that generates an output clock whose frequency depends on the control voltage, and a divide-by-4 unit that turns the output clock into the feedback clock.

A. Phase Detector

Figure 21 shows the schematic of the PLL phase detector. The phase detector is built from two D flip-flops from the 74HC74 IC and a NAND gate from the 74HC00. When the reference clock is ahead of the feedback clock, the duty cycle of the "Up" signal indicates how far ahead it is. Likewise, when the reference clock is behind the feedback clock, the "Down" signal does the same.

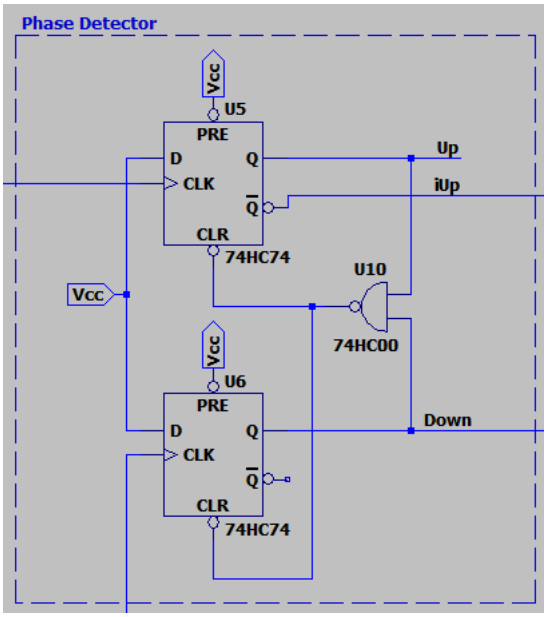

Fig. 21. Phase Detector Schematic

B. Divide-by-4

Figure 22 shows the schematic of the divide-by-4 circuit. The module is built from two D flip-flops, each in a divide-by-2 configuration, resulting in an overall division of the output frequency by 4. This way, the PLL will synchronize the feedback clock with the reference clock, meaning the output frequency will be 4 times higher than the reference frequency.

C. Voltage-Controlled Oscillator

Figure 23 shows the schematic of the VCO configuration. The VCO setup centers around the LTC6990 VCO IC, which provides all of the core functionality. Resistor values were selected such that the gain of the VCO is $K_{VCO} = -12.5\,\text{kHz}$, and the VCO outputs a clock of frequency $500\,\text{kHz}$ at a control voltage of $2.5\,\text{V}$, for reasons that are made apparent in the charge pump design.

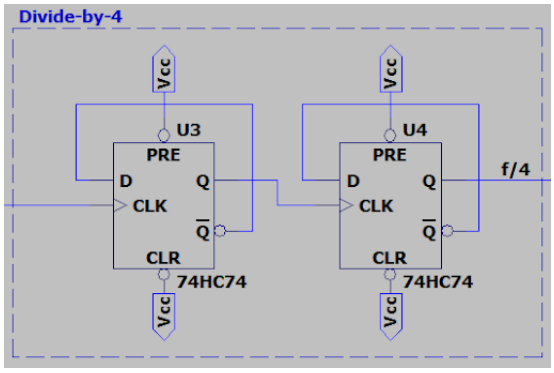

Fig. 22. Divide-by-4 Schematic

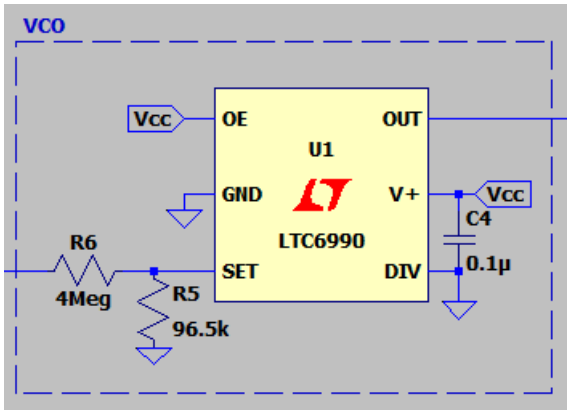

Fig. 23. VCO Configuration Schematic

D. Charge Pump and Loop Filter

Figure 24 shows the schematic of the charge pump and loop filter for the PLL. Since the VCO gain is negative, the "Down" signal from the phase detector will increase the control voltage in order to decrease the output frequency, and vice versa for the inverted "iUp" signal. The charge pump uses a simplified topology with Schottky diodes, instead of MOSFETs paired with current sources. As the charge pump does not use constant current sources, it runs the risk of charging and discharging the capacitors asymmetrically, causing instability in the PLL. To mitigate this flaw, the VCO is configured such that the nominal control voltage of the PLL is $2.5\,\text{V}$, so charging and discharging happen at the same rate when the PLL is locked.

Following the charge pump, a 2^{nd}-order loop filter with a bandwidth of $5\,\text{kHz}$ stabilizes the PLL, and a subsequent buffer opamp prevents charge from leaking through the VCO resistors.

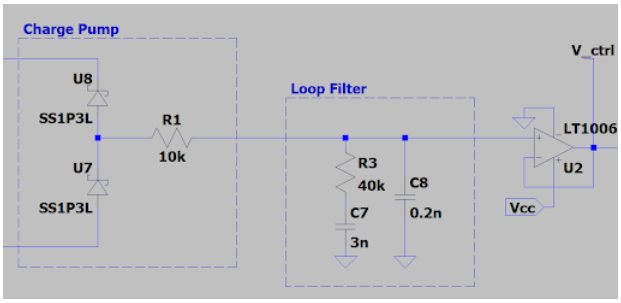

Fig. 24. Charge Pump and Loop Filter Schematic

E. PLL Performance

Figure 25 shows a graph of the PLL control voltage during the start up sequence. For the first 0.95 ms, the VCO is starting up, so there is no feedback clock to lock to. Afterward, the VCO begins oscillating, and the PLL takes 0.66 ms to lock. After a total of 1.61 ms, the PLL is locked and stable.

The minor oscillations after locking are 62 mV peak-to-peak, which corresponds to 0.155% jitter and a maximum difference between periods of 6.2 ps.

V. Signal Integrity and Power Integrity

A. Signal Integrity

Signal integrity tests were performed with a 6", 50-ohm transmission line and a 500kHz clock signal. Transmitter and receiver models were both taken from 74HCxx series ICs, which use standard CMOS logic. The corresponding HyperLynx schematic can be seen in Figure 26. The rising edge of the transmitter and receiver signals can be seen in Figure 27, which indicates that the receiver voltage only slightly lags behind and shoots ahead of the transmitter voltage - no termination required.

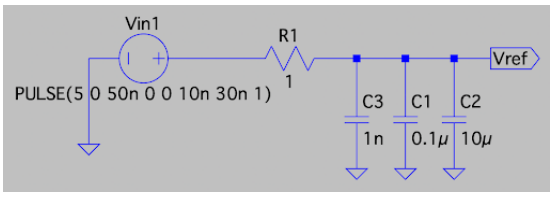

Fig. 26. HyperLynx SI Schematic

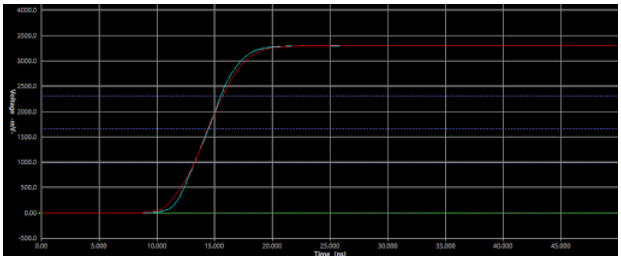

Fig. 27. Rising Edge of Transmitter and Receiver Voltages

B. Power Integrity

By adding a 1 Ω resistor in parallel with the ideal supply voltage, a nonideal power supply can be simulated. Figure 28 shows the schematic of this power supply, along with decoupling capacitors. Figures 29 and 30 show voltage spikes and dips, respectively, and the power rail staying constant for both conditions, thanks to the capacitors.

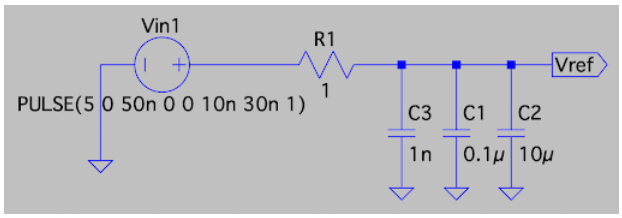

Fig. 28. PI Schematic

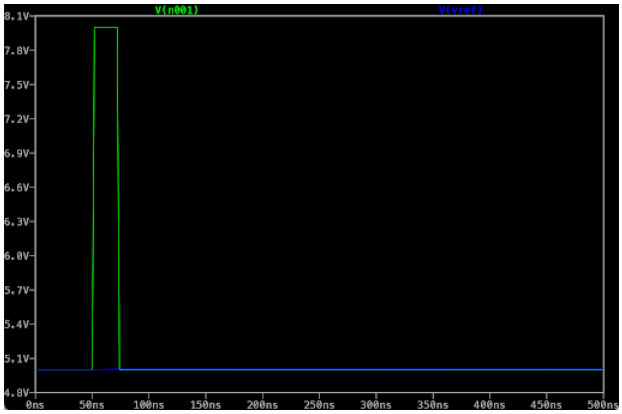

Fig. 29. 10 ns Voltage Spike

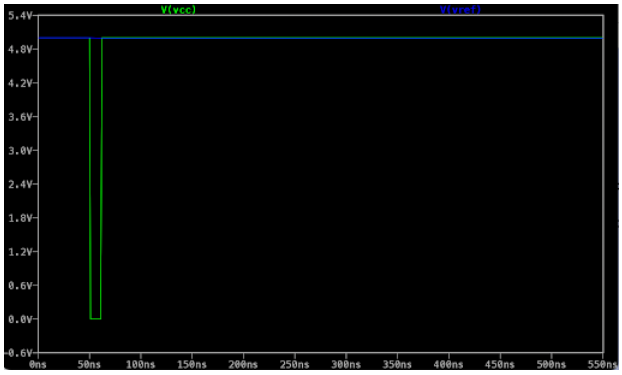

Fig. 30. 10 ns Voltage Dip

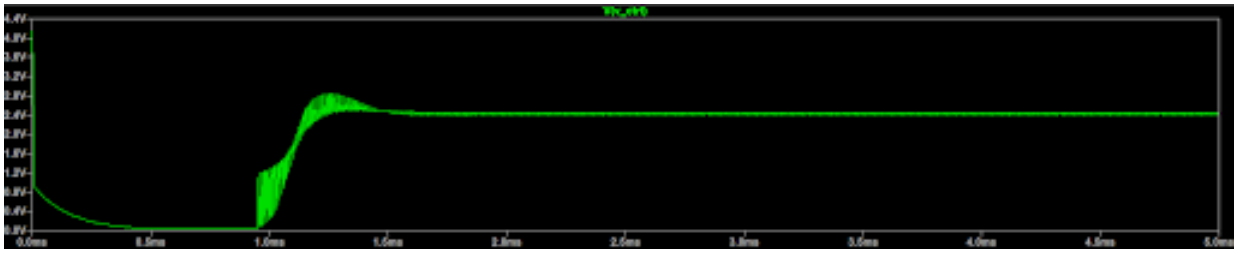

Fig. 25. PLL Control Voltage Graph