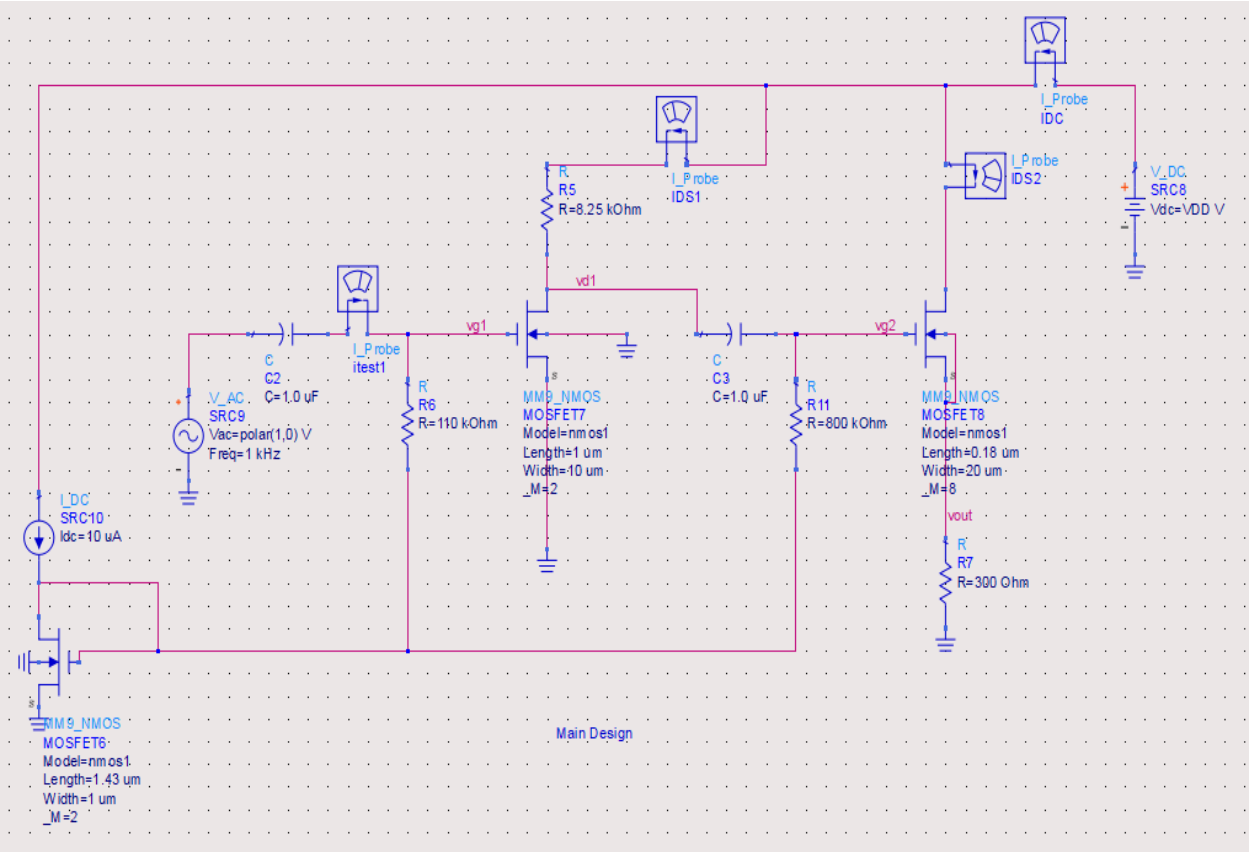
(1) Summary of design

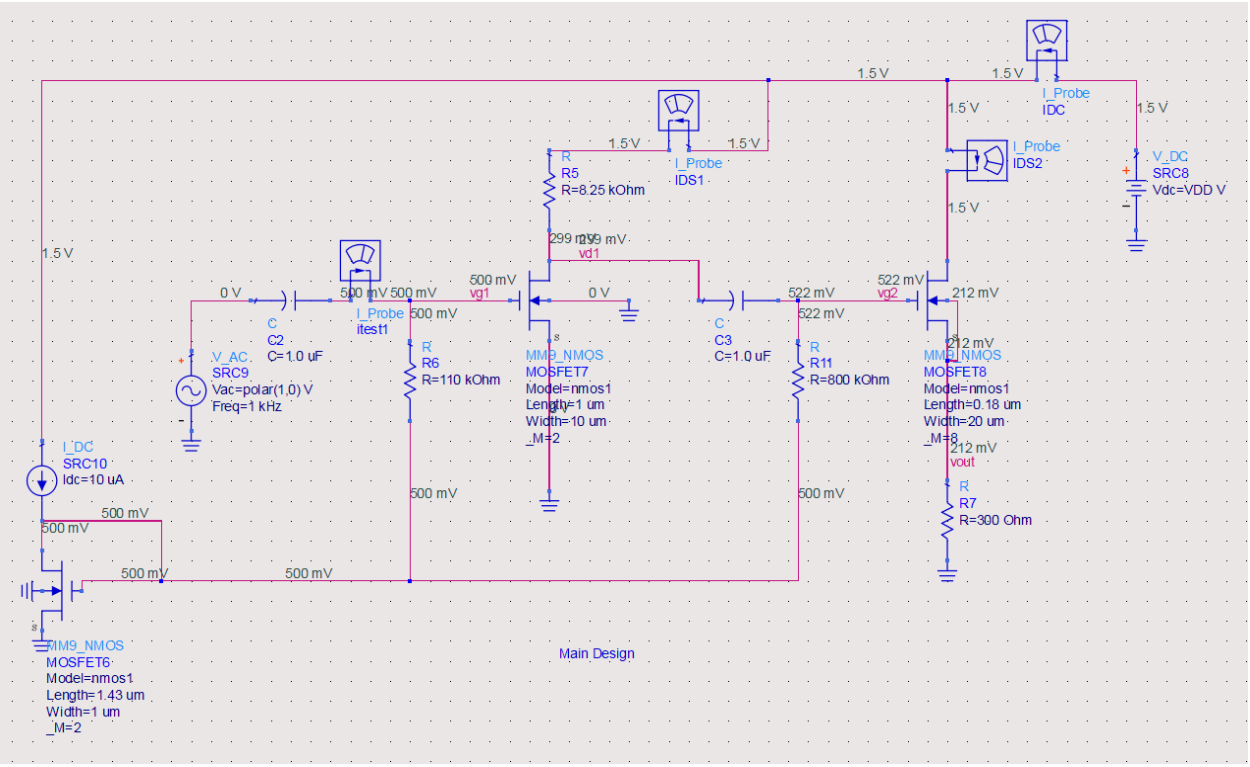
The design is a common source topology followed by a common drain topology. The common drain stage is connected to the output of the common source stage and separated by a capacitor. Common source provides a large voltage gain ($-g_m(R_D||r_O)$) but has a high output impedance, which is not desired. Common drain attenuates the voltage but provides both a high input impedance and a low output impedance, which is desired. Connecting the two topologies means that a high voltage gain, high input impedance, and low output impedance are attained.

(2) Target specifications vs actual simulated performance

Criteria	Target Specifications	Actual Value
V_{DD}	≤1.5 V	1.5V
Frequency	1 kHz	1 kHz
Total DC Current	≤2 mA	861.748 μA
Magnitude of Voltage Gain	≥20 dB (Magnitude ≥ 10)	20.01862 dB (Magnitude = 10.02146)
Input Impedance	≥100 kΩ	104.258 kΩ
Output Impedance	≤30 Ω	8.62527 Ω
Reference Current of Current Mirrors	10 μA	10 μA

(3) Complete Schematic (the one below is labeled with DC voltages)





(4) Theoretical analysis

Calculated Voltage Gain

$A_{v,CS} = -g_{m1}(R_D || r_{o1}) = -0.00152 * (8250 || 94.893k) \approx -0.00152 * 8250 = -12.54.$

$A_{v,CD} = \frac{R_s || r_{o2}}{\frac{1}{g_{m2}} + (R_s || r_{o2})} = \frac{300||3512.80}{\frac{1}{0.03340} + (300||3512.80)} = \frac{276.3953}{\frac{1}{0.03340} + 276.3953} = 0.902.$

Overall gain: $A_{v,tot} = A_{v,CS} \bullet A_{v,CD} = -12.54 \bullet 0.902 = -11.314.$

(Note that the measured g_{m1} of the CS transistor is 0.00152 S. The measured g_{m2} of the CD transistor is 0.03340 S. The measured r_{O1} of the CS transistor is about 94.893 kΩ. The measured r_{O2} of the CD transistor is about 3512.80 Ω. See below for how these values are obtained.)

Calculated Impedance

Input impedance: $R_{in} = 100k || \infty = 100k\Omega$ (ideally, the gate resistance in infinity because no current should flow into the gate, so R_{in} is the DC biasing resistance in parallel with infinity).

Output impedance: $R_{out} = \frac{1}{g_{m2}} || r_{O2} || R_S = \frac{1}{0.03340} || 3512.80 || 300 = 27.014\Omega.$

Operation in the Saturation Region

Both transistors for the CS and CD stages are biased in the saturation region ($V_{DS} > V_{GS} - V_{TH}$).

For the CS stage, set $V_{GS} = 0.5V$ and assume $V_{TH} = 0.3V$ yields $V_{DS} > 0.2V$ for the transistor to operate in the saturation region. The simulation results give $I_{DS1} = 145.529\mu A$. Plug this value into the following equation to calculate $V_D = V_{DD} - I_{DS1} \bullet R_D = 1.5 - 145.529\mu \bullet 8.25k = 0.299V$. $V_{DS} = V_D - V_S = 0.299 - 0 = 0.299V > 0.2V$. The simulation results below for $V_{DS} = 299.385mV > 0.2V$ also support this calculated value.

For the CD stage, the simulation results gives $I_{DS2} = 706.219\ \mu A$. Plug this value into the following equation to calculate $V_S = I_{DS2} \bullet R_S = 706.219\ \mu \bullet 300 = 0.212V$. (The simulation's result of DC.vout = $V_S = 211.857$mV corresponds to this value.) Note that $V_D = V_{DD} = 1.5V$, and the simulation indicates that $V_G = 0.522V$, so $V_{GS} - V_{TH} = 0.522 - 0.211857 - 0.3 = 0.0101V$. Hence, $V_{DS} = 1.5 - 0.211857 = 1.288143V > 0.0101V = V_{GS} - V_{TH}$.

Rationale behind chosen W and L values for the transistors

- The transistor by the reference current has $L = 1.43\mu m$, $W = 1\mu m$, and _M = 2. These values are chosen so that the gate voltage V_G of the CS-stage transistor is at around 0.5V. This ensures that it is biased in the saturation region.
- For the CS-stage transistor, $L = 1\mu m$, $W = 10\mu m$, and _M = 2. These values maximize the gain of the CS stage.
- For the CD-stage transistor, $L = 0.18\mu m$, $W = 20\mu m$, and _M = 8. To decrease the output impedance R_{out} to the specified value, $1/g_m$ needs to be smaller, which means g_m needs to be larger. To increase $g_m = \sqrt{2\mu_n C_{OX} \frac{W}{L} I_{DS}}$, the ratio of $\frac{W}{L}$ can be increased. Therefore, the ratio of W to L is larger for the CD-stage transistor.

(5) **Simulation Result**

CS stage (gm, Av, IDS, VDS)

freq	AC.IDS1.i	AC.vd1	freq	DC.IDS1.i	DC.vd1
1.00000 kHz	0.00152 / 0.08700	12.57924 / -179.91300	0.000000 Hz	145.529 uA	299.385 mV

CD stage (gm, Av, IDS, VS)

freq	AC.IDS2.i	AC.vout	freq	DC.IDS2.i	DC.vout
1.00000 kHz	0.03340 / -179.89998	10.02146 / -179.89997	0.000000 Hz	706.219 uA	211.857 mV

Total voltage gain

Rin

freq	1/AC.itest1.i
1.00000 kHz	1.04258E5 / -0.10351

Rout

freq	1/AC.itest2.i
1.00000 kHz	8.62527 / 0.00047

Total IDC

freq	DC.IDC.i
0.000000 Hz	861.748 uA

r_o1

freq	1/AC.IDS4.i
1.00000 kHz	94893.40722 / -0.06424

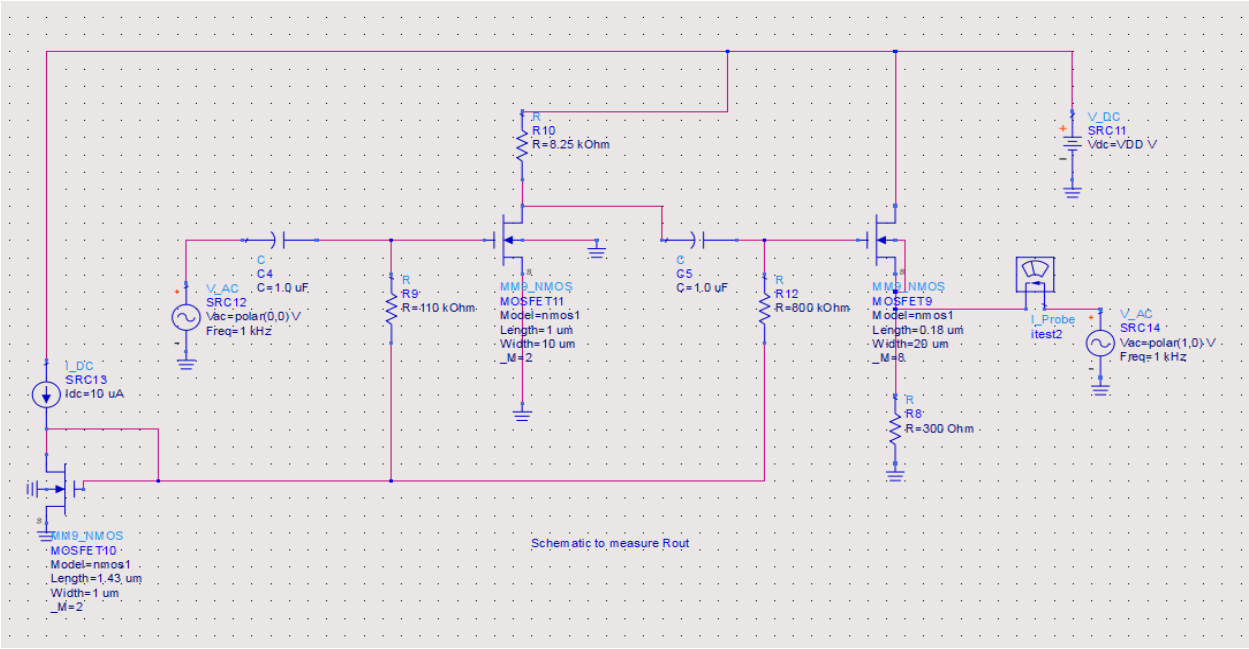
r_o2

freq	1/AC.IDS5.i
1.00000 kHz	3512.79568 / -0.00016

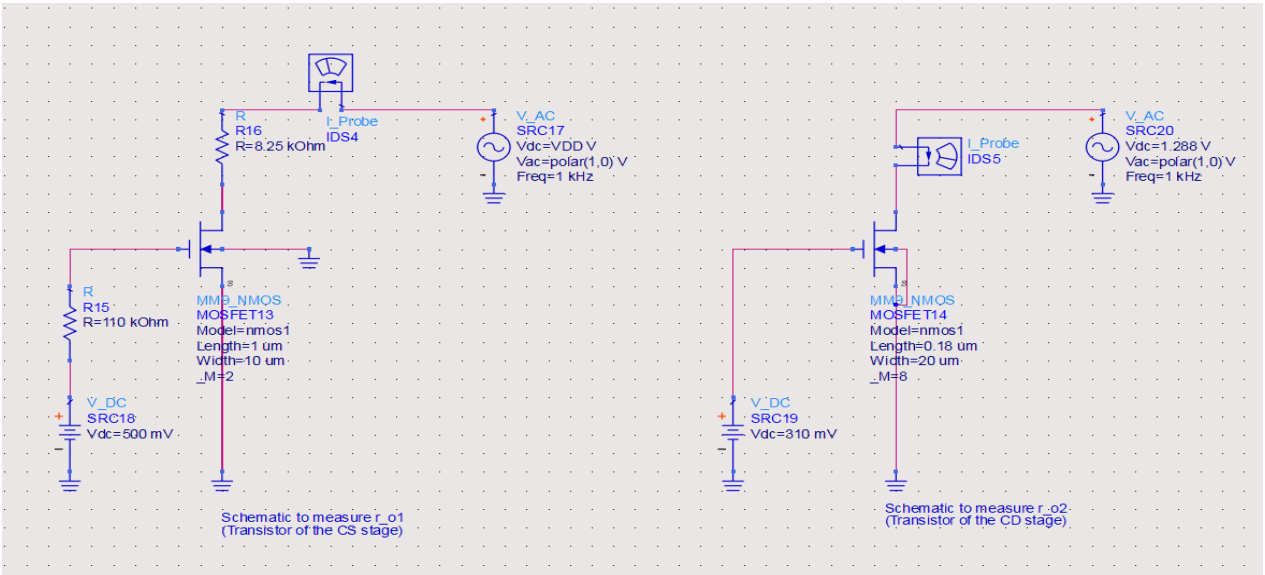
For the CS stage, AC.IDS1.i is the g_{m1}, AC.vd1 is the voltage gain of the CS stage, DC.IDS1.i is the I_{DS1}, and DC.vd1 is the V_{DS} of the first NMOS. For the CD stage, AC.IDS2.i is the g_{m2}, AC.vout is the overall voltage gain, DC.IDS2.i is the I_{DS2}, and DC.vout is the V_S of the second NMOS.

R_{in} is calculated by 1/AC.itest1.i when v_{ac} at the input is set to 1V. R_{out} is calculated by 1/AC.itest2.i when the v_{ac} at the input is set to 0 and v_{ac} at the output is set to 1V. Calculating R_{out} requires attaching another AC source to the output as the test voltage, so a separate schematic is constructed on the right of the main schematic to obtain this measurement.

Below is the schematic used to calculate R_{out}:



Below is the schematics used to calculate r_{o1} (of the CS transistor) and r_{o2} (of the CD transistor):



For r_{O2}, V_DC is set to 310mV because that is the V_{GS} value obtained from the labeled schematic in part (3). In this case, $V_{GS} = 522mV - 212mV = 310mV$. For V_AC, the Vdc is set to 1.288V because that is the V_{DS} value obtained from the labeled schematic in part (3). In this case, $V_{DS} = 1.5V - 212mV = 1.288V$.

The total IDC, which is 861.748 μA, is obtained by a current probe next to VDD.

(6) Comparison between calculated and simulated performances

The calculated voltage gain of the CS stage ($A_{v,CS}$) is around -12.54, while the actual gain is -12.57924, which is similar to the calculated value (the -179.91300 under AC.vd1 is the phase, which accounts for the negative sign of the CS gain). For the overall gain ($A_{v,tot}$), the calculated value is around -11. 314, while the actual total voltage gain is -10.02146. There is a slight discrepancy between these two values because of the transistors' second order effects/parameters, which are not accounted for in the calculations above. These second order effects may have slightly decreased the voltage gain, so the actual performance is not as good as the calculated gain.

The input impedance is calculated as $100k\Omega$, while the actual value is $104.258k\Omega$, which is slightly higher. This is due to how there is a small current (a few pA) flowing into the transistor's gate. Therefore, the gate resistance is a very large value but not infinity, but the calculation above assumes that the gate resistance is infinity. This discrepancy means that the actual input impedance is slightly higher.

The output impedance is calculated as 27.014Ω, which is higher than the simulated value of 8.62527Ω. This value is slightly off because there are second-order effects from the transistor that the calculations did not account for.