LAB REPORT

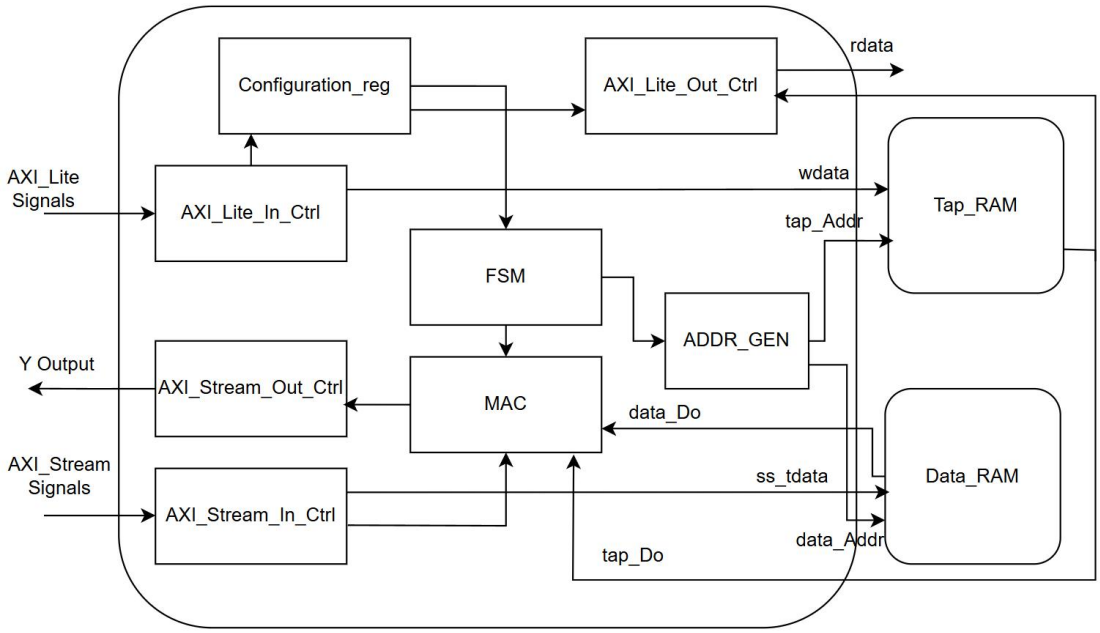
(Lab3 Verilog FIR Design)

Author: Wu Chengkai
EESM6000 SoC Lab
HKUST – Dept. of ECE

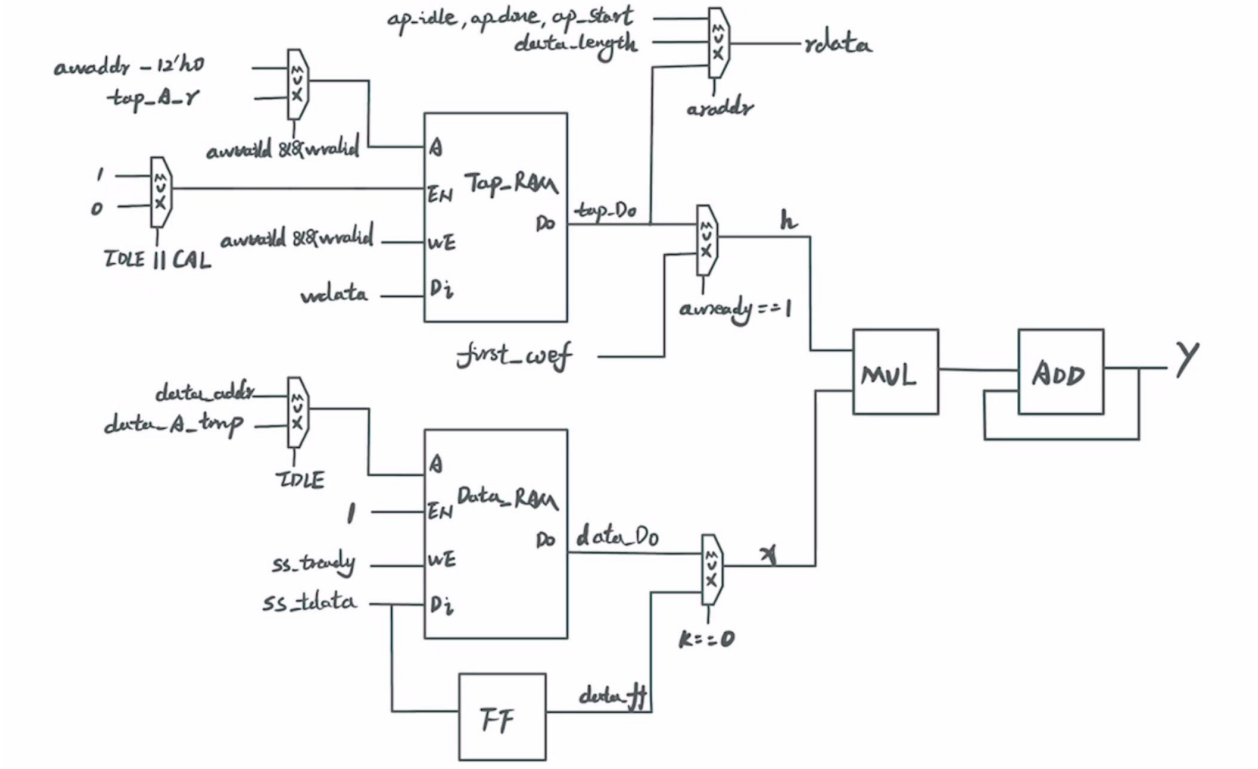
Date: March 2025

TABLE OF CONTENTS

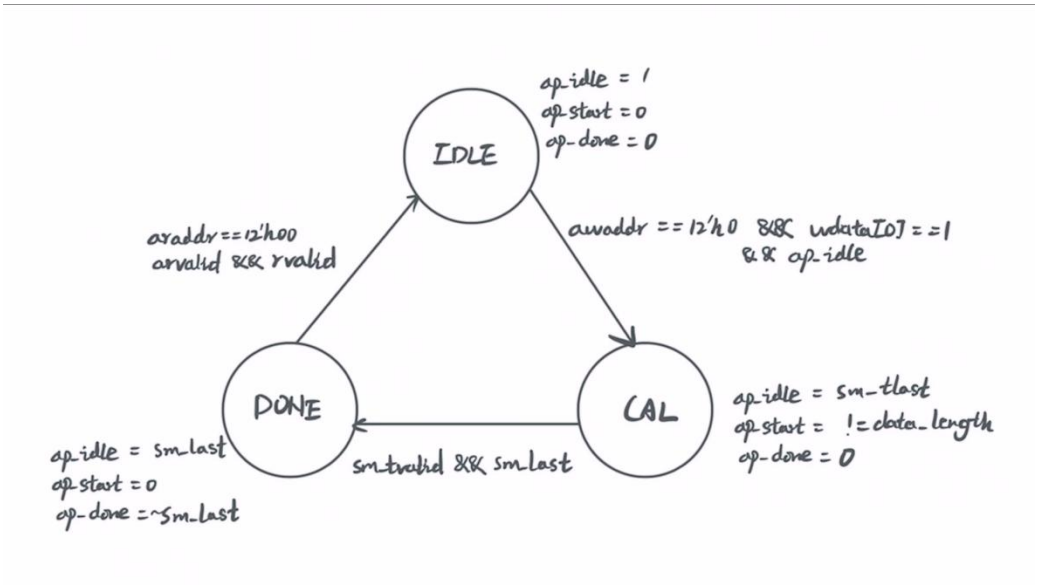
1.0 BLOCK DIAGRAM



1.1 Datapath



1.2 FSM



2.0 OPERATION

In this lab, we aim to construct a Finite Impulse Response (FIR) operation module with 11 coefficients to perform filtering. The module's data must adhere to the AXI-Stream protocol.

AXI-Lite Interface: Manages configuration signals from the host/testbench . It handles writes for filter taps and reads for status signals (ap_done, ap_idle, ap_start).
AXI-Stream Interface: Transfers real-time input data x[t] to the filter, computes the FIR, and outputs results back to the host.

For data storage, dual BRAM are required.
Tap coefficients are stored in Tap_RAM, while raw input data is stored in Data_RAM.

Initialization Phase:
The configuration register is set to 32'h04, indicating enter the IDLE state.
When the host (testbench) detects the IDLE state, it begins sending tap coefficients and data length information via the AXI-Lite protocol.
For different awaddr values:
awaddr = 0x00, wdata represents ap_start.
awaddr = 0x10, wdata represents the data_length.
awaddr ≥ 0x20, wdata represents the tap coefficient.

Transition to CAL State:
After storing all tap coefficients into Tap_RAM at addresses generated by the addr_gen block , the configuration register is set to 32'h01 (ap_start == 1), initiating the CAL state.

The AXI-Stream interface then waits for the ap_start signal. Upon entering CAL, input data is loaded into data_RAM via ss_tdata, with addresses generated by addr_gen block
Address Generation Logic:

The addr_gen block uses an internal counter to manage BRAM addresses:
Tap_RAM: Coefficients are read sequentially at addresses 0, 4, 8, ..., 40, repeating every 11 cycles.
Data_RAM: Addresses follow a sliding window pattern to align with coefficients:
Example sequence after enter CAL state:
First input: 0, 40, 36, ..., 4
Second input: 4, 0, 40, ..., 8
Third input: 8, 4, 0, ..., 12
This pattern continues until the 11th iteration.

Computation and Completion:
The corresponding tap_do (tap coefficient data output) and data_do (input data output) are fed into the MAC unit (Multiply-Accumulate unit) to perform multiplication and accumulation operations. After 11 iterations, sm_tvalid is asserted to output the result Y.

An internal tlast_cnt tracks the data length. When tlast_cnt matches data_length, ss_tlast is asserted. After the final computation, sm_tlast and ap_done are raised, transitioning the system to the DONE state.

Timing Optimization:
To compensate for the 1-cycle latency of BRAM outputs, ss_tdata is delayed by one cycle using a flip-flop (FF). This ensures Data_Do is available at the start of the next computation cycle, reducing overall cycle count. Additionally, the first tap coefficient is preloaded upon entering the CAL state to avoid an extra wait cycle for tap_Do.

3.0 RESOURCE USAGE

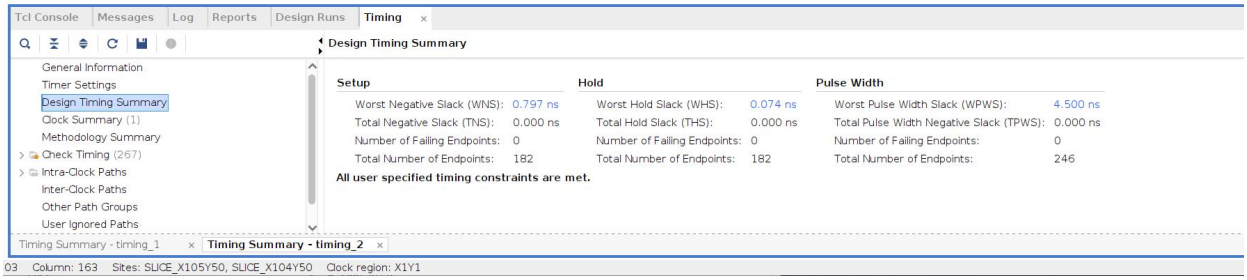
3.1 FF and LUT

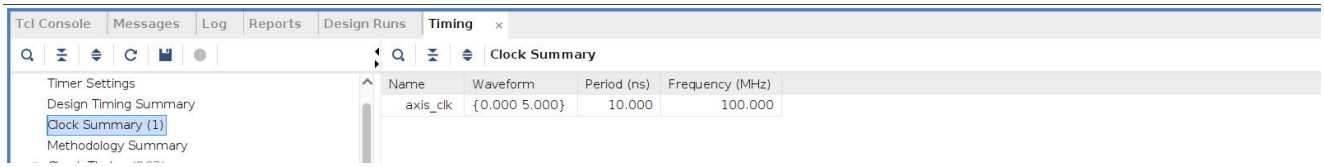
Site Type	Used	Fixed	Prohibited	Available	Util%
Slice LUTs*	92	0	0	53200	0.17
LUT as Logic	28	0	0	53200	0.05
LUT as Memory	64	0	0	17400	0.37
LUT as Distributed RAM	64	0			
LUT as Shift Register	0	0			
Slice Registers	4	0	0	106400	<0.01
Register as Flip Flop	4	0	0	106400	<0.01
Register as Latch	0	0	0	106400	0.00
F7 Muxes	0	0	0	26600	0.00
F8 Muxes	0	0	0	13300	0.00

3.2 BRAM

Site Type	Used	Fixed	Prohibited	Available	Util%
Block RAM Tile	0	0	0	140	0.00
RAMB36/FIFO*	0	0	0	140	0.00
RAMB18	0	0	0	280	0.00

4.0 TIMING REPORT





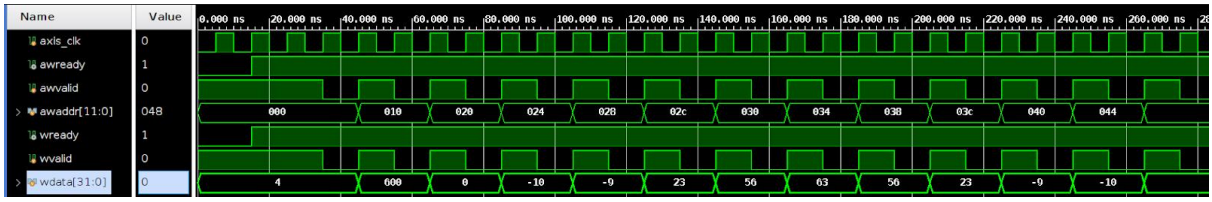

```
Max Delay Paths
--------------------------------------------------------------------------------------
Slack (MET) :             0.797ns  (required time - arrival time)
  Source:                 h_reg[16]/C
                            (rising edge-triggered cell FDCE clocked by axis_clk  {rise@0.000ns fall@5.000ns period=10.000ns})
  Destination:            m_reg[29]/D
                            (rising edge-triggered cell FDCE clocked by axis_clk  {rise@0.000ns fall@5.000ns period=10.000ns})
  Path Group:             axis_clk
  Path Type:              Setup (Max at Slow Process Corner)
  Requirement:            10.000ns  (axis_clk rise@10.000ns - axis_clk rise@0.000ns)
  Data Path Delay:        9.098ns  (logic 7.435ns (81.717%)  route 1.663ns (18.283%))
  Logic Levels:           7  (CARRY4=4 DSP48E1=2 LUT5=1)
  Clock Path Skew:        -0.145ns (DCD - SCD + CPR)
    Destination Clock Delay (DCD):    2.128ns = ( 12.128 - 10.000 )
    Source Clock Delay      (SCD):    2.456ns
    Clock Pessimism Removal (CPR):    0.184ns
  Clock Uncertainty:      0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter     (TSJ):    0.071ns
    Total Input Jitter      (TIJ):    0.000ns
    Discrete Jitter          (DJ):    0.000ns
    Phase Error              (PE):    0.000ns
```

```
    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
                         (clock axis_clk rise edge)
                                                      0.000     0.000 r
                                                      0.000     0.000 r  axis_clk (IN)
                         net (fo=0)                   0.000     0.000    axis_clk
                                                                     r  axis_clk_IBUF_inst/I
                         IBUF (Prop_ibuf_I_O)         0.972     0.972 r  axis_clk_IBUF_inst/O
                         net (fo=1, unplaced)         0.800     1.771    axis_clk_IBUF
                                                                     r  axis_clk_IBUF_BUFG_inst/I
                         BUFG (Prop_bufg_I_O)         0.101     1.872 r  axis_clk_IBUF_BUFG_inst/O
                         net (fo=245, unplaced)       0.584     2.456    axis_clk_IBUF_BUFG
                         FDCE                                           r  h_reg[16]/C
  -------------------------------------------------------------------    -------------------
                         FDCE (Prop_fdce_C_Q)         0.478     2.934 r  h_reg[16]/Q
                         net (fo=1, unplaced)         0.800     3.734    h[16]
                                                                     r  m_tmp/A[16]
                         DSP48E1 (Prop_dsp48e1_A[16]_PCOUT[47])
                                                      4.211     7.945 r  m_tmp/PCOUT[47]
                         net (fo=1, unplaced)         0.055     8.000    m_tmp_n_106
                                                                     r  m_tmp__0/PCIN[47]
                         DSP48E1 (Prop_dsp48e1_PCIN[47]_P[0])
                                                      1.518     9.518 r  m_tmp__0/P[0]
                         net (fo=1, unplaced)         0.800    10.318    m_tmp__0_n_105
                                                                     r  m[19]_i_7/I4
                         LUT5 (Prop_lut5_I4_O)        0.124    10.442 r  m[19]_i_7/O
                         net (fo=1, unplaced)         0.000    10.442    m[19]_i_7_n_0
                                                                     r  m_reg[19]_i_1/S[1]
```

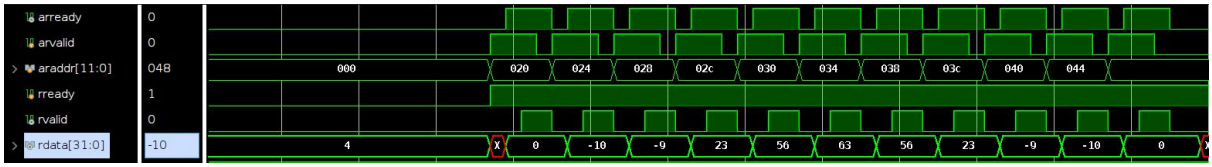
```
                        CARRY4 (Prop_carry4_S[1]_CO[3])
                                                   0.533    10.975 r  m_reg[19]_i_1/CO[3]
                        net (fo=1, unplaced)       0.009    10.984    m_reg[19]_i_1_n_0
                                                             r  m_reg[23]_i_1/CI
                        CARRY4 (Prop_carry4_CI_CO[3])
                                                   0.117    11.101 r  m_reg[23]_i_1/CO[3]
                        net (fo=1, unplaced)       0.000    11.101    m_reg[23]_i_1_n_0
                                                             r  m_reg[27]_i_1/CI
                        CARRY4 (Prop_carry4_CI_CO[3])
                                                   0.117    11.218 r  m_reg[27]_i_1/CO[3]
                        net (fo=1, unplaced)       0.000    11.218    m_reg[27]_i_1_n_0
                                                             r  m_reg[31]_i_1/CI
                        CARRY4 (Prop_carry4_CI_O[1])
                                                   0.337    11.555 r  m_reg[31]_i_1/O[1]
                        net (fo=1, unplaced)       0.000    11.555    m_reg[31]_i_1_n_6
                        FDCE                                         r  m_reg[29]/D
------------------------------------------------------------------------------------------------
                        (clock axis_clk rise edge)
                                                  10.000    10.000 r
                                                   0.000    10.000 r  axis_clk (IN)
                        net (fo=0)                 0.000    10.000    axis_clk
                                                             r  axis_clk_IBUF_inst/I
                        IBUF (Prop_ibuf_I_O)       0.838    10.838 r  axis_clk_IBUF_inst/O
                        net (fo=1, unplaced)       0.760    11.598    axis_clk_IBUF
                                                             r  axis_clk_IBUF_BUFG_inst/I
                        BUFG (Prop_bufg_I_O)       0.091    11.689 r  axis_clk_IBUF_BUFG_inst/O
                        net (fo=245, unplaced)     0.439    12.128    axis_clk_IBUF_BUFG
                        FDCE                                         r  m_reg[29]/C
                        clock pessimism            0.184    12.311
                        clock uncertainty         -0.035    12.276
                        FDCE (Setup_fdce_C_D)      0.076    12.352    m_reg[29]
------------------------------------------------------------------------------------------------
                        required time                       12.352
                        arrival time                       -11.555
------------------------------------------------------------------------------------------------
                        slack                               0.797
```

5.0 SIMULATION WAVEFORM

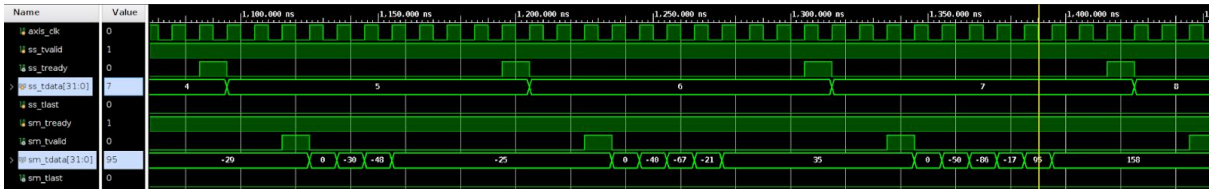
5.1 Coefficient program



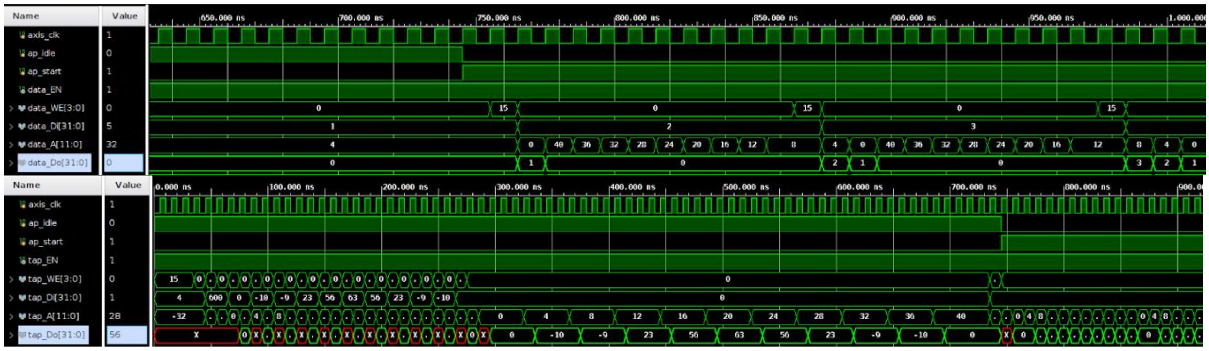
5.2 Read back



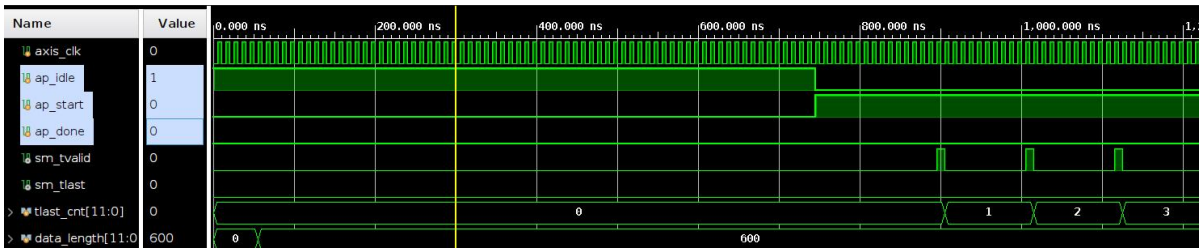
5.3 Data-in Stream-in && Data-out Stream-OUT

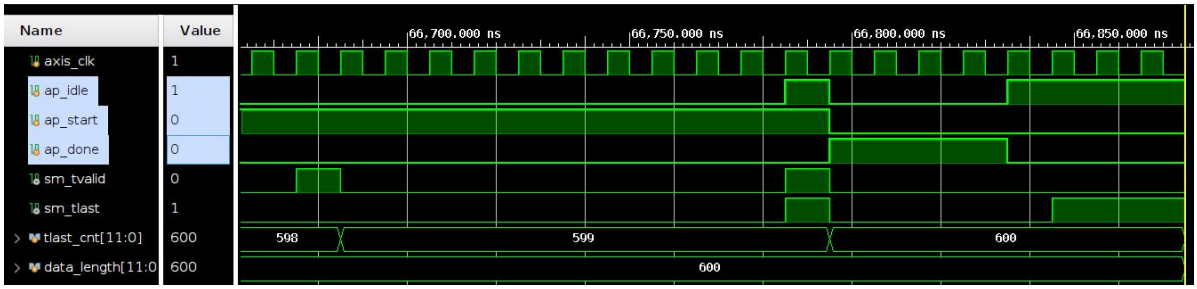


5.4 RAM access control



5.5 FSM





Github: https://github.com/edwu186/System-on-Chip-SoC-Laboratory