Registermap

Overview

Name	Address	Description
LEDG	0x5000	Green LED Register
LEDR	0x5002	Red LED Register
HEX0	0x5010	Seven Segment Digit 0 Register
HEX1	0x5012	Seven Segment Digit 1 Register
HEX2	0x5014	Seven Segment Digit 2 Register
HEX3	0x5016	Seven Segment Digit 3 Register
KEY	0x5020	Pushbuttons Register
SW	0x5022	Switch Register
ENDPI0_CONTROL	0x6000	Endpoint In 0 Control Register
ENDPI0_DATA	0x6002	Endpoint In 0 Data Register
ENDPI1_CONTROL	0x6004	Endpoint In 1 Control Register
ENDPI1_DATA	0x6006	Endpoint In 1 Data Register
ENDPO0_CONTROL	0x6040	Endpoint Out 0 Control Register
ENDPO0_DATA	0x6042	Endpoint Out 0 Data Register
USB_ADDRESS	0x6100	USB Address Register
USB_TOKEN	0x6102	USB Token Register
USB_STATUS	0x6104	USB Status Register

Detailed Description

LEDG

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	-	-	LEDG							
Mode	r0	r0	r0	r0	r0	r0	r0	r0	w							
Reset	-	-	-	-	-	-	-	-	0x00							

Green LED Register
Address: 0x5000

LEDR

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	LEDR									
Mode	r0	r0	r0	r0	r0	r0	w									
Reset	-	-	-	-	-	-	0x000									

Red LED Register
Address: 0x5002

The registers LEDG and LEDR control the eight green and the ten red LEDs of the evaluation board respectively.

A set bit means the LED is on, a reset bit means the LED is off.

HEX0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	-	-	-	HEX0						
Mode	r0	r0	r0	r0	r0	r0	r0	r0	r0	w						
Reset	-	-	-	-	-	-	-	-	-	0x00						

Seven Segment Digit 0 Register
Address: 0x5010

HEX1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	-	-	-	HEX1						
Mode	r0	r0	r0	r0	r0	r0	r0	r0	r0	w						
Reset	-	-	-	-	-	-	-	-	-	0x00						

Seven Segment Digit 1 Register
Address: 0x5012

HEX2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	-	-	-	HEX2						
Mode	r0	r0	r0	r0	r0	r0	r0	r0	r0	w						
Reset	-	-	-	-	-	-	-	-	-	0x00						

Seven Segment Digit 2 Register
Address: 0x5014

HEX3

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	-	-	-	HEX3						
Mode	r0	r0	r0	r0	r0	r0	r0	r0	r0	w						
Reset	-	-	-	-	-	-	-	-	-	0x00						

Seven Segment Digit 3 Register
Address: 0x5016

The registers HEX0—HEX3 control the segments of the four-digit hexadecimal display of the evaluation board.

A set bit means the segment is on, a reset bit means the segment is off.

KEY

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	-	-	-	-	-	-	KEY			
Mode	r0	r0	r0	r0	r0	r0	r0	r0	r0	r0	r0	r0	r			
Reset	-	-	-	-	-	-	-	-	-	-	-	-	-			

Pushbuttons Register
Address: 0x5020

The KEY register contains the state of the four pushbuttons of the evaluation board.

A set bit means the button is not pressed, a reset bit means the button is pressed.

SW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	SW									
Mode	r0	r0	r0	r0	r0	r0	r									
Reset	-	-	-	-	-	-	-									

Toggle Switch Register
Address: 0x5022

The SW register contains the state of the ten switches of the evaluation board.

A set bit means the switch is on, a reset bit means the switch is off.

ENDPI0_CONTROL

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	-	-	-	-	-	-	-	STALL	ACK	FULL
Mode	r0	r0	r0	r0	r0	r0	r0	r0	r0	r0	r0	r0	r0	w	w	r
Reset	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0

Endpoint In 0 Control Register
Address: 0x6000

Name	Function
STALL	Request a STALL answer to the host for the next handshake. Cleared by hardware when a new SETUP is received. 0: no stall 1: stalled
ACK	Acknowledge IN data 0: send NAK 1: send DATA packet
FULL	FIFO full bit 0: FIFO is not full 1: FIFO is full

The STALL bit will be automatically cleared after every SETUP token. The ACK bit will be cleared after every IN transaction.

ENDPI0_DATA

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	-	-	DATA							
Mode	r0	r0	r0	r0	r0	r0	r0	r0	w							
Reset	-	-	-	-	-	-	-	-	-							

Endpoint In 0 Data Register
Address: 0x6002

A write access to DATA will put a data into the FIFO of the IN endpoint.

ENDPI1_CONTROL

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	-	-	-	-	-	-	-	STALL	ACK	FULL
Mode	r0	r0	r0	r0	r0	r0	r0	r0	r0	r0	r0	r0	r0	w	w	r
Reset	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0

Endpoint In 1 Control Register
0x6004

ENDPI1_DATA

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	-	-	DATA							
Mode	r0	r0	r0	r0	r0	r0	r0	r0	w							
Reset	-	-	-	-	-	-	-	-	-							

Endpoint In 1 Data Register
0x6006

See ENDPI0_CONTROL and ENDPI0_DATA.

ENDPO0_CONTROL

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EMPTY
Mode	r0	r0	r0	r0	r0	r0	r0	r0	r0	r0	r0	r0	r0	r0	r0	r
Reset	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0

Endpoint Out 0 Control Register
Address: 0x6040

Name	Function
EMPTY	FIFO empty bit 0: FIFO contains data 1: FIFO is empty

ENDPO0_DATA

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	-	-	DATA							
Mode	r0	r0	r0	r0	r0	r0	r0	r0	r							
Reset	-	-	-	-	-	-	-	-	-							

Endpoint Out 0 Data Register
Address: 0x6042

In order to read data from the FIFO of the OUT endpoint the bit ENDPO0_CONTROL.RDREQ must be set first. The following read access of DATA will fetch the FIFO item.

USB_ADDRESS

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	-	-	-	DEVICE_ADDRESS						
Mode	r0	r0	r0	r0	r0	r0	r0	r0	r0	rw						
Reset	-	-	-	-	-	-	-	-	-	0x00						

USB Address Register
Address: 0x6100

USB_TOKEN

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	-	-	-	-	TOKEN		ENDP			
Mode	r0	r0	r0	r0	r0	r0	r0	r0	r0	r0	r		r			
Reset	-	-	-	-	-	-	-	-	-	-	00		0x0			

USB Token Register
Address:0x6102

Name	Function
TOKEN	Token of the last transaction. Bit 4 determines the direction of the transfer. 00: - 01: OUT 10: IN 11: SETUP
ENDP	These bits encode the endpoint address that received or transmitted the previous token. The base address of the endpoint can be calculated with 0x6000 + 2 · USB_STATUS[4:0].

USB_STATUS

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	-	-	-	BTO	CRC16	CRC5	PID	USB_ RESET	STALL	TOKEN_ DONE
Mode	r0	r0	r0	r0	r0	r0	r0	r0	r0	rw1	rw1	rw1	rw1	rw1	rw1	rw1
Reset	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0

USB Status Register
Address: 0x6104

Name	Function
BTO	This bit is set if a bus turnaround time-out error has occurred. This USB uses a bus turnaround timer to keep track of the amount of time elapsed between the token and data phases of a SETUP or OUT token or the data and handshake phases of an IN token. If more than 17 bit times are counted from the previous EOP before a transition from IDLE, a bus turnaround time-out error will occur.
CRC16	The CRC16 failed.
CRC5	The CRC5 failed.
PID	The PID check failed.
USB_RESET	This bit is set when the USB has decoded a valid USB Reset.
STALL	A STALL handshake was sent by the SIE.
TOKEN_DONE	This bit is set when the current token being processed is complete. The microprocessor should immediately read the USB_STATUS register to determine the Endpoint number and direction used for this token. Clearing this bit causes the USB_STATUS register to be cleared or the USB_STATUS holding register to be loaded into the STAT register if another token has been processed.

Status flags of the SIE. If a ‘1’ is written the flag is cleared.