

# EECS 16A

## Circuit Analysis



Vide source: [www.afrotechmods.com](http://www.afrotechmods.com)  
Do not try this at home (or in the EECS 16A Lab)

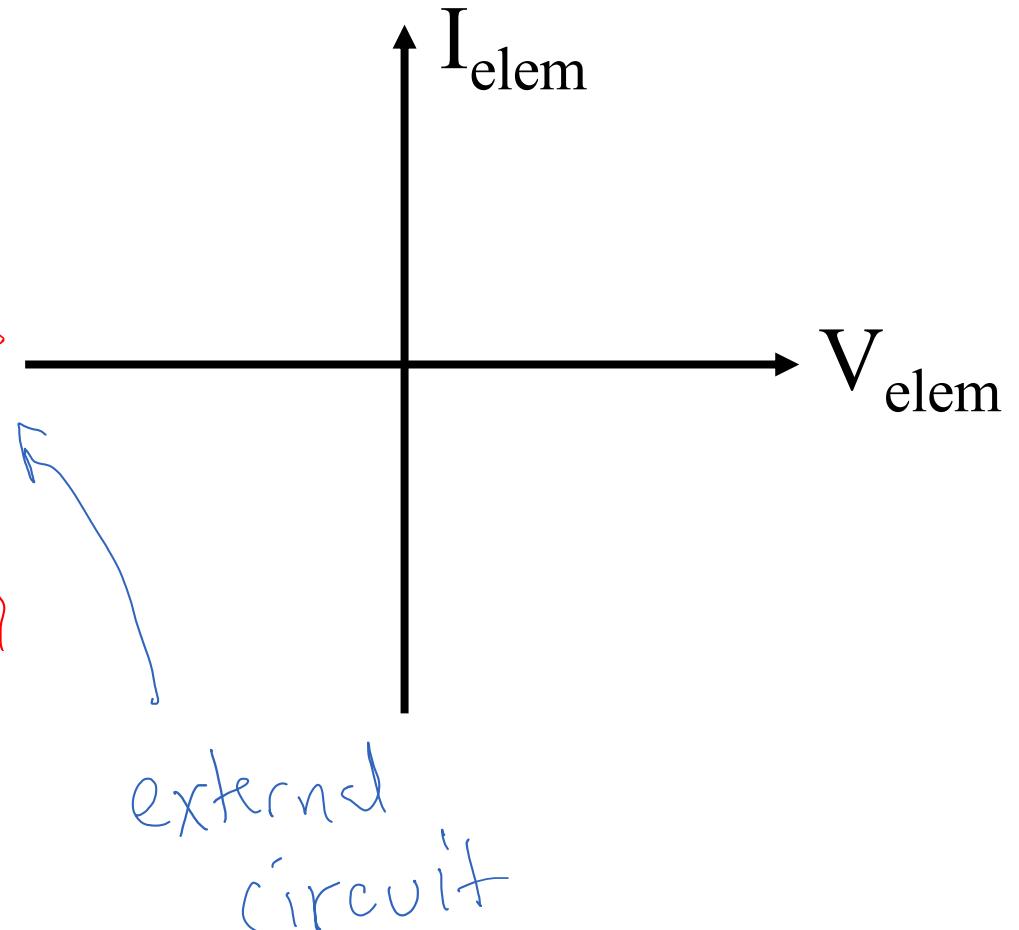
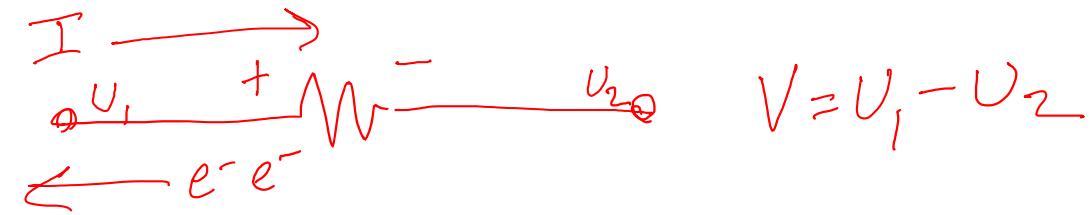
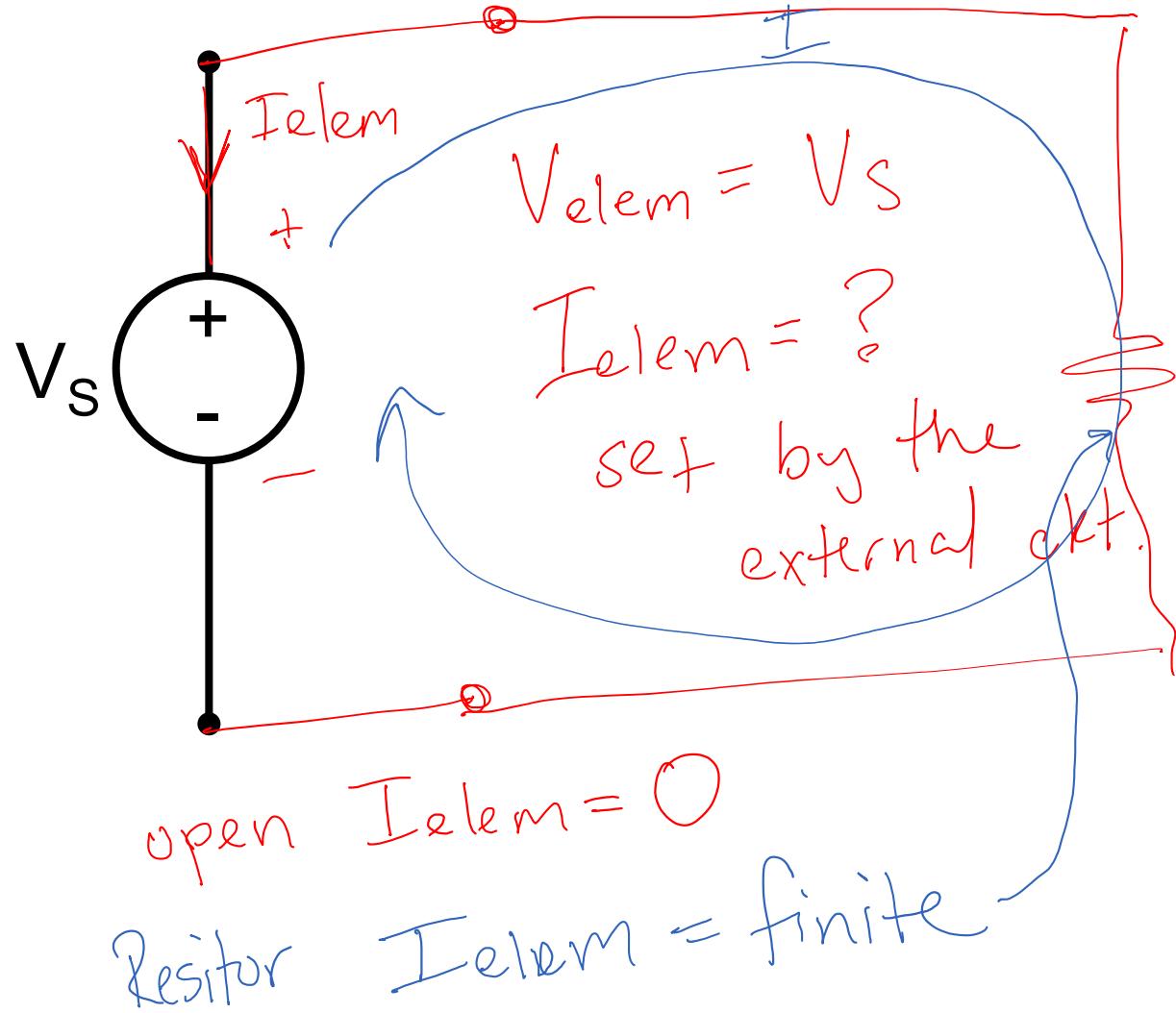
# Admin

First Midterm Exam: Wednesday March 1, 7-9pm  
Covers Module 1 Material up to 2/16 lecture.

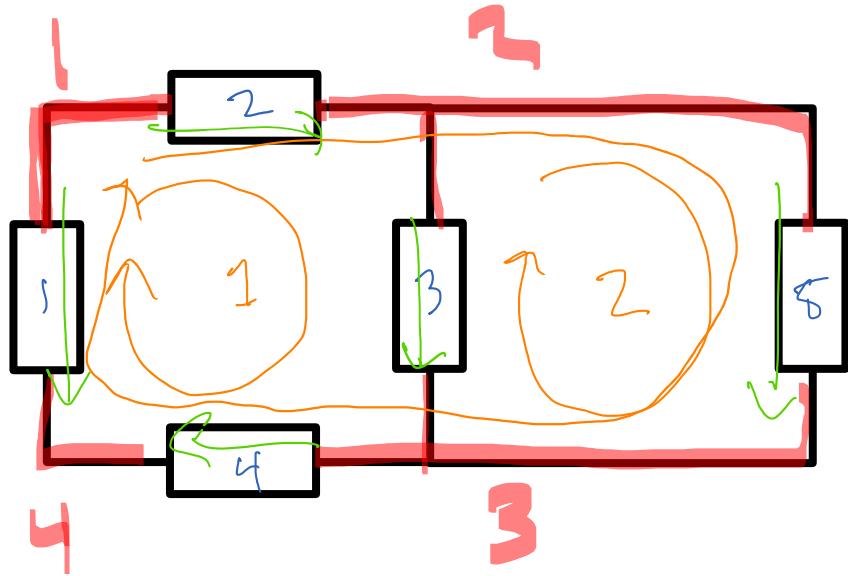
Things I shouldn't have to say...

Cheating

# “Value Set By External Circuit”



# Recap: Nodes, Branches, Loops



Elements? 5

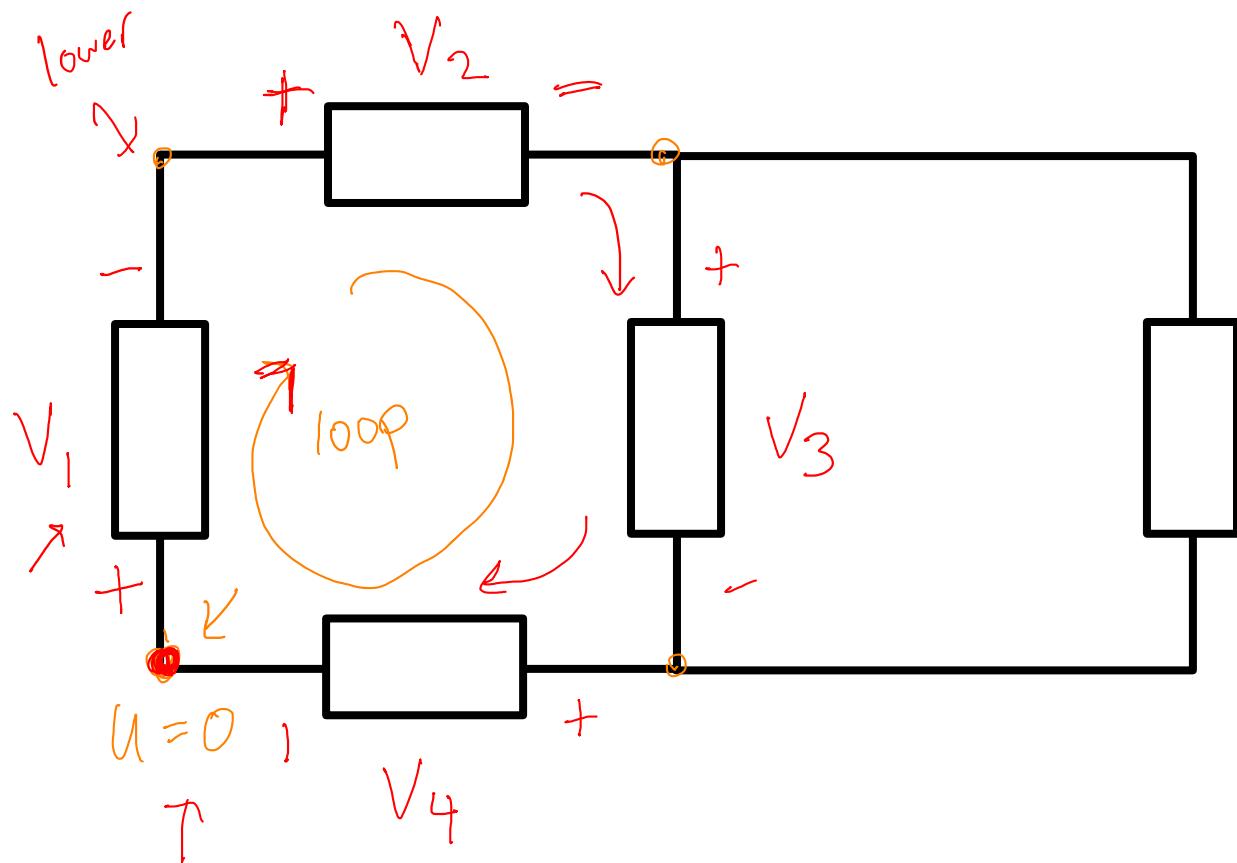
How many nodes in this circuit? 4

How many branches? 5

How many loops? 3

# Rules for circuit analysis: Kirchoff's Voltage Law (KVL)

Sum of voltages across the elements in a loop equal zero

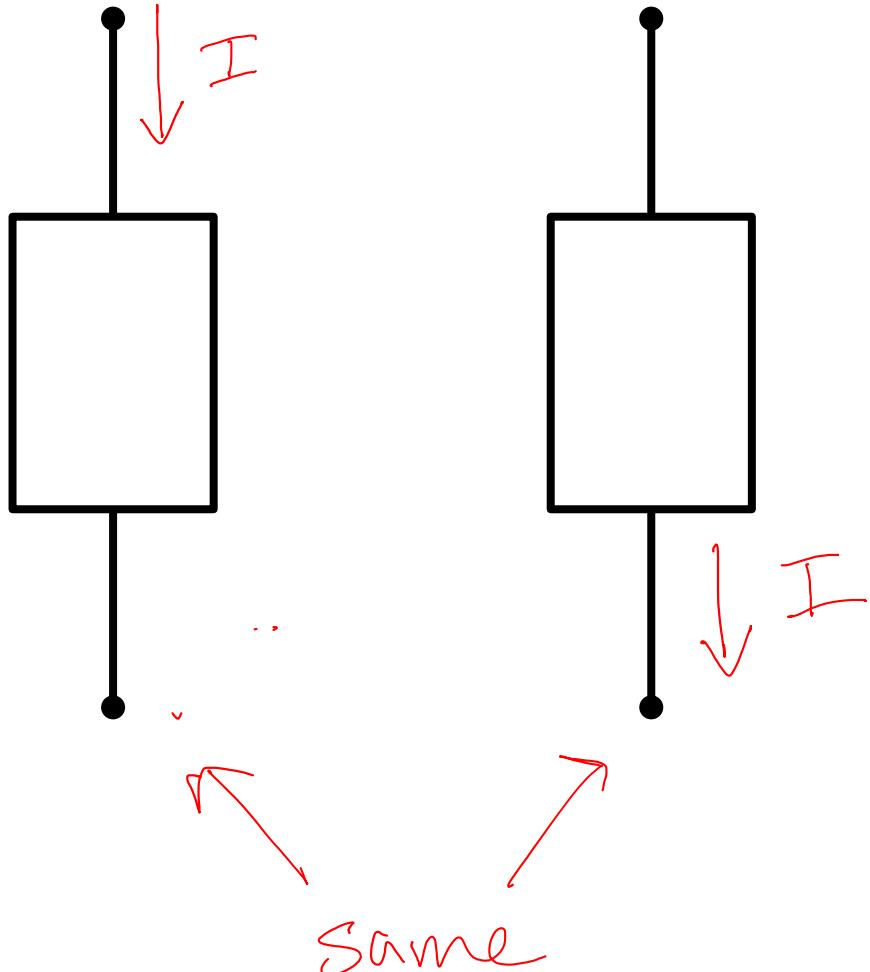


$$0 - V_1 - V_2 - V_3 - V_4 = 0$$
$$\Rightarrow V_1 + V_2 + V_3 + V_4 = 0$$

Some can be positive  
Some can be negative  
(mix of + & -)

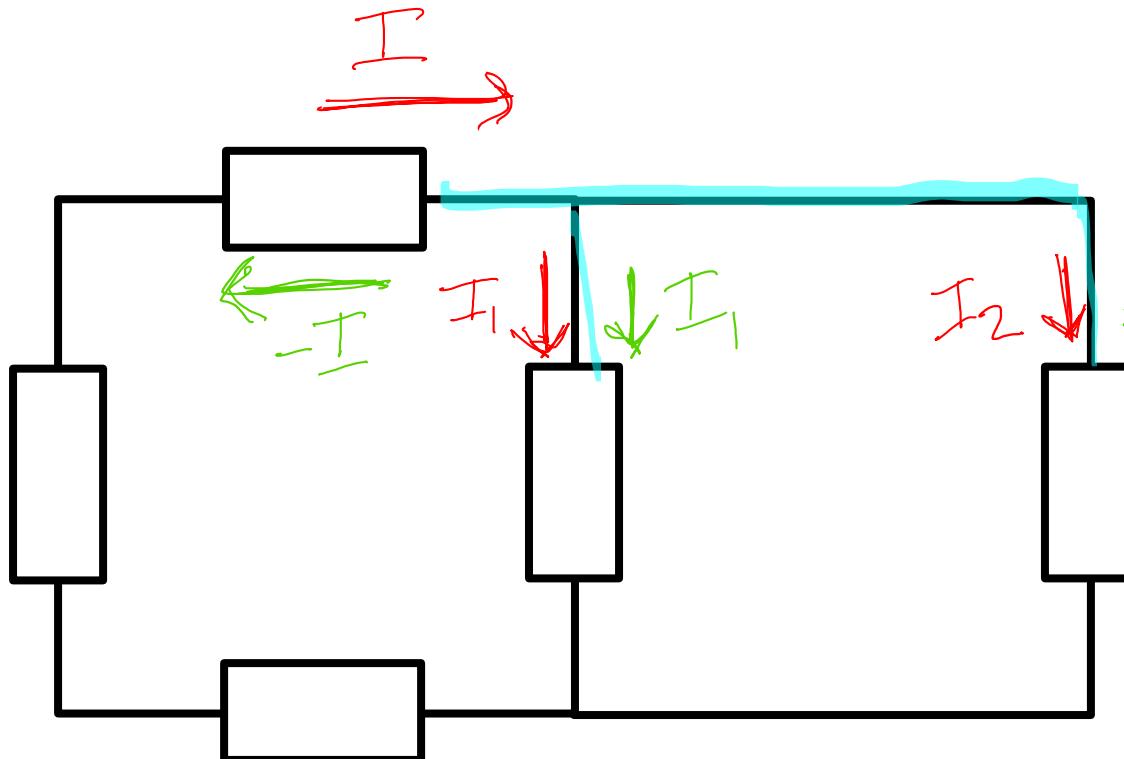
# Rules for circuit analysis: Kirchoff's Current Law (KCL) In-element

The current flowing into an element must equal the current flowing out

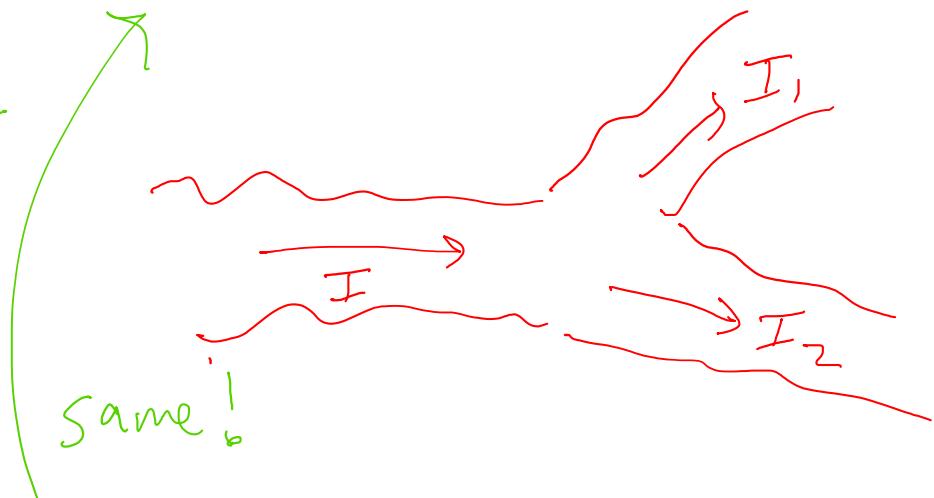


# Rules for circuit analysis: Kirchoff's Current Law (KCL)

The current flowing into any node must equal the current flowing out  
→ (same as: all currents flowing out of a node sum to 0)



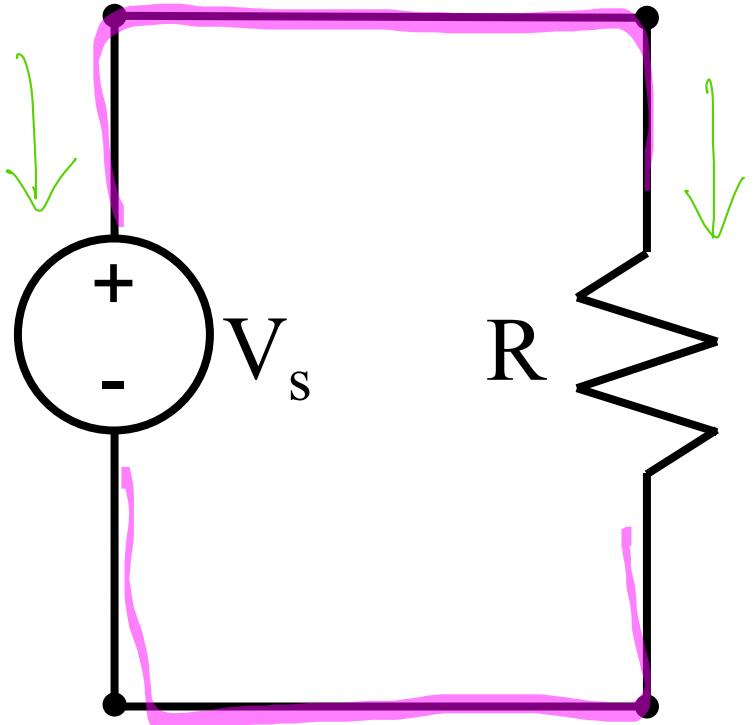
$$I = I_1 + I_2$$



$$I_1 + I_2 - I = 0$$

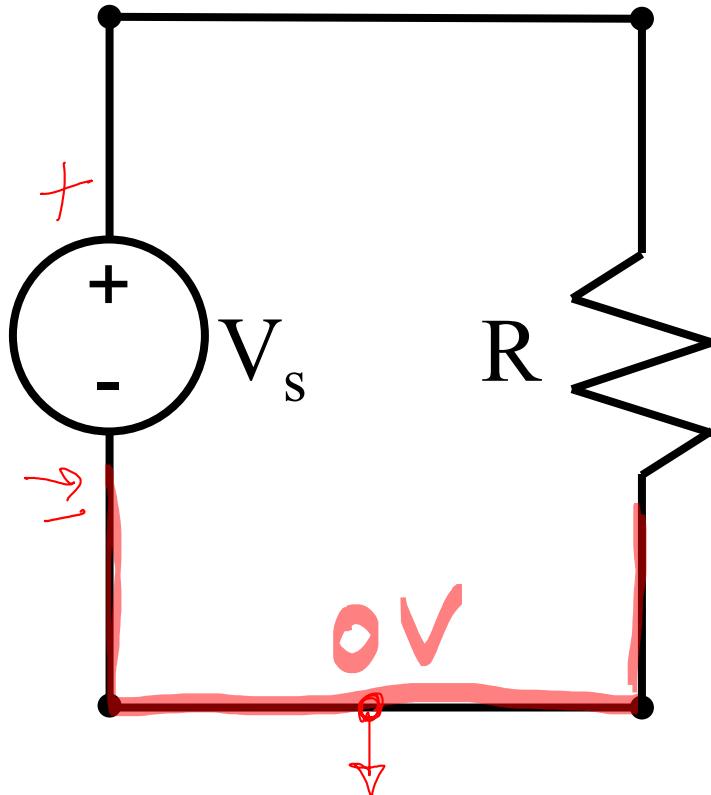
# Example Circuit: Find all node voltages and branch currents

potentials



# Circuit Analysis Algorithm: Step 1

Pick a reference node and label it as 0 potential (ground).  
All voltages are measured relative to this node.

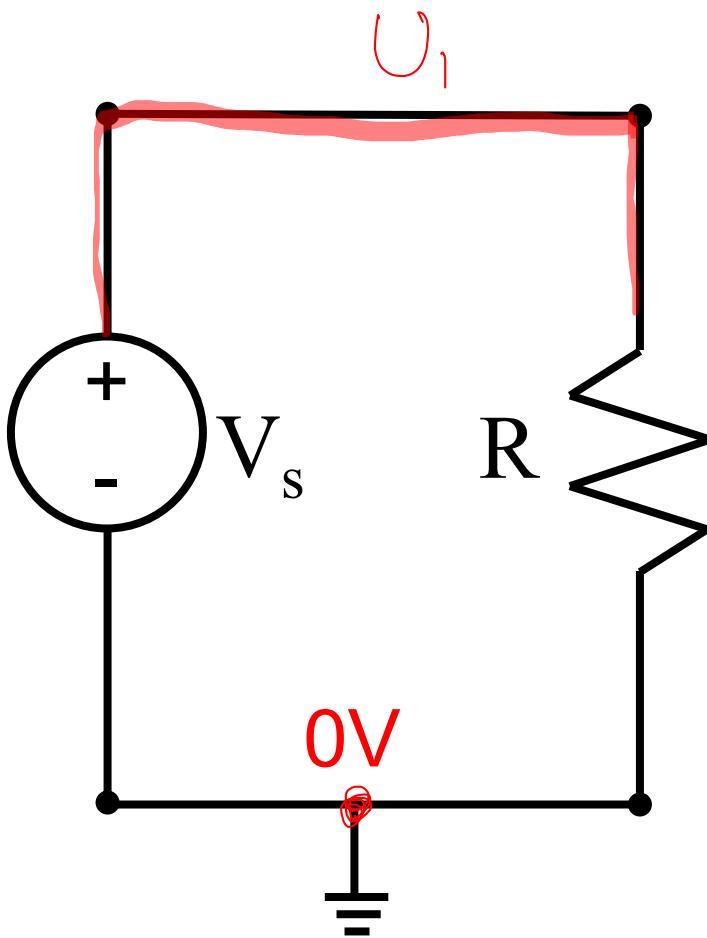


0V → "ground"  
gnd  
↓  
=

a good location is negative  
terminal of source  
(but not required)

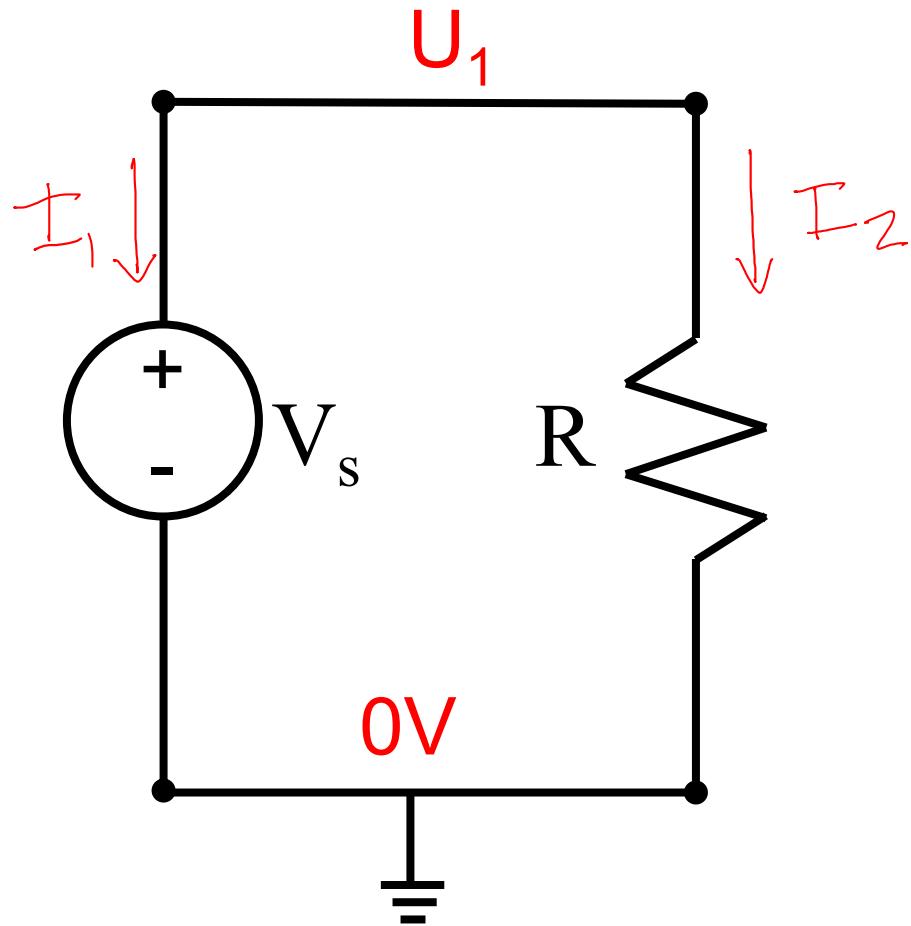
# Circuit Analysis Algorithm: Step 2

Label all remaining nodes as potentials  $U_i$   
[ $U_1 \dots U_{N-1}$ ]



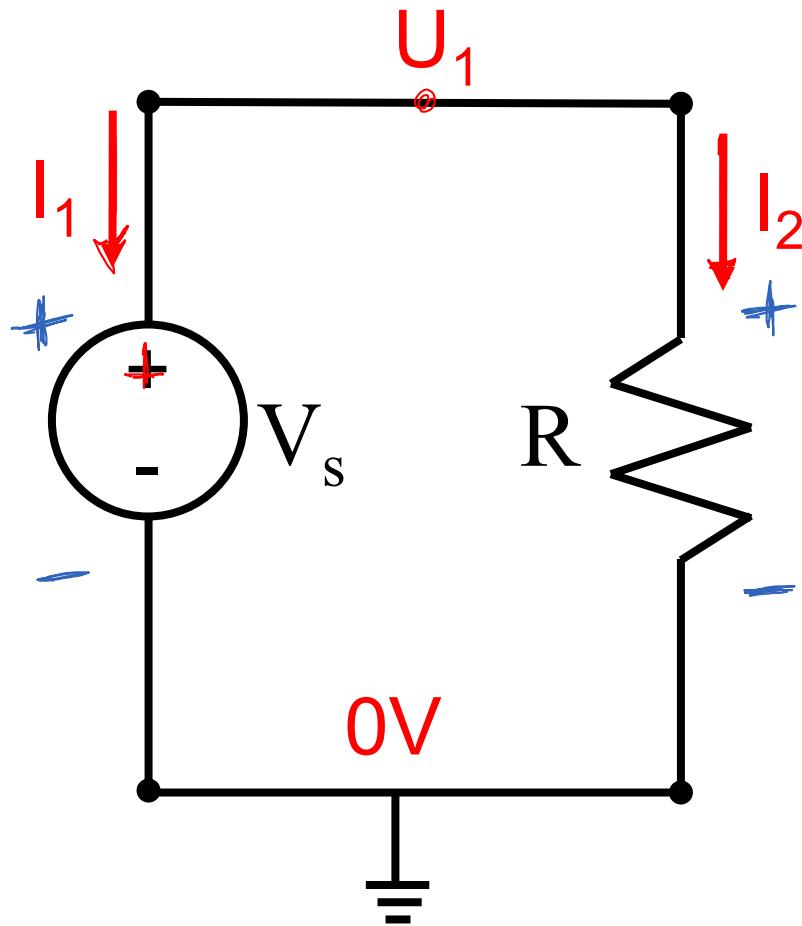
# Circuit Analysis Algorithm: Step 3

Label all branch currents with  $I_i$   
 $[I_1 \dots I_k]$

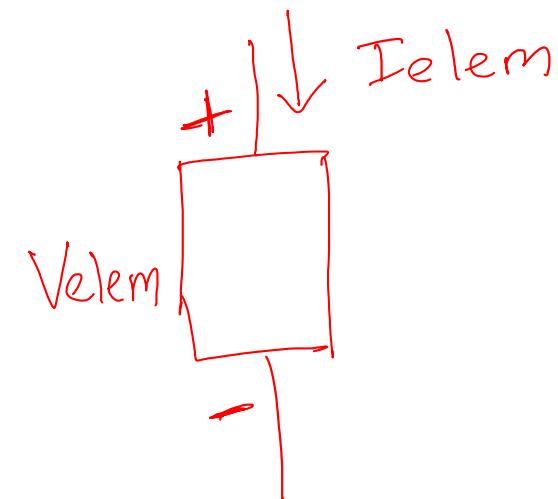


# Circuit Analysis Algorithm: Step 4

Add signs + and – element voltages to each element following the passive sign convention

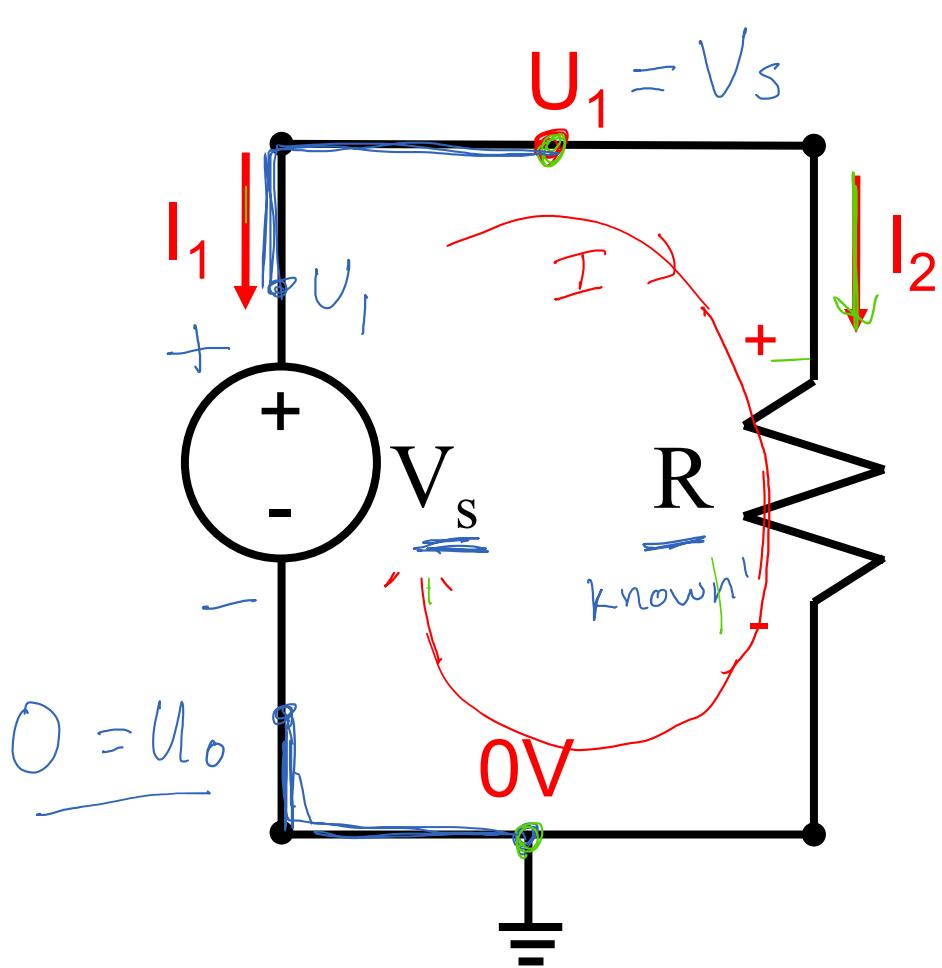


Passive sign convention:  
Positive current enters  
positive voltage terminal



# Circuit Analysis Algorithm: Step 5

Identify unknowns and reduce using KVL/KCL



→ all currents flowing out of anode = 0

unknowns:  ~~$I_1, I_2$~~ ,  $\underline{I}$

KCL:  $I_1 + I_2 = 0$  ←  
 ~~$I_2 = -I_1 = I$~~  ←

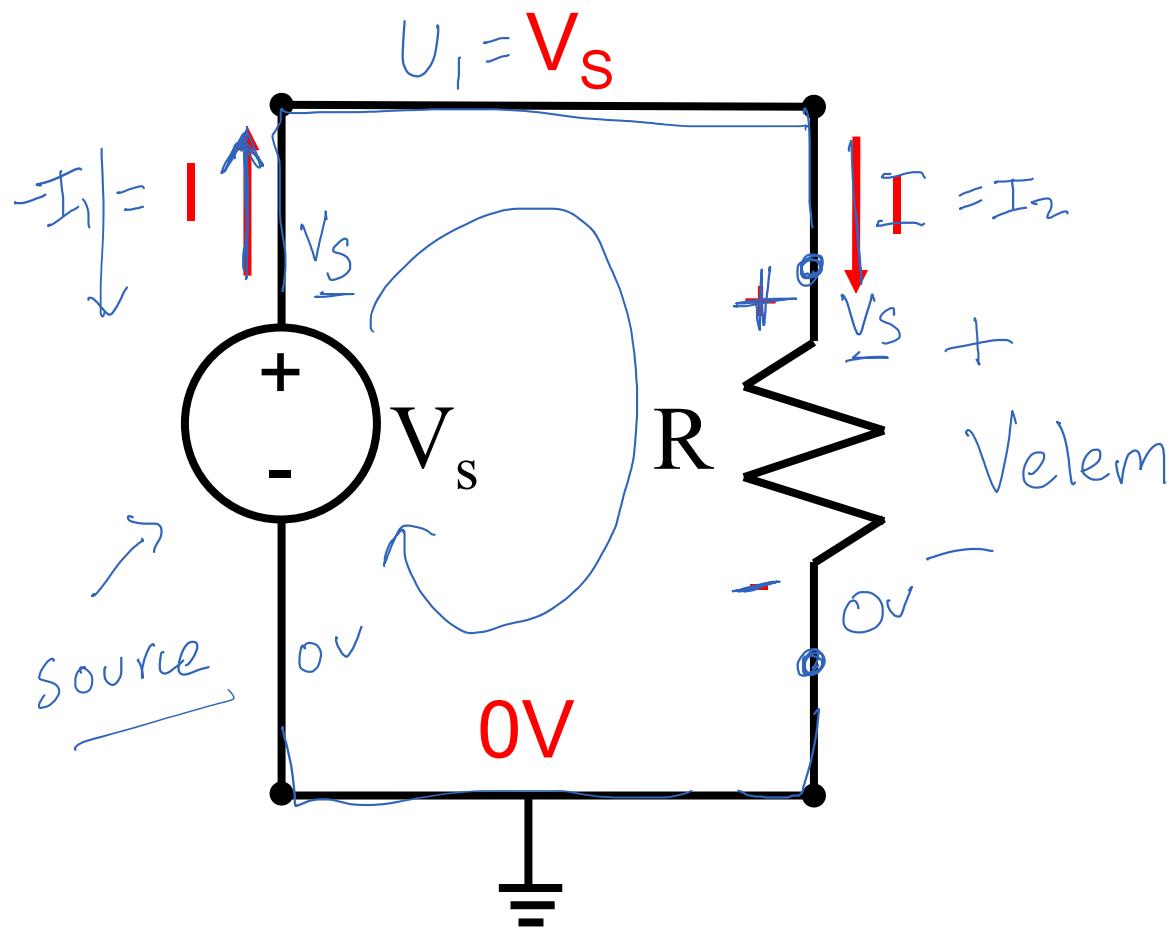
KVL:  $V_s = U_1 - U_0$

$V_s = U_1 - 0$

$V_s = U_1$

# Circuit Analysis Algorithm: Step 6

Identify remaining unknowns and set up a system of linear equations to solve using KVL/KCL/I-V equations



$$V = IR$$

$V_s - 0 = IR$  known!

$$I = \frac{V_s}{R}$$

# Circuit Analysis Algorithm: Step 7 (if needed)

Is the system of equations complicated? Linear Algebra can help!

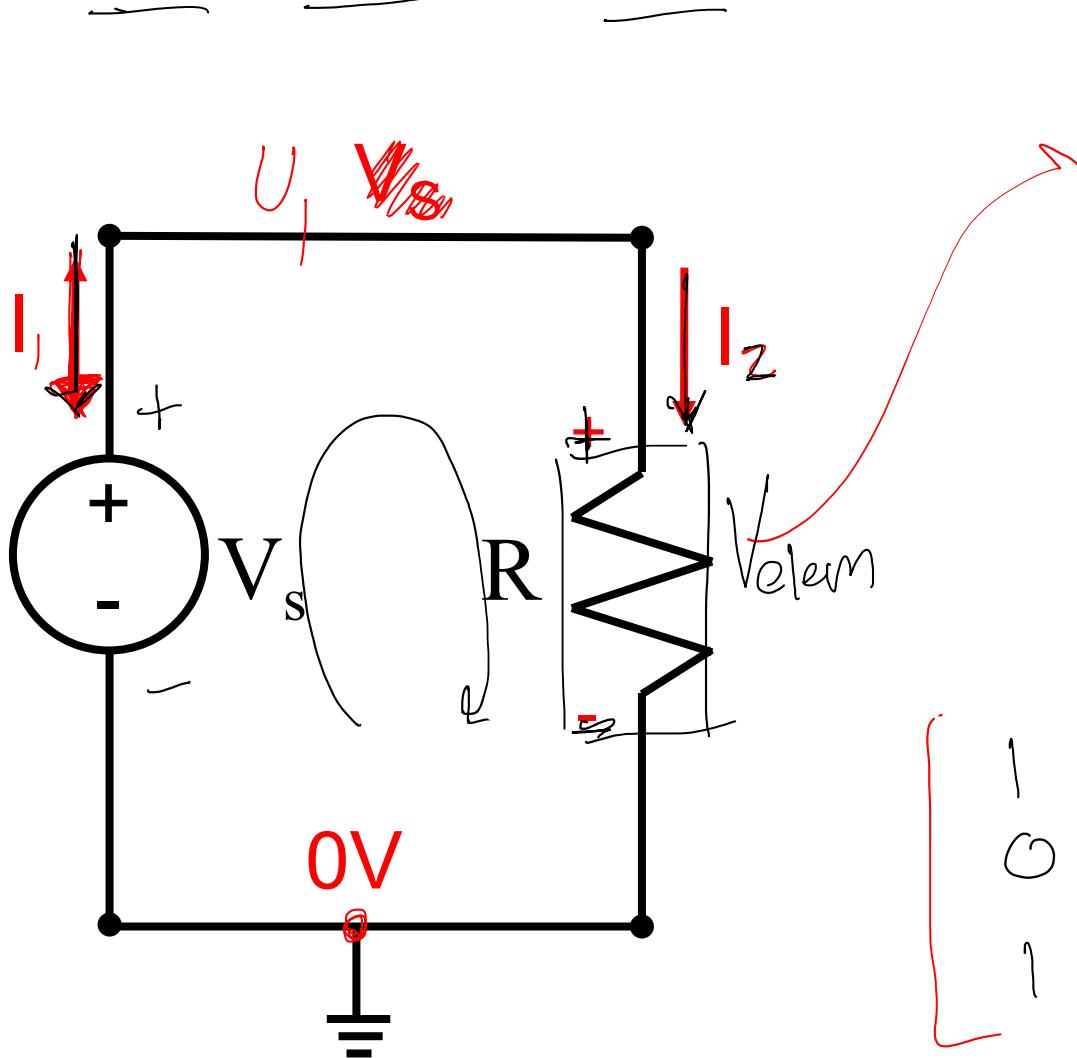
$$A\vec{x} = \vec{b}$$

$\vec{x}$  Unknowns (currents and potentials)  
 $\vec{b}$  Knowns/constants  
 $A$  Knowns/constants

$$\begin{matrix} A & \xrightarrow{\quad} & \vec{x} & \xleftarrow{\quad} \\ \left[ \begin{array}{cccc|c} 1 & -1 & 0 & 0 & 0 \\ 0 & 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & -1 & 0 \\ 0 & 0 & 0 & 1 & 0 \end{array} \right] & = & \left[ \begin{array}{c} U_1 \\ I_1 \\ I_2 \end{array} \right] & = & \left[ \begin{array}{c} b_1 \\ b_2 \\ b_3 \\ b_4 \end{array} \right] \end{matrix}$$

# Circuit Analysis Algorithm: Step 7 (if needed)

Use KCL, KVL and  $V=IR$  to fill in  $A$  and  $\vec{b}$



$$V=IR : U_1 - 0 = I_2 R$$

$$U_1 - I_2 R = 0$$

$$KCL : I_1 + I_2 = 0$$

$$KVL : V_s = V_{elem} = U_1 - 0$$

$$V_s = U_1$$

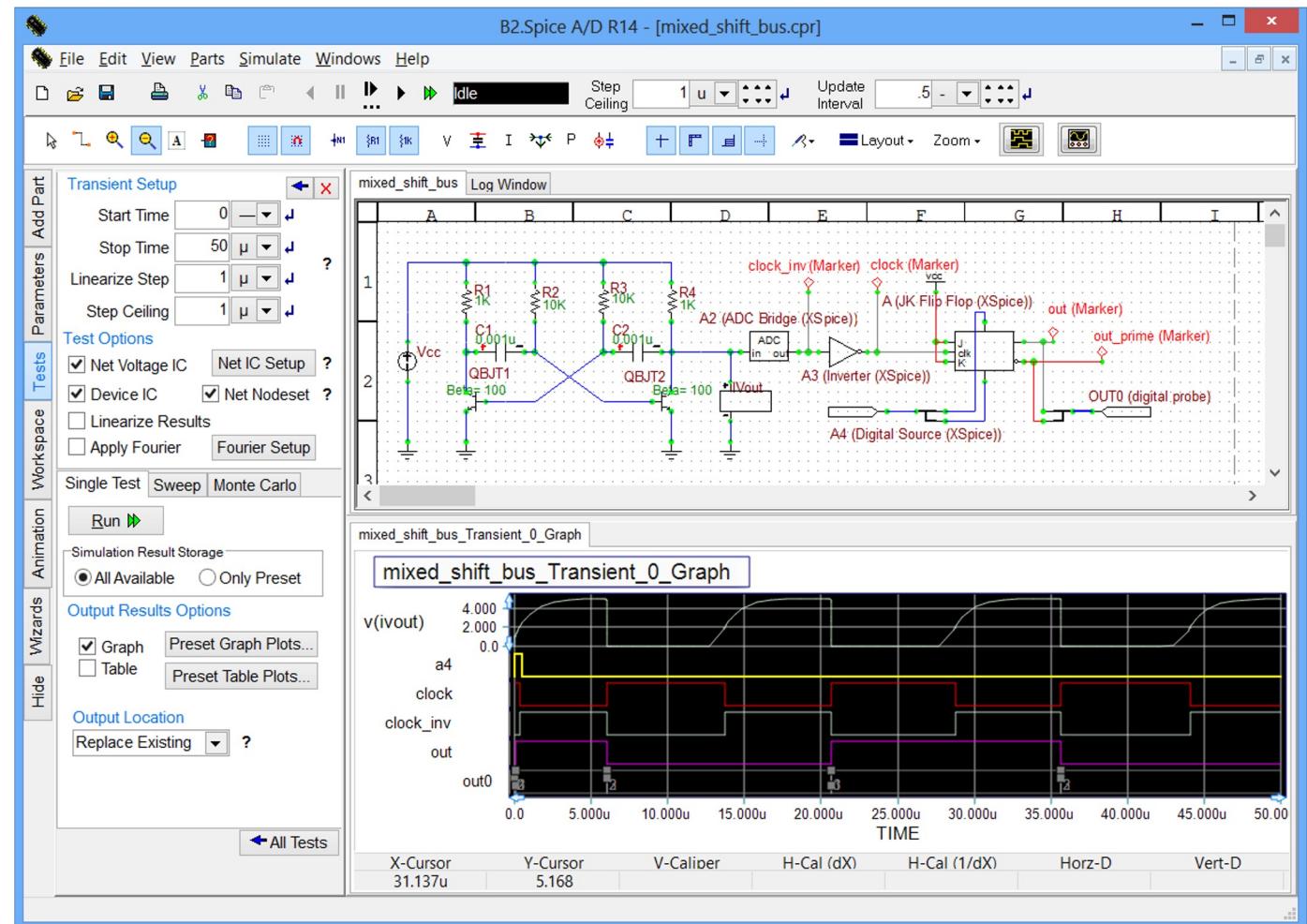
$$U_1 = V_s$$

$$A \quad \begin{bmatrix} 1 & 0 & -R \\ 0 & 1 & 1 \\ 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} U_1 \\ I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ V_s \end{bmatrix}$$

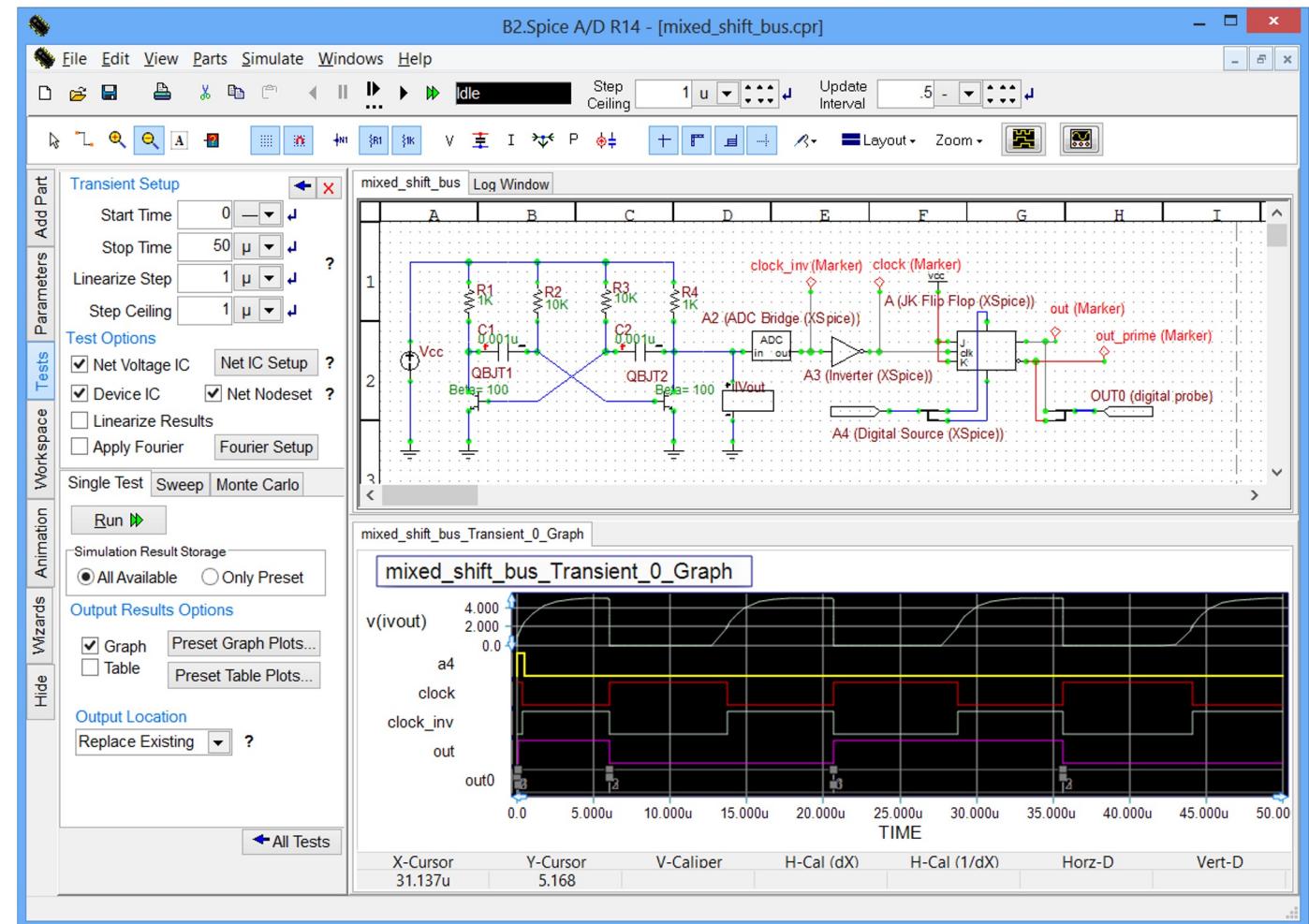
# Electronic Design Automation (tool)

SPICE (Simulation Program with Integrated Circuit Emphasis): started as a student project at Berkeley!

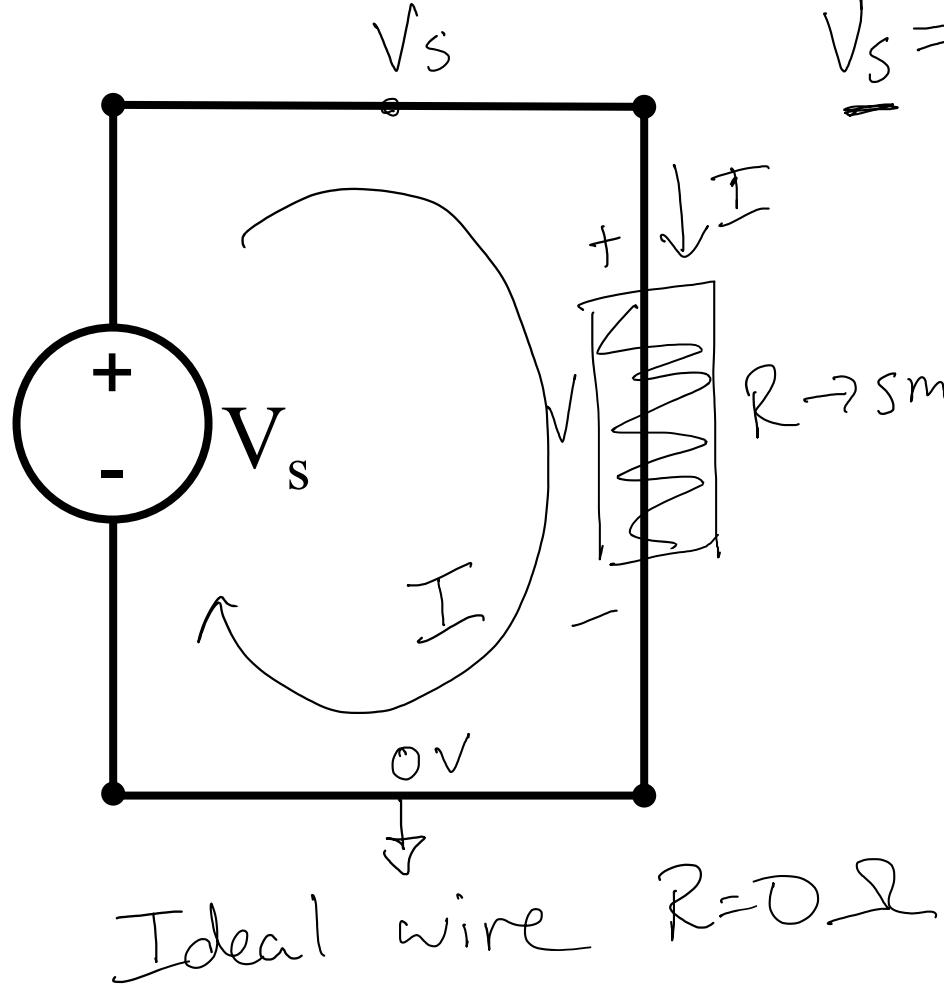
Now the basis for open-source electronic circuit simulation, to design and model device characteristics and check circuit boards



# Electronic Design Automation (tool)

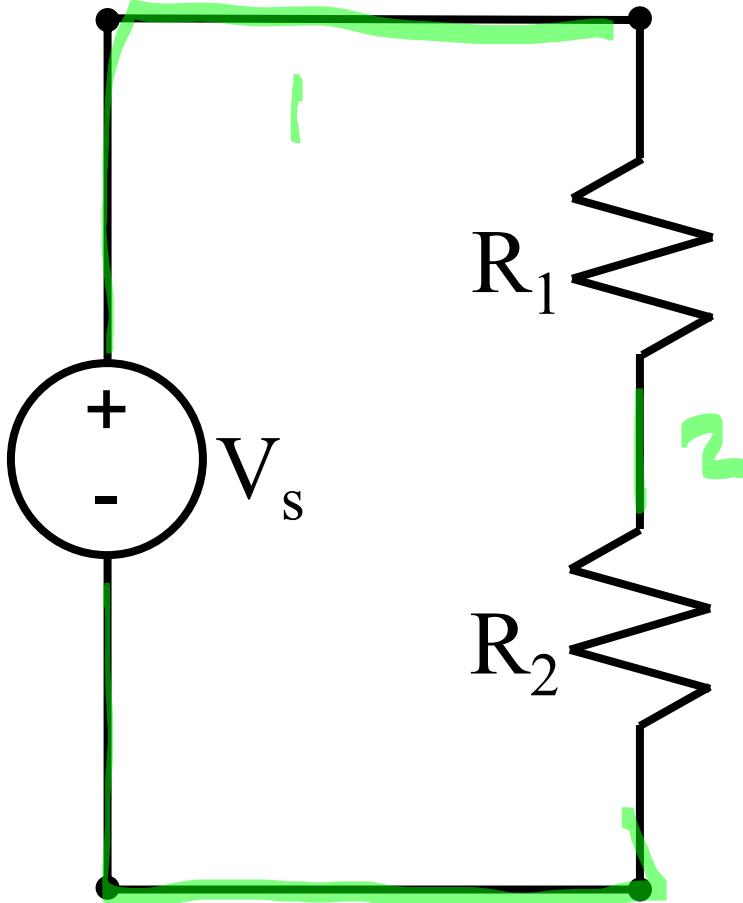


# What Happens When You Short A Voltage Source?



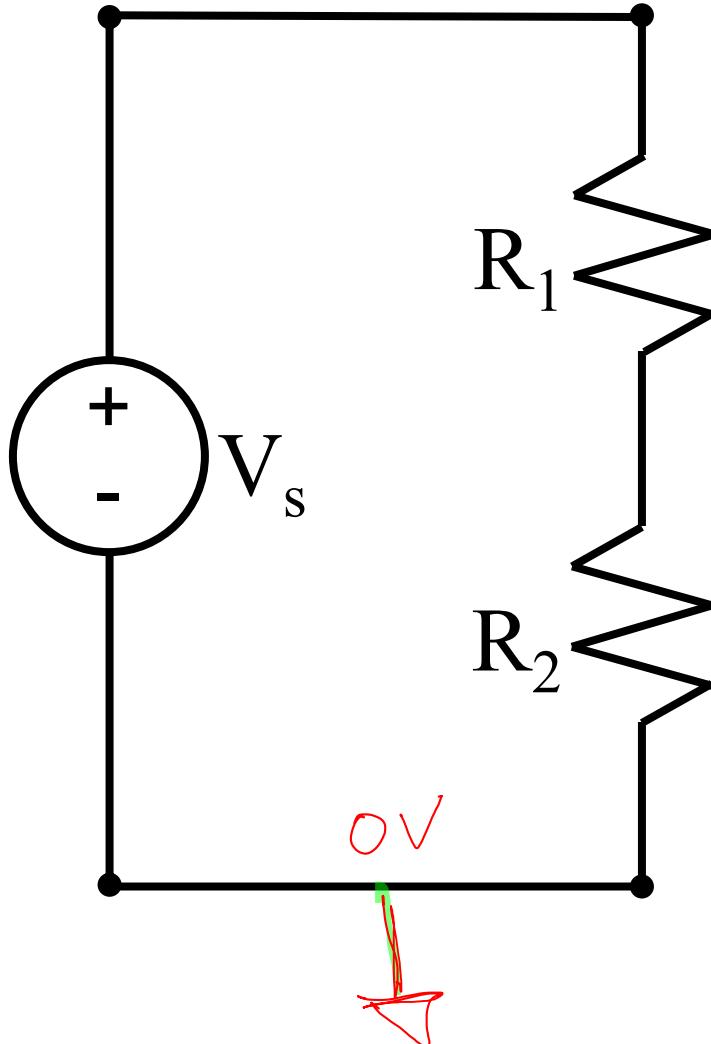
# Simplifying Circuit Analysis: The Voltage Divider

Find all node voltages and branch currents

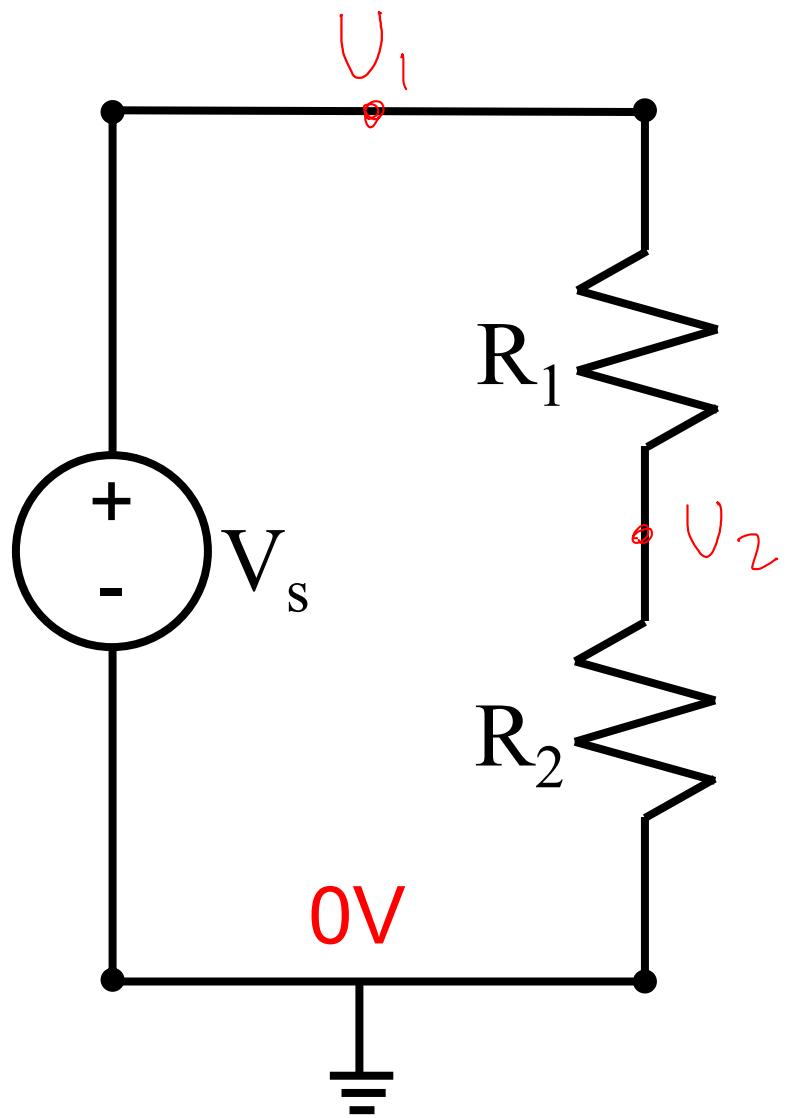


# Circuit Analysis Algorithm: Step 1

Pick a reference node and label it as 0 potential (ground).



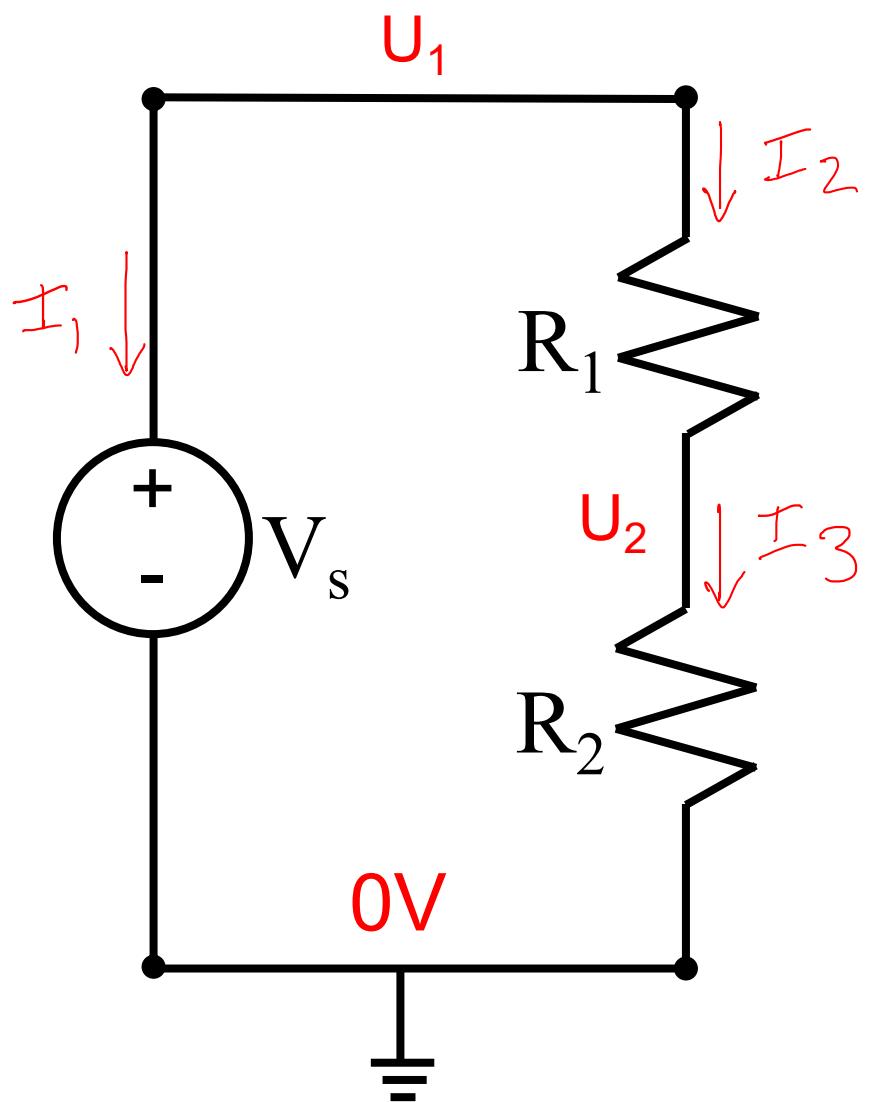
# Circuit Analysis Algorithm: Step 2



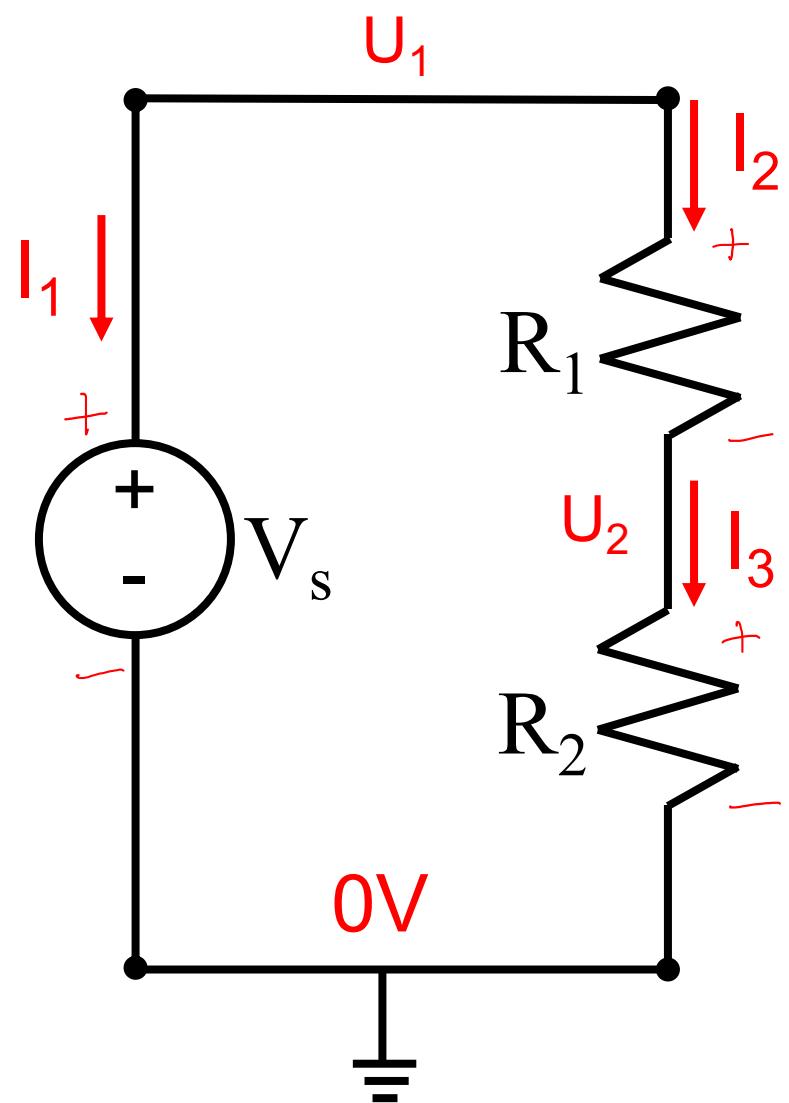
Label all remaining nodes as potentials  $U_i$   
[ $U_1 \dots U_{N-1}$ ]

# Circuit Analysis Algorithm: Step 3

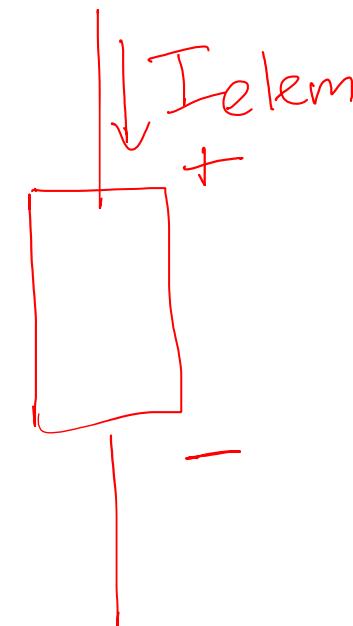
Label all branch currents with  $I_i$   
[ $I_1 \dots I_k$ ]



# Circuit Analysis Algorithm: Step 4

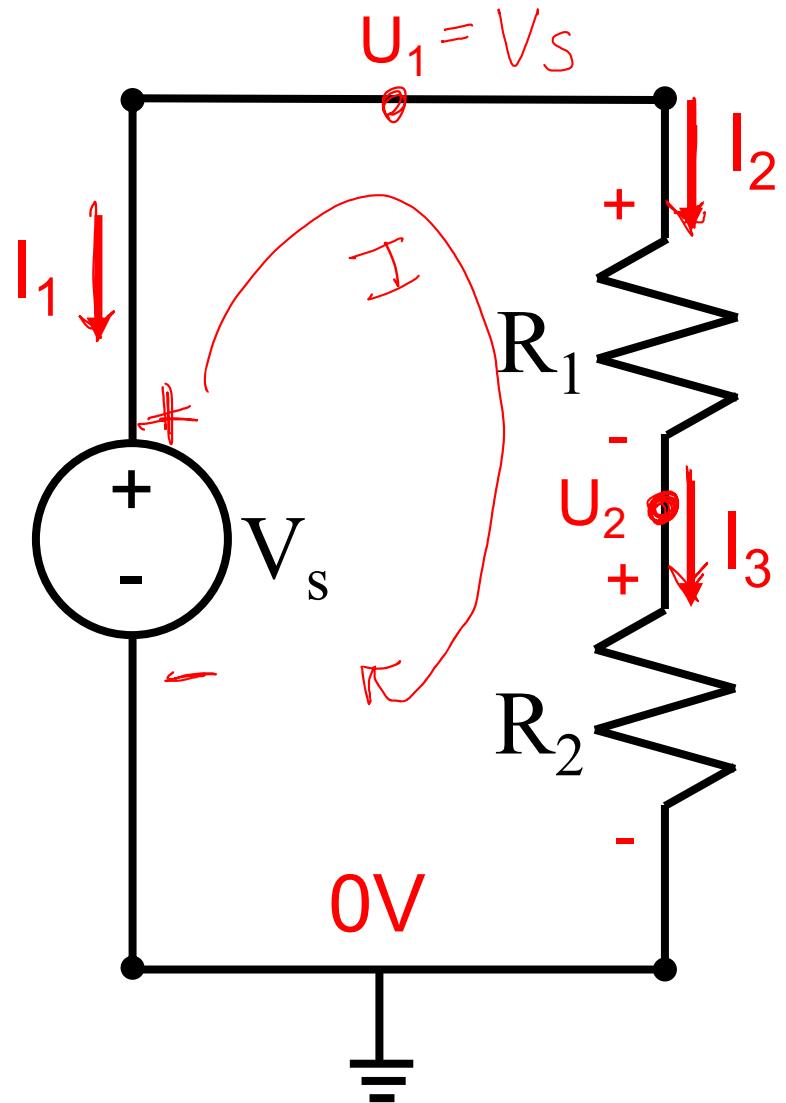


Add signs + and – element voltages to each element following the passive sign convention



# Circuit Analysis Algorithm: Step 5

Identify unknowns and  
reduce using KVL/KCL



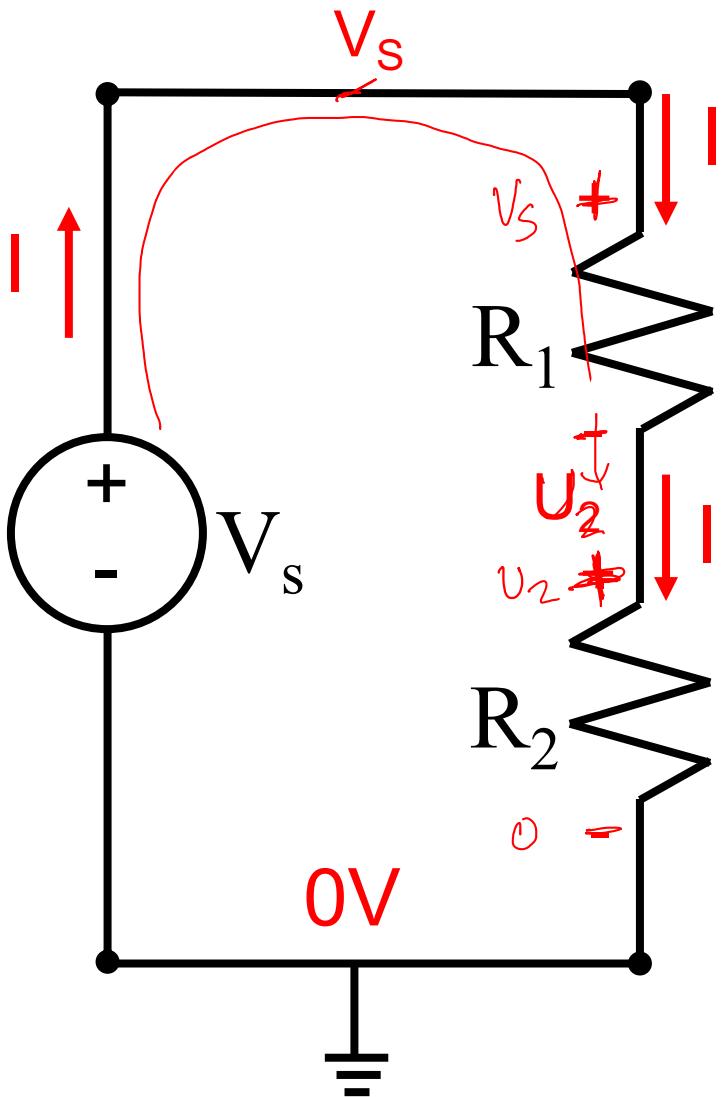
Unknowns:  $U_1, U_2, I_1, I_2, I_3$

$V_s = U_1 - 0 \quad V_s = U_1$

KCL:  $I_1 + I_2 = 0$

$I = I_2 = -I_1 = I_3$

# Circuit Analysis Algorithm: Step 6



Identify remaining unknowns and set up a system of linear equations to solve using KVL/KCL/I-V equations

Unknowns:  $I, U_2$

Ohm's law :  $V = I R_1$

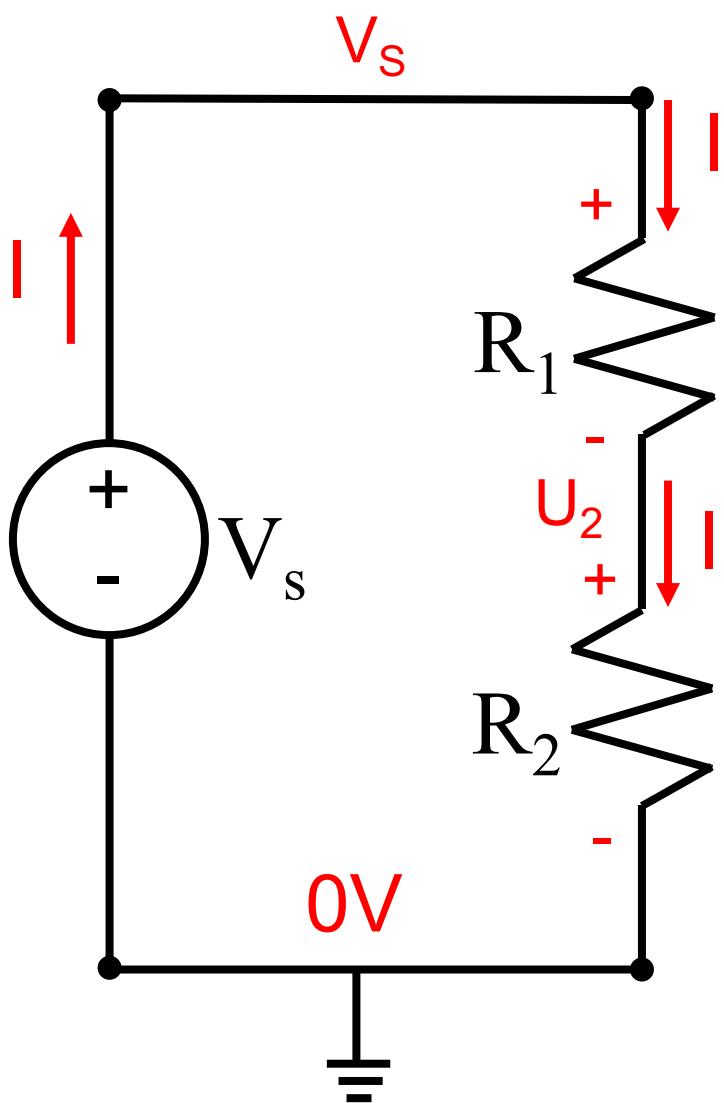
$$V_s - U_2 = I R_1$$

$$* I R_1 + U_2 = V_s$$

$$U_2 - 0 = I R_2$$

$$* I R_2 - U_2 = 0$$

# Circuit Analysis Algorithm: Step 7 (if needed)



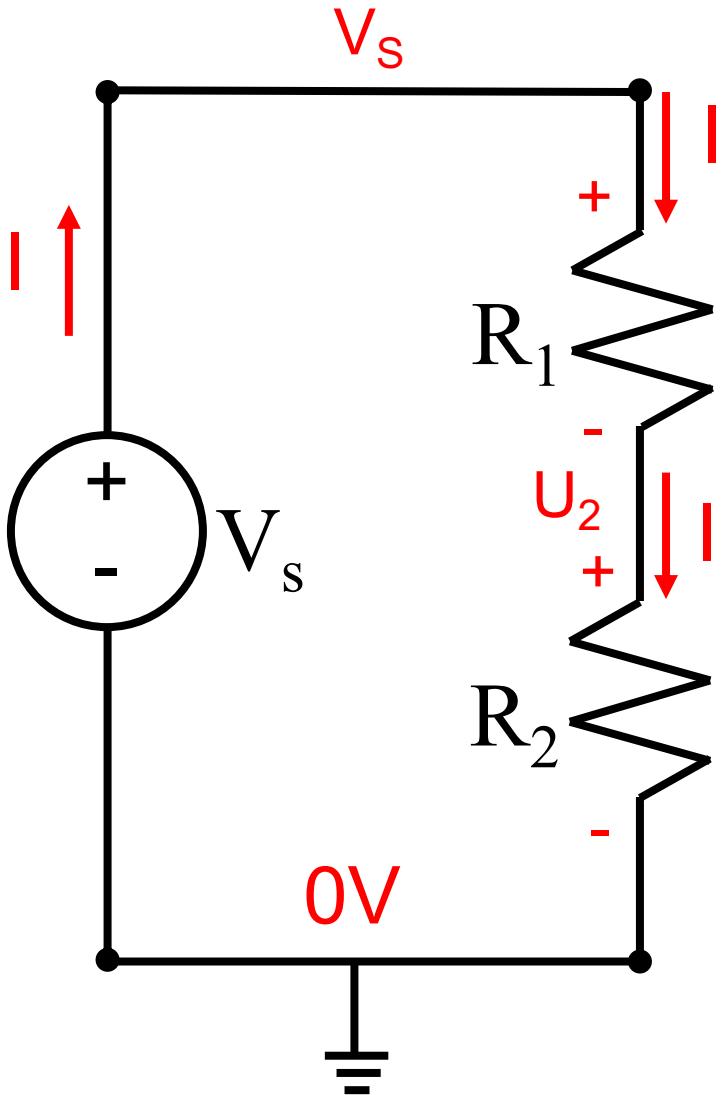
Is the system of equations complicated? Linear Algebra can help!  $A\vec{x} = \vec{b}$

$$\rightarrow IR_1 + U_2 = V_s$$

$$\rightarrow IR_2 - U_2 = 0$$

$$\begin{bmatrix} R_1 & 1 \\ R_2 & -1 \end{bmatrix} \begin{bmatrix} I \\ U_2 \end{bmatrix} = \begin{bmatrix} V_s \\ 0 \end{bmatrix}$$

# Voltage Divider Summary



$$I = \frac{V_s}{R_1 + R_2}$$
$$U_2 = \frac{V_s R_2}{R_1 + R_2}$$

# Voltage Divider Analogy

