EECS 16A Designing Information Devices and Systems I
Fall 2022 Homework 10

This homework is due November 11, 2022, at 23:59.
Self-grades are due November 14, 2022, at 23:59.

Submission Format
Your homework submission should consist of **one** file.

- `hw10.pdf`: A single PDF file that contains all of your answers (any handwritten answers should be scanned).

Submit the file to the appropriate assignment on Gradescope.

1. Reading Assignment

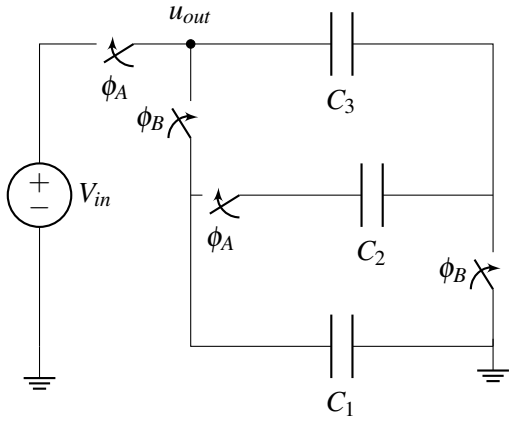
For this homework, please read Note 17A to learn about comparators and op-amps, Note 17B to learn about charge sharing, as well as the charge sharing circuit cookbook in the resources section of the course website. You are always encouraged to read beyond this as well.

(a) If the op-amp supply voltages are $V_{DD} = 5\,\text{V}$ and $V_{SS} = 0\,\text{V}$, then what is the minimum/maximum value of V_{out}?

(b) What is the purpose of a comparator? How can we use a comparator circuit to detect a touch for a capacitive touchscreen?

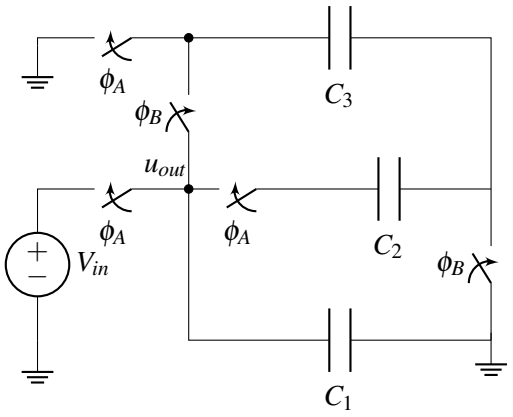
2. Charge sharing check-in

(a) Let us analyze the capacitor circuit shown below. Let us set all of the capacitors to have the same capacitance $C_1 = 2C$ and $C_2 = C_3 = C$. Assume that all capacitors start without any initial charge, i.e. they are completely discharged before phase A.



The switches for phase A close first and the capacitors charge up completely. Those switches are then disconnected and the switches for phase B are closed. **What is the voltage at node u_{out} in phase B in terms of C and V_{in}?**

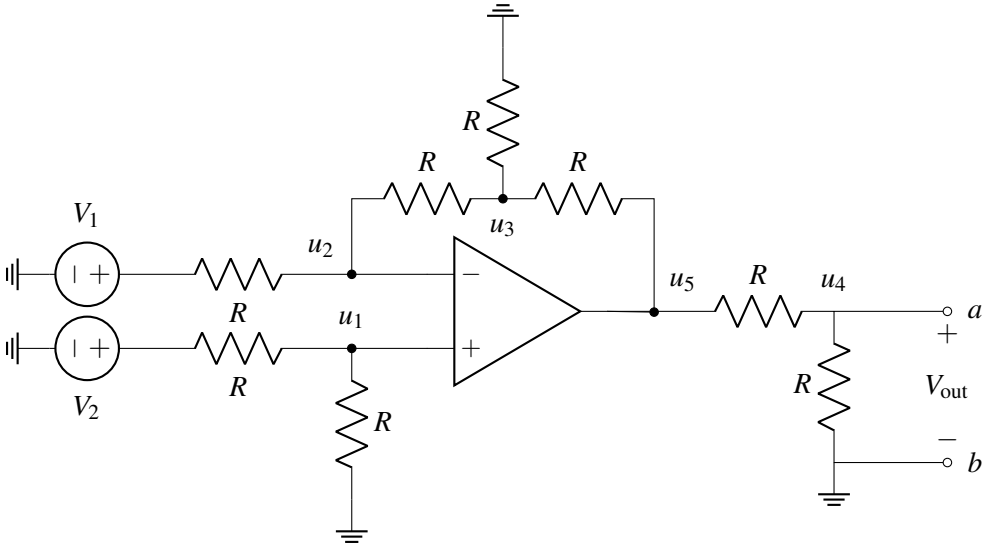
(b) Now consider the following circuit. Let us again set all of the capacitors to have the same capacitance $C_1 = 2C$ and $C_2 = C_3 = C$. Assume that all capacitors start without any initial charge, i.e. they are completely discharged before phase A. The switches for phase A close first and the capacitors charge up completely. Those switches are then disconnected and the switches for phase B are closed.



What is the voltage at u_{out} in phase B in terms of C and V_{in}?

3. Op Amp Nodal Analysis

Consider this op amp circuit below. We are interested in analyzing its input-output relationship, finding the Thévenin equivalent of this op amp circuit, and making some observations about the resulting equivalent.



(a) What is the node voltage at u_1?

(b) Write a KCL equation at node u_2 in terms of the node potentials (u_i).

(c) Write a KCL equation at node u_3 in terms of the node potentials (u_i).

(d) Write an expression for u_4 in terms of u_5 using circuit topologies you learned in class.

(e) Noting that this circuit is in negative feedback and putting together every expression we have derived in previous parts, find an expression for V_{out} as a function of V_1 and V_2.

(f) Turn off all independent sources ($V_1 = V_2 = 0V$). What is the equivalent resistance as seen between terminals a and b? This will be your Thevenin resistance, R_{Th}. (Hint: Consider what the voltage at

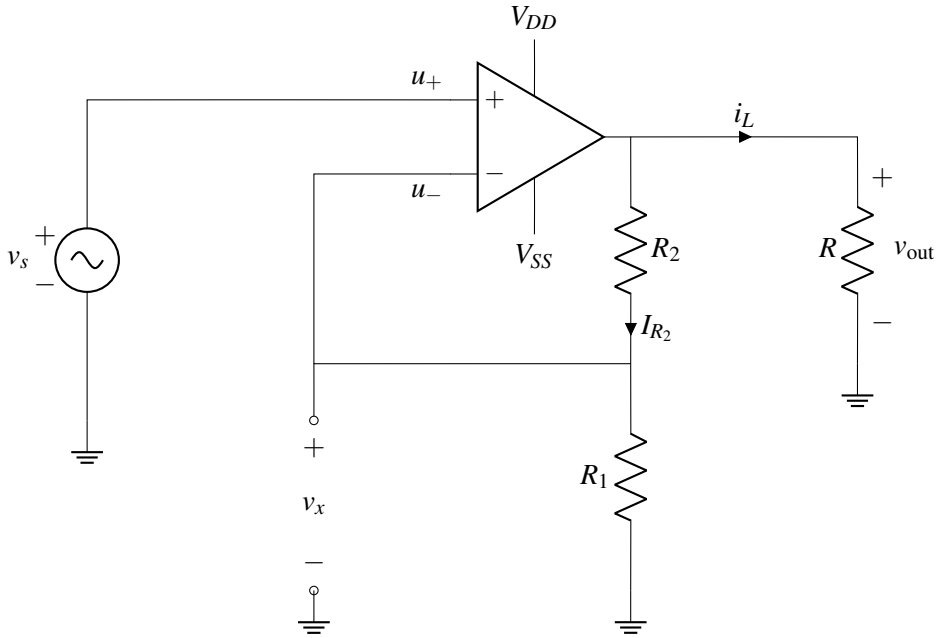
the output of the op amp becomes and use a test source, or replace the op amp with its internal model where it has a dependent source.)

(g) Use what you found in previous parts to draw the Thévenin equivalent.

(h) **Practice (Optional)**: Does the Thévenin resistance depend on all the resistors or a strict subset? What might explain this?

4. Op-Amp in Negative Feedback

In this question, we analyze op-amp circuits that have finite op-amp gain A. We replace the op-amp with its circuit model with parameterized gain and observe the gain's effect on the terminal and output voltages as the gain approaches infinity. **Note here that $V_{SS} = -V_{DD}$.**



For parts (a) - (e) only, assume that the op-amp is ideal (i.e., $A \to \infty$). We will consider the case of finite gain A in parts (f) - (h).

(a) Consider the circuit shown above and $V_{SS} = -V_{DD}$. What is $u_+ - u_-$?

(b) Find v_x as a function of v_{out}.

(c) What is I_{R_2}, i.e. the current flowing through R_2 as a function of v_s? *Hint: Find the current through R_1 first.*

(d) Find v_{out} as a function of v_s.

(e) What is the current i_L through the load resistor R? Give your answer in terms of v_{out}.

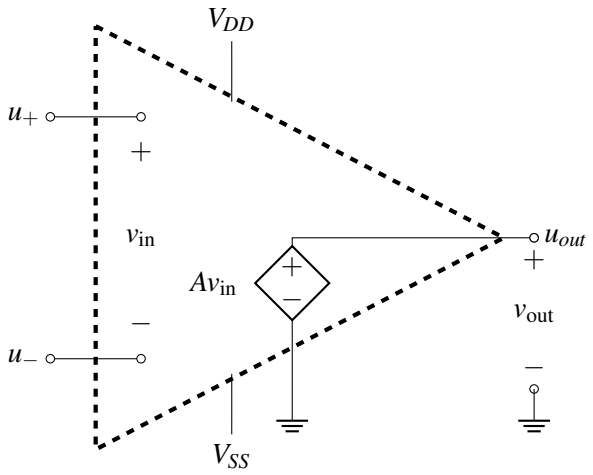


Figure 1: Op-amp model

(f) We will now examine what happens when A is not ∞. To understand what happens in this case, first draw an equivalent circuit for the first op amp circuit, **by replacing the ideal op-amp in the non-inverting amplifier with the op-amp model shown above.**

Now, using this setup, calculate v_{out} and v_x in terms of A, v_s, R_1, R_2, and R. Is the magnitude of v_x larger or smaller than the magnitude of v_s? Do these values depend on R? *Hint: Note that the first golden rule still applies, i.e. the currents through the input terminals are zero.*

(g) Using your solution to the previous part, calculate the limits of v_{out} and v_x as $A \to \infty$. You should get the same answer as in part (d) for v_{out}.

5. Transresistance Amplifier

A common use of an op-amp is to convert a current signal into a voltage signal. This configuration is called a *transresistance amplifier*, as shown in Figure 2. (Note: In the real world, we call this a trans*impedance* amplifier. Impedance is just a fancy word to describe resistance as a function of frequency.) Assume that $V_{SS} = -V_{DD}$ for all the parts of this problem.

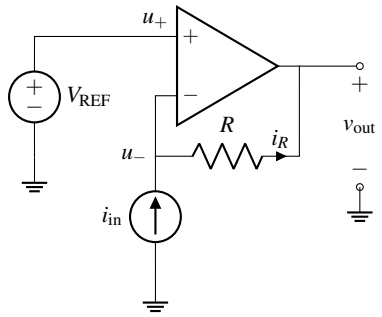


Figure 2: Transresistance amplifier

(a) What is the value of the current i_R in Figure 2? *Hint: Your answer should be in terms of i_{in}.*

(b) What is the voltage at the negative terminal of the op-amp u_- in terms of V_{REF}.

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(c) Using the results from parts (a) and (b), find an expression for v_{out} in terms of V_{REF} and i_{in}.

(d) If we set $V_{\text{REF}} = 0\,\text{V}$, calculate the gain of the overall circuit $G = \frac{v_{\text{out}}}{i_{\text{in}}}$.

6. Pre-Lab Questions

These questions pertain to the Pre-Lab reading for the Touch 3B lab. You can find the reading under the Touch 3B Lab section on the 'Schedule' page of the website.

(a) Why can't we have an ideal current source?

(b) For the integrator circuit, if $V_{in}(t)$ is a triangle wave, what kind of wave will $I_{in}(t)$ be?

(c) Does V_{out} increase or decrease when you touch the touchscreen?

7. Homework Process and Study Group

Who did you work with on this homework? List names and student ID's. (In case you met people at homework party or in office hours, you can also just describe the group.) How did you work on this homework? If you worked in your study group, explain what role each student played for the meetings this week.