EECS 16A Designing Information Devices and Systems I
Spring 2023 Homework 9

This homework is due Friday, March 24, 2023 at 23:59.
Self-grades are due Friday, April 7, 2023 at 23:59.

Submission Format
Your homework submission should consist of **one** file.

- `hw9.pdf`: A single PDF file that contains all of your answers (any handwritten answers should be scanned).

Submit the file to the appropriate assignment on Gradescope.

1. Reading Assignment

For this homework, please read Notes 16 and Sections 17.1 - 17.2 from Note 17. Note 16 will provide an introduction to capacitors (a circuit element which stores charge), capacitive equivalence, and the underlying physics behind them. Sections 17.1 - 17.2 in Note 17 will provide an overview of the capacitive touchscreen and how to measure capacitance.

(a) How do we calculate the equivalent capacitance of series and parallel capacitors? Compare this with how we calculate resistor equivalences.

(b) Consider the capacitive touchscreen. Briefly describe how it works: what quantity changes when your finger touches it? Compare and contrast it to the resistive touchscreens we have seen in previous lectures and homeworks.

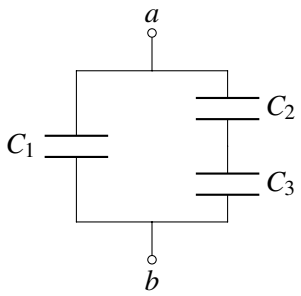
Solution:

a) Capacitors in parallel can be combined into an equivalent capacitance that is the sum of the individual capacitance (just like resistors in **series**). Capacitors C_1, C_2 in series can be combined into an equivalent capacitance of $\frac{C_1 C_2}{C_1+C_2}$ (just like resistors in **parallel**).

b) The capacitive touch screen works by detecting a change in capacitance, which is caused by the additional capacitance of a finger being added to the capacitance of the touch screen. The resistive touch screen detects the position of a touch by modeling the touch screen as a voltage divider when pressed down.

2. Equivalent Capacitance

(a) Find the equivalent capacitance between terminals a and b of the following circuit in terms of the given capacitors C_1, C_2, and C_3. Leave your answer in terms of the addition, subtraction, multiplication, and division operators **only**.



Solution:

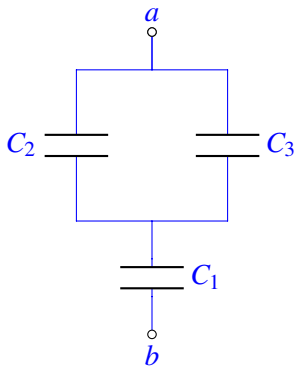
$$C_{eq} = C_1 + (C_2||C_3)$$
$$C_{eq} = C_1 + \frac{C_2 C_3}{C_2 + C_3}$$

Here, $||$ represents the mathematical parallel operator ($a||b = \frac{ab}{a+b}$).

(b) Find and draw a capacitive circuit using three capacitors, C_1, C_2, and C_3, that has equivalent capacitance of

$$\frac{C_1(C_2+C_3)}{C_1+C_2+C_3}$$

Solution: This expression is the same as $C_1||(C_2+C_3)$, so C_2 and C_3 are in parallel with each other, and C_1 is series with both of them:



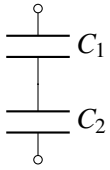
3. Modeling Weird Capacitors

For each part of this problem,

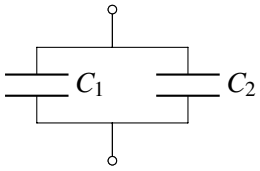
i. Pick the circuit option from below that *best* models the given physical capacitor.

ii. Calculate the total equivalent capacitance of the circuit in terms of the given quantities (e.g. $\varepsilon_1, \varepsilon_2, \varepsilon_3, L, W, D$).

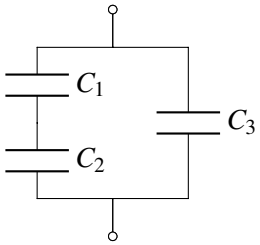
Option 1



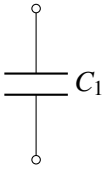
Option 2



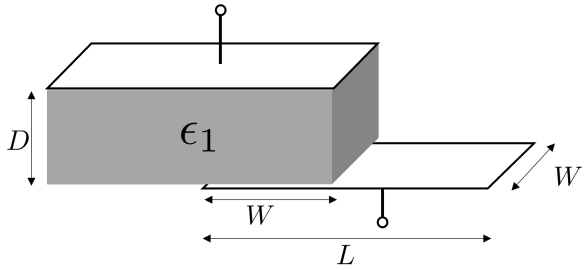
Option 3



Option 4



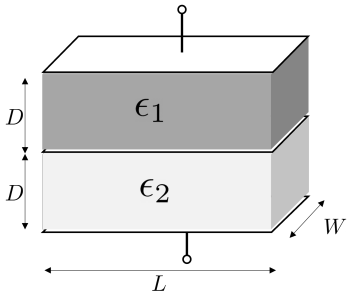
(a) A parallel plate capacitor with plate dimensions L and W, separated by a gap D, is filled with an insulator of permittivity ε_1, with the bottom plate displaced with overlap W as shown below. You can assume $W < L$ and $D << W$.
(i) Pick the circuit option from above that best models this physical capacitor, and (ii) calculate the total equivalent capacitance of the circuit in terms of L, W, D, ε_1.



Solution: Option 4, where

$$C = C_1 = \varepsilon_1 \frac{W \cdot W}{D}$$

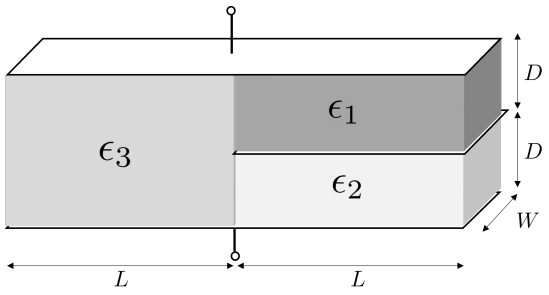
(b) A parallel plate capacitor with plate dimensions L and W, separated by a gap $2 \cdot D$, is filled with two insulators of permittivities ε_1 and ε_2 as shown below. You can assume there's a plate between the two dielectrics.
(i) Pick the circuit option from above that best models this physical capacitor, and (ii) calculate the total equivalent capacitance of the circuit in terms of $L, W, D, \varepsilon_1, \varepsilon_2$.



Solution: Option 1, where

$$C = C_1 || C_2 = \frac{L \cdot W}{D} \frac{\varepsilon_1 \varepsilon_2}{\varepsilon_1 + \varepsilon_2}$$

(c) A parallel plate capacitor with plate dimensions L and W, separated by a gap $2 \cdot D$, is filled with three different materials with permittivities ε_1, ε_2, and ε_3 as shown in the figure below. You can assume there's a plate between the two dielectrics on the right.
(i) Pick the circuit option from above that best models this physical capacitor, and (ii) calculate the total equivalent capacitance of the circuit in terms of $L, W, D, \varepsilon_1, \varepsilon_2, \varepsilon_3$.

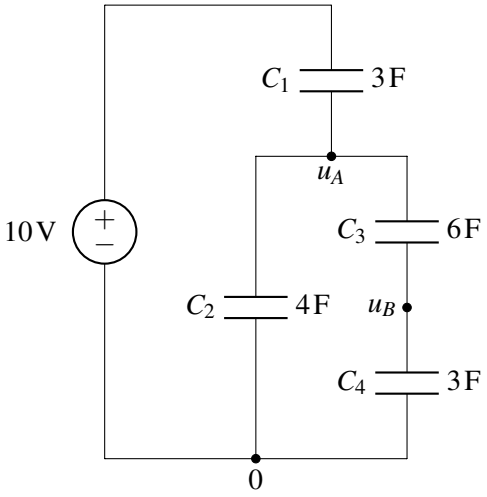


Solution: Option 3, where

$$C = (C_1||C_2) + C_3 = \frac{L \cdot W}{D}\frac{\varepsilon_1\varepsilon_2}{\varepsilon_1+\varepsilon_2} + \frac{L \cdot W\varepsilon_3}{2D} = \frac{L \cdot W}{D}\left(\frac{\varepsilon_1\varepsilon_2}{\varepsilon_1+\varepsilon_2} + \frac{\varepsilon_3}{2}\right)$$

4. Circuit with Capacitors

Find the voltages at nodes u_A and u_B, and currents flowing through all of the capacitors at steady state. Assume that before the voltage source is applied, the capacitors all initially have a charge of 0 Coulombs.



Solution: Guide: For capacitive circuits we often care about the steady state (i.e. after a long period of time when the capacitors are done charging). When analyzing the steady state for capacitive circuits powered by a voltage source, it is important to remember that once the capacitors are fully charged/discharged, no current will flow through the capacitors since there is no change in charge. In other words, we will have

$$i_1 = i_2 = i_3 = i_4 = 0\,\text{A}$$

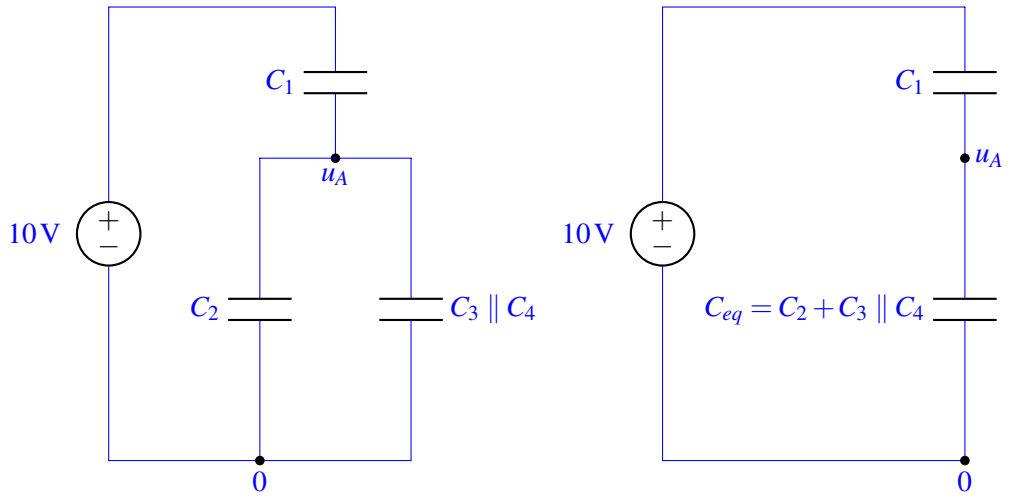
which means capacitors act as open circuits at steady state!

Thus we only need to solve for the voltages of the unknown nodes u_A, u_B in the circuit. We know that the charge stored on a capacitor and voltage difference between its terminals are related by

$$Q = CV,$$

so if we can set up equations relating the charges of the capacitors in our circuit, we should be able to solve for our unknown voltages.

Let's start by trying to find u_A. We can use our knowledge of equivalent capacitors to simplify the circuit. We see that C_3 and C_4 are in series, so we can replace it with a single capacitor with capacitance $C_3 \parallel C_4$. Now, C_2 is in parallel with the new capacitor we created, so we can combine them into a single capacitor with capacitance $C_2 + C_3 \parallel C_4$.



Note that we have collapsed the node u_B in this simplification so we will solve for that separately after first finding u_A.

Let's relate the charge between the two capacitors. Here are some helpful principles:

(a) The charge Q stored on a capacitor represents the magnitude of charge on each plate. One plate will have $+Q$ charge while the other will have $-Q$. The magnitude of charge on both plates must be exactly equal due to the physics of how capacitors work.

(b) Charge at a floating node (a node that has no connections via a resistor or wire to the rest of the circuit) is always conserved. This is because no new charges can enter this node. Importantly, if the sum of charges on the floating node is initially 0 (which occurs when all capacitors start uncharged) the sum of charges will still be 0 at steady state!

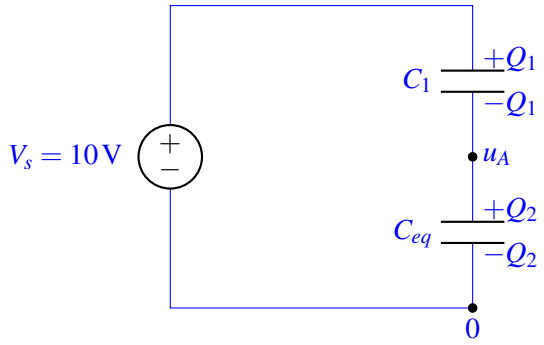
Our simplified circuit is called a capacitive divider, the capacitive analogue to a voltage divider, and so u_A should be some voltage between 0 and 10 V.

The voltage drop across C_1 will induce $+Q_1$ charge on the top plate of C_1 and $-Q_1$ on the bottom plate where

$$Q_1 = C_1(V_s - u_A) \tag{1}$$

where V_s is the voltage of the source. Similarly, the voltage drop across C_{eq} will induce $+Q_2$ charge on the top plate of C_{eq} and $-Q_2$ on the bottom plate where

$$Q_2 = C_{eq} u_A. \tag{2}$$



We note that u_A is a floating node, so we can apply principle (b) which means we must have $-Q_1 + Q_2 = 0$. In other words $Q_1 = Q_2$ so the magnitude of charge on both plates are the same! In general, this is true for all capacitors in series.

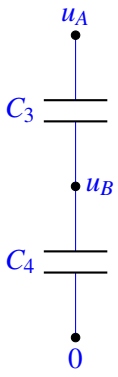
Now we can equate equations 1 and 2 and solve for u_A

$$\begin{aligned} C_1(V_s - u_A) &= C_{eq}u_A \\ C_1V_s &= C_{eq}u_A + C_1u_A \\ u_A &= V_s\frac{C_1}{C_{eq}+C_1}. \end{aligned}$$

We have found the equation for the middle node voltage of a capacitive divider. It is very similar to our voltage divider formulation except we now have C_{top} in the numerator and the sum of the capacitances on the denominator. Plugging in our given capacitance and voltage values, we have

$$\begin{aligned} C_{eq} &= C_2 + C_3 \parallel C_4 = 4\,\text{F} + \frac{6\,\text{F}\cdot 3\,\text{F}}{6\,\text{F}+3\,\text{F}} = 6\,\text{F} \\ u_A &= V_s\frac{C_1}{C_{eq}+C_1} = 10\,\text{V}\frac{3\,\text{F}}{6\,\text{F}+3\,\text{F}} = \frac{10}{3}\,\text{V}. \end{aligned}$$

Now let's solve for u_B. Observe the following sub-part of our original circuit:



We notice that again we have a capacitive divider. Using the capacitve divider equation we just derived, we can relate

$$u_B = u_A\frac{C_3}{C_4+C_3} = \frac{10}{3}\,\text{V}\frac{6\,\text{F}}{3\,\text{F}+6\,\text{F}} = \frac{20}{9}\,\text{V}.$$

Note the capacitive divider equation we have dervied can only be applied if the capacitors start uncharged!

Alternative method using charge conservation explicitly

Node u_A is a floating node because charge cannot escape or enter. Let us start by writing the equation for conservation of charge at u_A:

$$Q_{C_1} = Q_{C_2} + Q_{C_3}$$

For each capacitor, $Q = CV$ so we can equivalently write this equation for charge conservation in terms of node voltages as

$$(10\,\text{V} - u_A)3\,\text{F} = (u_A - 0)4\,\text{F} + (u_A - u_B)6\,\text{F},$$

which, after simplifying gives

$$30\,\text{V} = 13u_A - 6u_B. \tag{3}$$

Let us then write the charge conservation equation at node u_B; we have

$$Q_{C_3} = Q_{C_4}.$$

As before, we can write this charge conservation equation in terms of the node voltages as

$$(u_A - u_B)6\,\text{F} = u_B 3\,\text{F},$$

which after simplification gives

$$2u_A = 3u_B. \tag{4}$$

Equations 3 and 4 give us two linearly independent equations in two unknowns. Solving the system, we get

$$u_A = 10/3\,\text{V},$$
$$u_B = 20/9\,\text{V}.$$

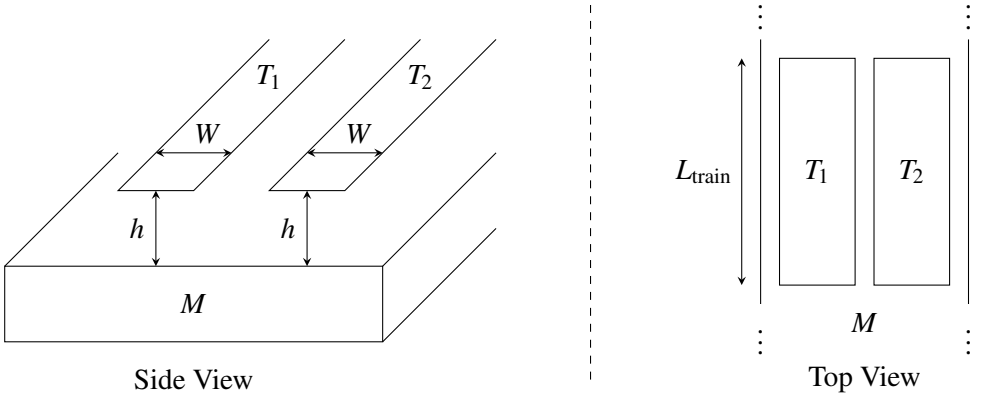
We write the currents across the capacitors again here for reader's convenience:

$$i_{C_1} = i_{C_2} = i_{C_3} = i_{C_4} = 0\,\text{A}$$

5. Maglev Train Height Control System

One of the fastest forms of land transportation are trains that actually travel slightly elevated from the ground using magnetic levitation (or "maglev" for short). Ensuring that the train stays at a relatively constant height above its "tracks" (the tracks in this case are what provide the force to levitate the train and propel it forward) is critical to both the safety and fuel efficiency of the train. In this problem, we'll explore how maglev trains use capacitors to stay elevated. (Note that real maglev trains may use completely different and much more sophisticated techniques to perform this function, so if you get a contract to build such a train, you'll probably want to do more research on the subject.)

(a) As shown below, we put two parallel strips of metal (T_1, T_2) along the bottom of the train and we have one solid piece of metal (M) on the ground below the train (perhaps as part of the track).



Assuming that the entire train is at a uniform height above the track and ignoring any fringing fields (i.e., we can use the simple equations developed in lecture to model the capacitance), as a function of L_{train} (the length of the train), W (the width of T_1 and T_2), h (the height of the train off of the track), and ε (the permittivity of the air between the train and the track) what is the capacitance between T_1 and M? What is the capacitance between T_2 and M?

Solution:

The distance between the plates (T_1 & M or T_2 & M) is h. The area of the parallel plate capacitor is $A = WL_{\text{train}}$. Using the formula for capacitance of a parallel plate capacitor, we get:

$$C = \frac{\varepsilon A}{d}$$

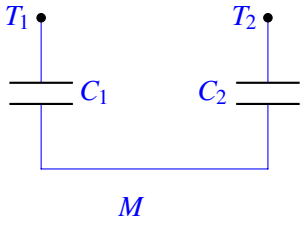
$$C_1 = \frac{\varepsilon W L_{\text{train}}}{h} \text{ (Capacitance between } T_1 \text{ and M)}$$

$$C_2 = \frac{\varepsilon W L_{\text{train}}}{h} \text{ (Capacitance between } T_2 \text{ and M)}$$

(b) Draw a circuit model showing how the capacitors between T_1 and M and between T_2 and M are connected to each other. *Hint: there should be three nodes in your circuit: T_1, T_2, and M.*

Solution:

The capacitors C_1 and C_2 are in series. To realize this, let's consider the train circuit that is in contact with T_1 and T_2. If there is current entering plate T_1, the same current has to exit plate T_2. Thus, the circuit can be modeled as follows:



(c) Using the same parameters as in part (a), provide an expression for the equivalent capacitance between T_1 and T_2.

Solution:

Since the two capacitors are in series, the equivalent capacitance between T_1 and T_2 is given by:

$$\frac{1}{C_{\text{eq}}} = \frac{1}{C_1} + \frac{1}{C_2}$$

Thus, we get

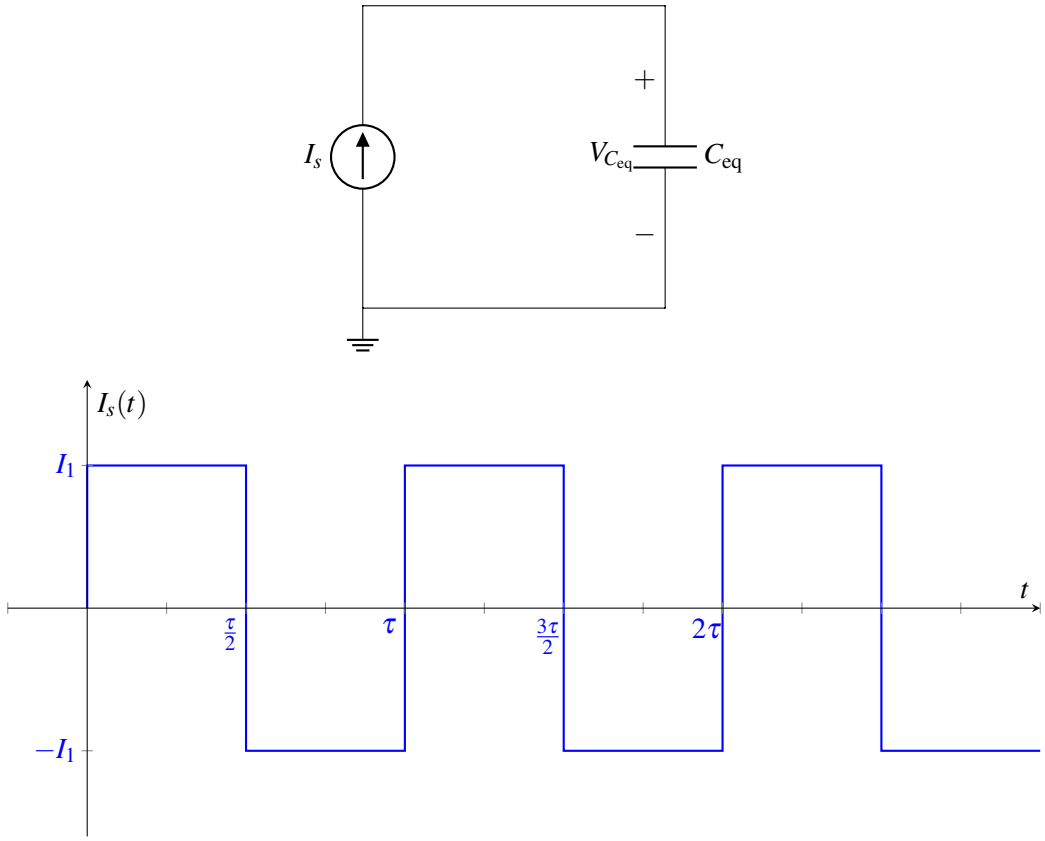
$$\frac{1}{C_{\text{eq}}} = \frac{h}{\varepsilon W L_{\text{train}}} + \frac{h}{\varepsilon W L_{\text{train}}}$$

$$C_{\text{eq}} = \frac{\varepsilon W L_{\text{train}}}{2h}$$

(d) We want to build a circuit that creates a voltage waveform with an amplitude that changes based on the height of the train. Your colleague recommends you start with the circuit as shown below, where I_s is a periodic current source, and C_{eq} is the equivalent capacitance between T_1 and T_2. The graph below shows I_s, a square wave with period τ and amplitude I_1, as a function of time.

Find an equation for and draw the voltage $V_{C_{\text{eq}}}(t)$ as a function of time. Assume the capacitor C_{eq} is discharged at time $t = 0$, so $V_{C_{\text{eq}}}(0) = 0\,\text{V}$.

Hint: Your final expression should resemble a periodic function.



Solution: We know the rate of change of voltage across a capacitor is related to the the current into the capacitor. That is:

$$I_{C_{\text{eq}}} = C_{\text{eq}} \frac{dV_{C_{\text{eq}}}}{dt}$$

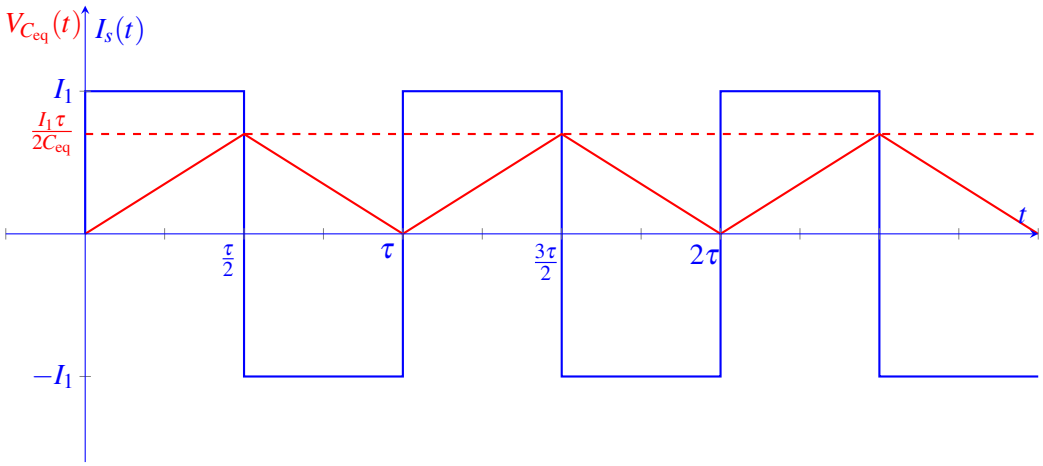
From KCL, we know $I_{C_{\text{eq}}} = I_s$. Then:

$$I_{C_{\text{eq}}} = I_s = C_{\text{eq}} \frac{dV_{C_{\text{eq}}}}{dt} \implies \frac{dV_{C_{\text{eq}}}}{dt} = \frac{I_s}{C_{\text{eq}}}$$

Since I_s is periodic, we can apply the procedure detailed in Note 17, Section 17.2.1 to get the following equation for $V_{C_{\text{eq}}}(t)$ for the first period, which repeats for subsequent periods. We recall that the capacitor is uncharged at $t = 0$ so that $V_{C_{\text{eq}}}(0) = 0\,\text{V}$.

$$V_{C_{\text{eq}}}(t) = \begin{cases} \frac{I_1}{C_{\text{eq}}} t & \text{when } 0 \leq t \leq \frac{\tau}{2} \\ \frac{-I_1}{C_{\text{eq}}}\left(t - \frac{\tau}{2}\right) + \frac{I_1 \tau}{2C_{\text{eq}}} & \text{when } \frac{\tau}{2} < t \leq \tau \end{cases}$$

Given this equation for the output voltage, $V_{C_{\text{eq}}}(t)$, as a function of the current, I_s, we can draw what the output waveform should look like.



(e) Based on your answer to the previous 2 parts, how does the voltage $V_{C_{eq}}(t)$ change with the height of the train h?

Solution: The peak height of $V_{C_{eq}}(t)$ is directly proportional to the height h because it is inversely proportional to C_{eq}, which is itself inversely proportional to h.

(f) What if we change the period of the square wave from τ to $\frac{\tau}{2}$ (and keep its amplitude I_1 the same)? How would $V_{C_{eq}}(t)$ change?

Solution: Halving the period of the square wave halves the peak height of $V_{C_{eq}}(t)$.

6. Homework Process and Study Group

Who did you work with on this homework? List names and student ID's. (In case you met people at homework party or in office hours, you can also just describe the group.) How did you work on this homework? If you worked in your study group, explain what role each student played for the meetings this week.

Solution:

I first worked by myself for 2 hours, but got stuck on problem 5. Then I met with my study group.

XYZ played the role of facilitator ... etc. We were still stuck on problem 5 so we went to office hours to talk about the problem.

Then I went to homework party for a few hours, where I finished the homework.