EECS 16A Designing Information Devices and Systems I
Summer 2023 Homework 6

This homework is due Friday, July 28th, 2023, at 23:59.
Self-grades are due Friday, August 4th, 2023, at 23:59.

Submission Format
Your homework submission should consist of **one** file.

- `hw6.pdf`: A single PDF file that contains all of your answers (any handwritten answers should be scanned).

Submit the file to the appropriate assignment on Gradescope.

Mid-Semester Survey

Please fill out the mid-semester survey: https://forms.gle/XKNPXWDidcsoM7LB9.

We highly value and appreciate your feedback!

1. Reading Assignment

For this homework, please read Note 17, 18, and 19. Note 17 introduces comparators and how we can use them to detect touch in a capacitive touchscreen. Note 18 and 19 provide an overview of op-amps, including the "golden rules" of op-amps, and various op-amp configurations. You are always encouraged to read beyond this as well.

(a) Consider the capacitive touchscreen. Briefly describe how it works: what quantity changes when your finger touches it? Compare and contrast it to the resistive touchscreens we have seen in previous lectures and homeworks.

Solution: The capacitive touch screen works by detecting a change in capacitance, which is caused by the additional capacitance of a finger being added to the capacitance of the touch screen. The resistive touch screen detects the position of a touch by modeling the touch screen as a voltage divider when pressed down.

(b) What is the purpose of a comparator? How can we use a comparator circuit to detect a touch for a capacitive touchscreen?

Solution: A comparator gives a binary output of either a logical 'high' or 'low' value depending on the difference of voltage between its two input terminals. Thus, comparators can be used as logical indicators, and in the case of a touchscreen a comparator can indicate whether or not a touch occurs. In the capacitive touchscreen, we connect an alternating current source to the equivalent capacitance, so that it can charge and discharge periodically. Then one terminal of the comparator is connected to the capacitor voltage and the other terminal is connected to a reference voltage source. The value of this reference voltage source needs to be between the peaks of the capacitor voltage with and without touch. Thus, when a touch occurs, the voltage difference between the input terminals will invert in sign, and the comparator will respond.

(c) If the op-amp supply voltages are $V_{DD} = 5\,\text{V}$ and $V_{SS} = 0\,\text{V}$, then what are the minimum and maximum value of V_{out}?

Solution: The minimum op-amp output will always be the value of the V_{SS} supply rail, and thus 0V in this case. The maximum op-amp output will always be the value of the V_{DD} supply rail, and thus 5V in this case.

(d) What does the internal gain of an op-amp, A, mean? What is its value for an ideal op-amp? What about for a non-ideal one?

Solution: The internal gain of an op-amp, A is the ratio of the output voltage to the error voltage, i.e. A is given by $\frac{v_{out}}{u_+ - u_-}$. For ideal op-amps, $A \to \infty$. For non-ideal op-amps, A is finite.

(e) What are the two "golden rules" of ideal op-amps? When do these rules hold true?

Solution: The golden rules are the following:

- The currents into the input terminals of the op-amp are zero, i.e. $I_+ = I_- = 0$. This rule is always true.
- The error signal going into the op-amp must be zero, i.e. $u_+ = u_-$. This rule only holds when there is negative feedback and the op-amp gain is large.

(f) What is the effect of "loading" and how can op-amps be used to mitigate this effect?

Solution: Loading is the effect when a load is connected to the output of a circuit. If we model the circuit output terminal as a Thevenin equivalent, we notice that the load resistance forms a voltage divider with the Thevenin resistance. As a result, the output voltage will decrease due to the loading effect. If we place an op-amp in between the circuit output and the load, we can mitigate the loading effect, since the op-amp will not draw any current on the inputs and thus there will be no voltage drop over the Thevenin resistance. Furthermore, the op-amp output is connected directly to a voltage source and thus will not change no matter what load resistance is attached.

2. Pre-Lab Questions

These questions pertain to the Pre-Lab reading for the APS lab. You can find the reading under the APS Lab section on the 'Schedule' page of the website.

(a) What two devices do we use in the APS setup as signal emitter and receiver?

Solution: In the APS system, we use speakers as signal emitters to emit sound waves (the signal) and use microphones as receivers.

(b) What is the formula for the time delay of arrival of the signal emitted from a speaker? Provide an expression in terms of the number of samples and sampling frequency (f_s)

Solution: The time delay of arrival of the signal from an emitter is given by the following formula: $\text{time} = \frac{\#samples}{f_s} = \frac{\#samples}{\frac{\#samples}{seconds}} = \text{seconds}$, where f_s is the sampling frequency of the receiver.

(c) What value of θ maximizes the dot product $\mathbf{a} \cdot \mathbf{b}$? HINT: Think of what value θ maximizes the function $\cos\theta$

Solution: $\theta = 0$, since $\cos\theta = 1$.

3. Digital to Analog Converter (DAC)

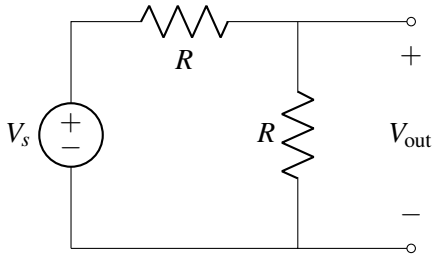
For some outputs, such as audio applications, we need to produce an analog output, or a continuous voltage from 0 to V_s. These analog voltages must be produced from digital voltages, that is sources, that can only be V_s or 0. A circuit that does this is known as a Digital to Analog Converter. It takes a binary representation of a number and turns it into an analog voltage.

The output of a DAC can be represented with the equation shown below:

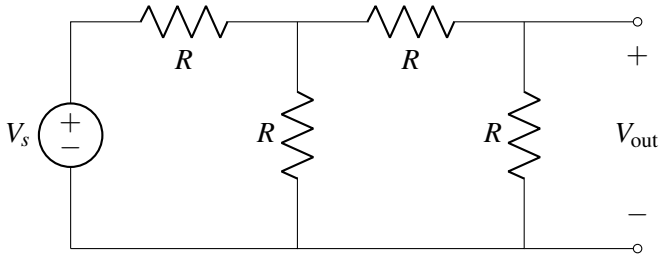
$$V_{\text{out}} = V_s \sum_{n=0}^{N} \frac{1}{2^n} \cdot b_n$$

where each binary digit b_n is multiplied by $\frac{1}{2^n}$.

(a) We know how to take an input voltage and divide it by 2:



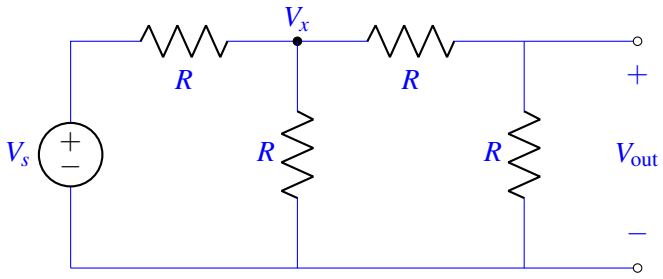
To divide by larger powers of two, we might hope to just "cascade" the above voltage divider. For example, consider:



Calculate V_{out} in the above circut. Is $V_{\text{out}} = \frac{1}{4}V_s$?

Solution:

We first find the potential V_x.



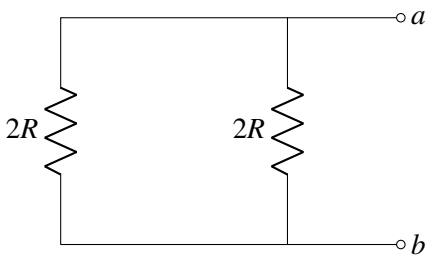
$$V_x = \frac{R \parallel 2R}{R + R \parallel 2R} V_s = \frac{\frac{2}{3}R}{R + \frac{2}{3}R} V_s = \frac{2}{5} V_s$$

$$V_{\text{out}} = \frac{R}{R+R} V_x = \frac{1}{2} \cdot \frac{2}{5} V_s = \frac{1}{5} V_s \neq \frac{1}{4} V_s$$

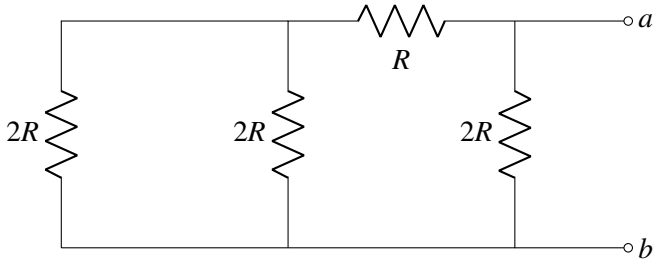
No, V_{out} does not equal $\frac{1}{4}V_s$.

(b) The R-$2R$ ladder, shown below, has a very nice property. For each of the circuits shown below, find the equivalent resistance looking in from points a and b. Do you see a pattern?

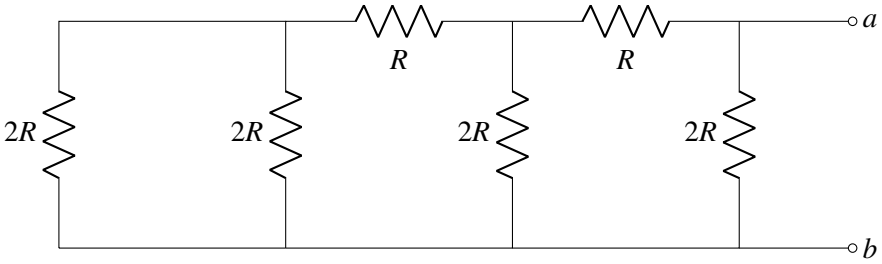
i.



ii.



iii.

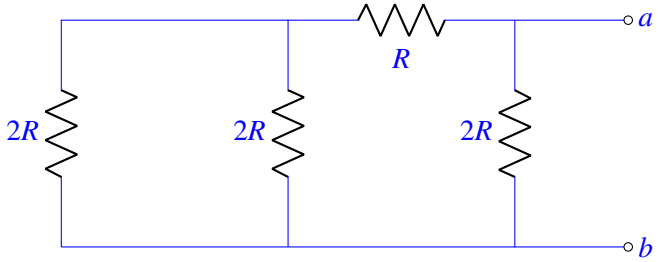


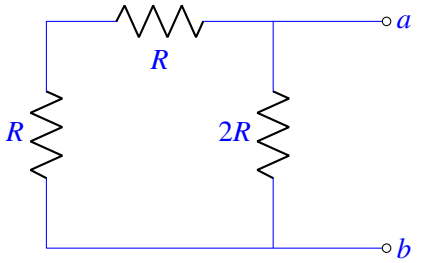
Solution:

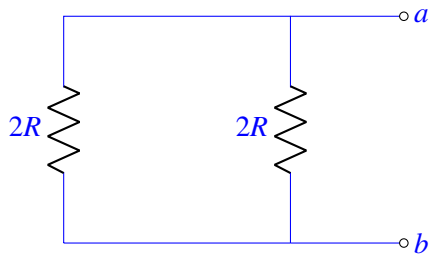
i.

$$R_{eq} = 2R \parallel 2R = R$$

ii. We find the equivalent resistance for the resistors from left to right.

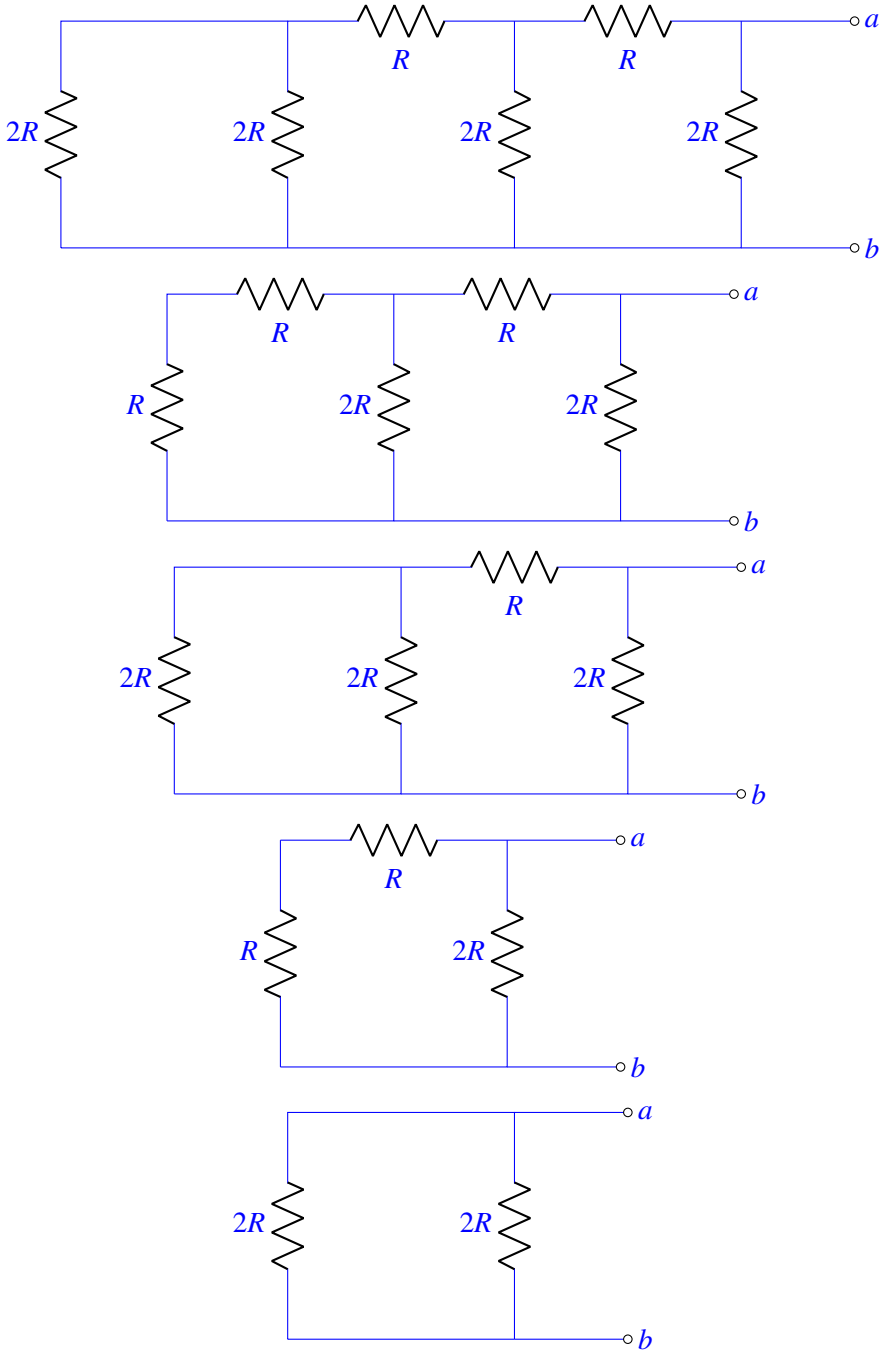






$$R_{eq} = 2R \parallel 2R = R$$

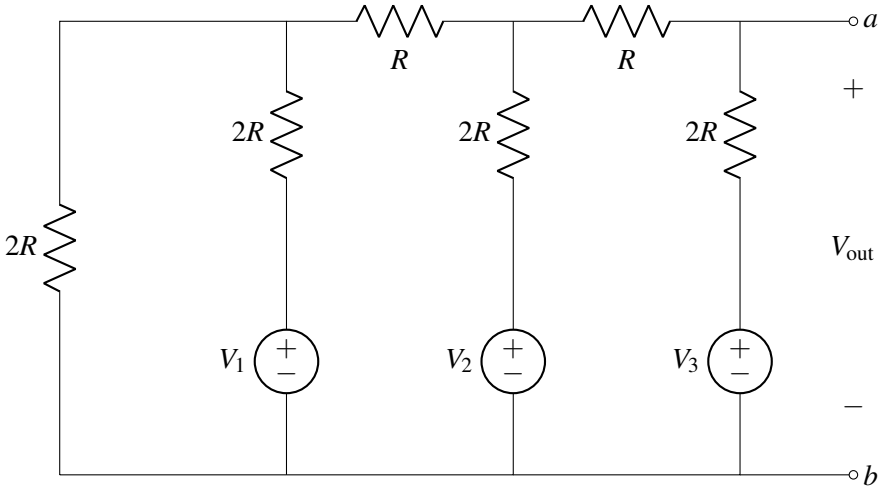
iii. Again, we find the equivalent resistance for the resistors from left to right.



$$R_{eq} = 2R \parallel 2R = R$$

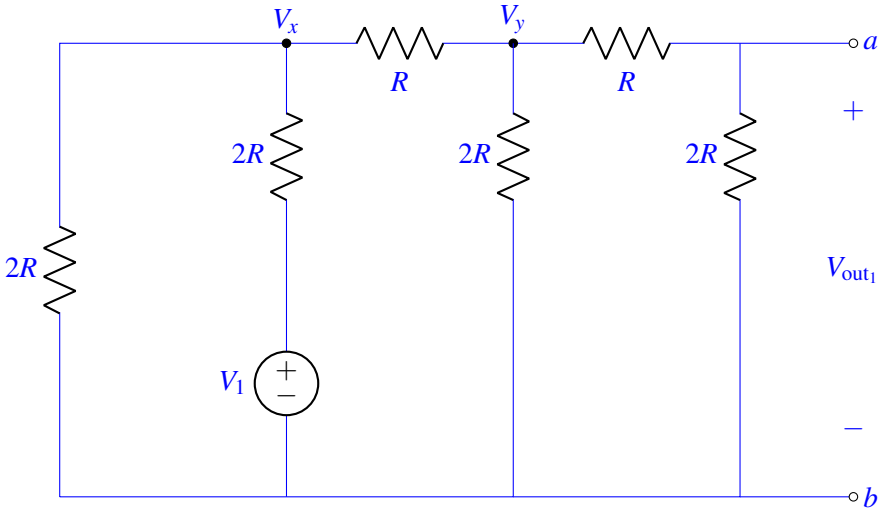
The equivalent resistance is always $R_{eq} = R$.

(c) The following circuit is an R-$2R$ DAC. To understand its functionality, use superposition to find V_{out} in terms of each V_k in the circuit.

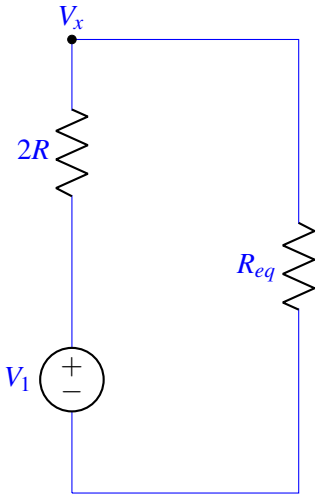


Solution:

V_1:



We first find the potential V_x. To do this, we can simplify the circuit.



$$R_{eq} = 2R \parallel (R + (2R \parallel (R + 2R))) = \frac{22}{21}R$$

We can then find V_x using the voltage divider formula.

$$V_x = \frac{\frac{22}{21}R}{2R + \frac{22}{21}R} V_1 = \frac{11}{32} V_1$$

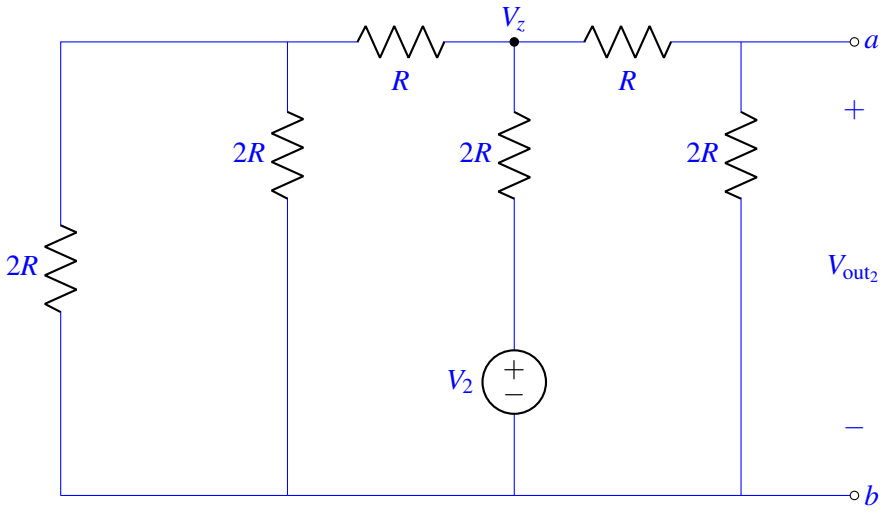
Similarly, we use the voltage divider formula to find V_y in terms of V_x.

$$V_y = \frac{2R \parallel (R+2R)}{R + 2R \parallel (R+2R)} V_x = \frac{\frac{6}{5}R}{R + \frac{6}{5}R} V_x = \frac{6}{11} \cdot \frac{11}{32} V_1 = \frac{3}{16} V_1$$

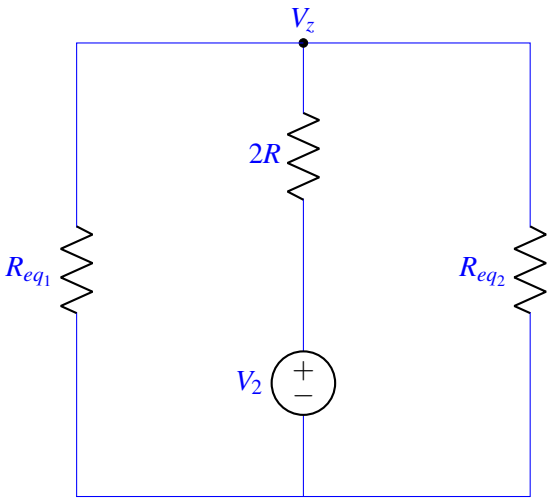
Applying the voltage divider formula again gives us V_{out_1}.

$$V_{\text{out}_1} = \frac{2R}{R+2R} V_y = \frac{2}{3} \cdot \frac{3}{16} V_1 = \frac{1}{8} V_1$$

V_2:



We first find the potential V_z. To do this, we can simplify the circuit.



$$R_{eq_1} = R + (2R \parallel 2R) = R + R = 2R$$

$$R_{eq_2} = R + 2R = 3R$$

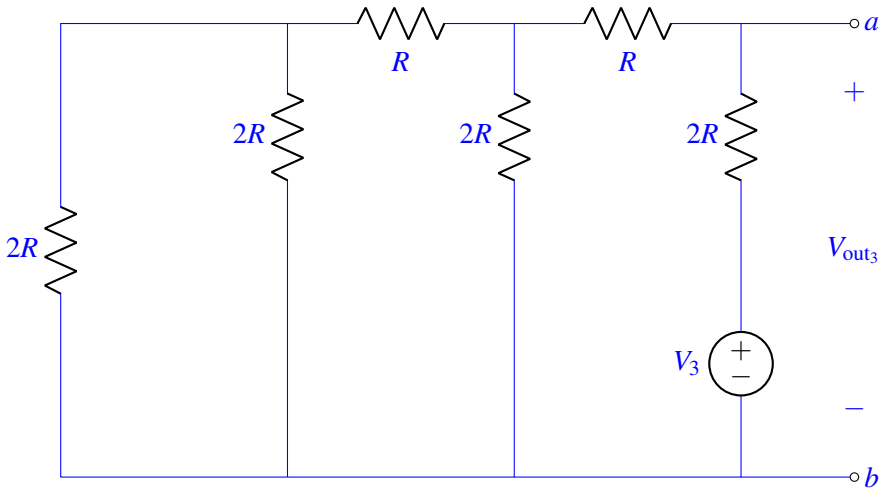
We can then find V_z using the voltage divider formula.

$$V_z = \frac{2R \parallel 3R}{2R + (2R \parallel 3R)} V_2 = \frac{\frac{6}{5}R}{2R + \frac{6}{5}R} V_2 = \frac{3}{8} V_2$$

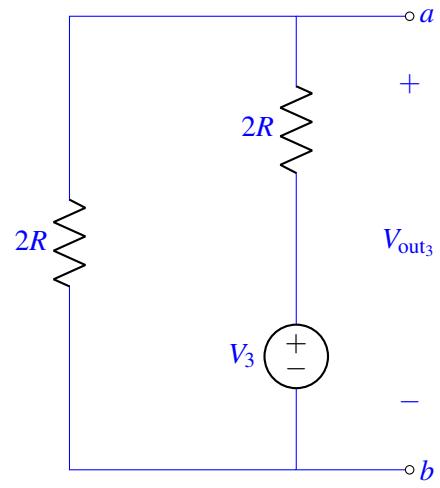
Applying the voltage divider formula again gives us V_{out_2}.

$$V_{\text{out}_2} = \frac{2R}{R + 2R} V_z = \frac{2}{3} \cdot \frac{3}{8} V_2 = \frac{1}{4} V_2$$

V_3:



We can simplify this circuit.



$$V_{out_3} = \frac{2R}{2R+2R}V_3 = \frac{1}{2}V_3$$

$$V_{out} = V_{out_1} + V_{out_2} + V_{out_3} = \frac{1}{8}V_1 + \frac{1}{4}V_2 + \frac{1}{2}V_3$$

(d) We've now designed a 3-bit R-$2R$ DAC. What is the output voltage V_{out} if $V_2 = 1\,\text{V}$ and $V_1 = V_3 = 0\,\text{V}$?

Solution:

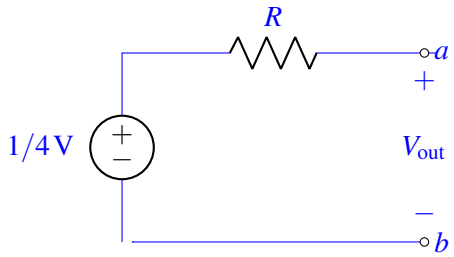
$$V_{out} = \frac{1}{8}\cdot 0\,\text{V} + \frac{1}{4}\cdot 1\,\text{V} + \frac{1}{2}\cdot 0\,\text{V} = 1/4\,\text{V}$$

(e) Draw the Thévenin equivalent of the above circuit, looking in from the terminals a and b with $V_2 = 1\,\text{V}$ and $V_1 = V_3 = 0\,\text{V}$.

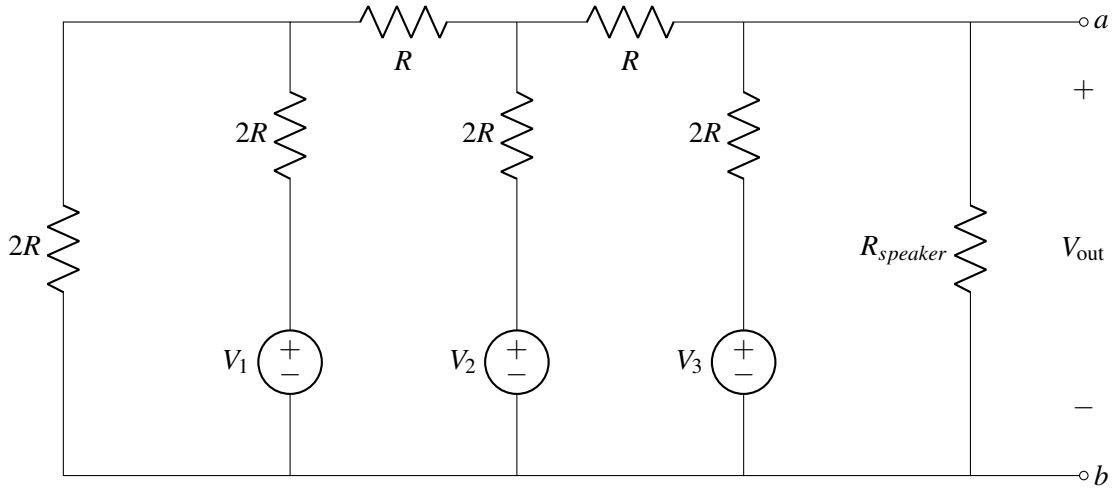
Solution:

$$V_{Th} = 1/4\,\text{V}$$

$$R_{Th} = R$$

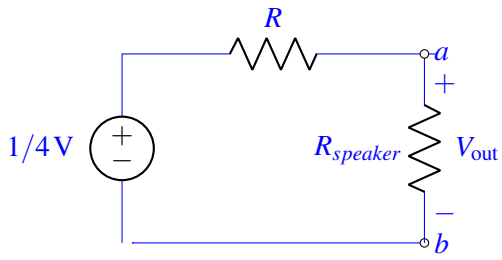


(f) Suppose that we now attach a speaker to the DAC with a resistance of $R_{speaker} = 50\Omega$ as shown in the figure below. Assume also, that the value of R is 50Ω as well. What is the voltage across the speaker and the power dissipated by the speaker? *Hint:* Use the Thevenin equivalent circuit to calculate the above.



Solution:

Attaching the speaker is equivalent to adding a load resistor to the output of the DAC as shown below:



$$V_{out} = \frac{R_{speaker}}{R + R_{speaker}} \cdot 1/4\,\text{V} = \frac{1}{2} \cdot 1/4\,\text{V} = 1/8\,\text{V}$$

$$P_{out} = \frac{{V_{out}}^2}{R_{speaker}} = 0.3125\text{mW}$$

(g) Repeat part (f) now assuming that the speaker resistance is 100Ω. The value of R remains 50Ω. How do the power and voltage values you found in the two parts compare? Why is the voltage across the speaker in both cases lower than V_{th}?

Solution:

$$V_{out} = \frac{R_{speaker}}{R + R_{speaker}} \cdot 1/4\,\text{V} = \frac{2}{3} \cdot 1/4\,\text{V} = 1/6\,\text{V}$$

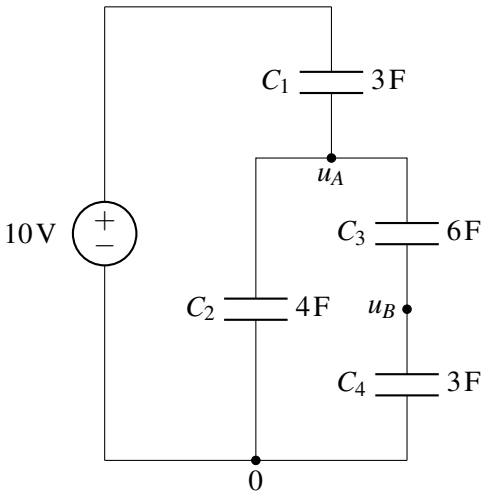
$$P_{out} = \frac{{V_{out}}^2}{R_{speaker}} \approx 0.278\text{mW}$$

Notice that even though the voltage across the speaker in this part is (as expected) larger than the voltage in the previous part the power delivered to the speaker is actually smaller! This indicates that maximum power transfer occurs when we have matching i.e. when $R_{speaker} = R_{th}$.

Finally, since the speaker has some equivalent resistance and therefore draws some current from the DAC. As a result, the voltage across the output will be lower than V_{th}.

4. Circuit with Capacitors

Find the voltages at nodes u_A and u_B, and currents flowing through all of the capacitors at steady state. Assume that before the voltage source is applied, the capacitors all initially have a charge of 0 Coulombs.



Solution: Guide: For capacitive circuits we often care about the steady state (i.e. after a long period of time when the capacitors are done charging). When analyzing the steady state for capacitive circuits powered by a voltage source, it is important to remember that once the capacitors are fully charged/discharged, no current will flow through the capacitors since there is no change in charge. In other words, we will have

$$i_1 = i_2 = i_3 = i_4 = 0\,\text{A}$$

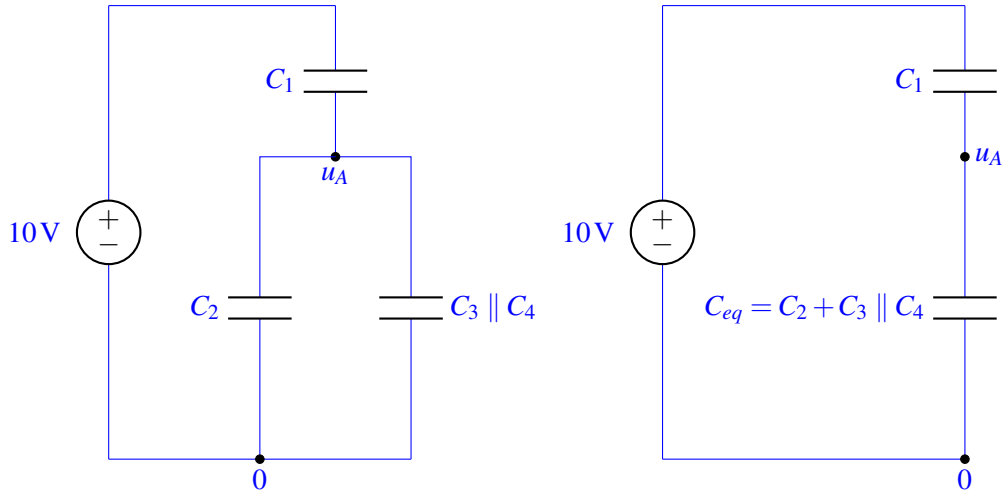
which means capacitors act as open circuits at steady state!

Thus we only need to solve for the voltages of the unknown nodes u_A, u_B in the circuit. We know that the charge stored on a capacitor and voltage difference between its terminals are related by

$$Q = CV,$$

so if we can set up equations relating the charges of the capacitors in our circuit, we should be able to solve for our unknown voltages.

Let's start by trying to find u_A. We can use our knowledge of equivalent capacitors to simplify the circuit. We see that C_3 and C_4 are in series, so we can replace it with a single capacitor with capacitance $C_3 \parallel C_4$. Now, C_2 is in parallel with the new capacitor we created, so we can combine them into a single capacitor with capacitance $C_2 + C_3 \parallel C_4$.



Note that we have collapsed the node u_B in this simplification so we will solve for that separately after first finding u_A.

Let's relate the charge between the two capacitors. Here are some helpful principles:

(a) The charge Q stored on a capacitor represents the magnitude of charge on each plate. One plate will have $+Q$ charge while the other will have $-Q$. The magnitude of charge on both plates must be exactly equal due to the physics of how capacitors work.

(b) Charge at a floating node (a node that has no connections via a resistor or wire to the rest of the circuit) is always conserved. This is because no new charges can enter this node. Importantly, if the sum of charges on the floating node is initially 0 (which occurs when all capacitors start uncharged) the sum of charges will still be 0 at steady state!

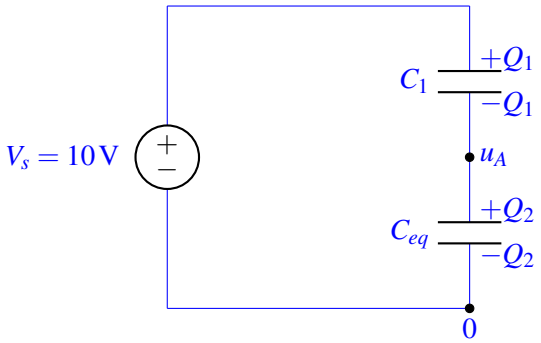
Our simplified circuit is called a capacitive divider, the capacitive analogue to a voltage divider, and so u_A should be some voltage between 0 and 10 V.

The voltage drop across C_1 will induce $+Q_1$ charge on the top plate of C_1 and $-Q_1$ on the bottom plate where

$$Q_1 = C_1(V_s - u_A) \tag{1}$$

where V_s is the voltage of the source. Similarly, the voltage drop across C_{eq} will induce $+Q_2$ charge on the top plate of C_{eq} and $-Q_2$ on the bottom plate where

$$Q_2 = C_{eq} u_A. \tag{2}$$



We note that u_A is a floating node, so we can apply principle (b) which means we must have $-Q_1 + Q_2 = 0$. In other words $Q_1 = Q_2$ so the magnitude of charge on both plates are the same! In general, this is true for all capacitors in series.

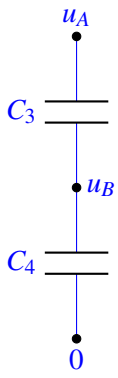
Now we can equate equations 1 and 2 and solve for u_A

$$C_1(V_s - u_A) = C_{eq}u_A$$
$$C_1V_s = C_{eq}u_A + C_1u_A$$
$$u_A = V_s\frac{C_1}{C_{eq}+C_1}.$$

We have found the equation for the middle node voltage of a capacitive divider. It is very similar to our voltage divider formulation except we now have C_{top} in the numerator and the sum of the capacitances on the denominator. Plugging in our given capacitance and voltage values, we have

$$C_{eq} = C_2 + C_3 \parallel C_4 = 4\,\text{F} + \frac{6\,\text{F}\cdot 3\,\text{F}}{6\,\text{F}+3\,\text{F}} = 6\,\text{F}$$
$$u_A = V_s\frac{C_1}{C_{eq}+C_1} = 10\,\text{V}\frac{3\,\text{F}}{6\,\text{F}+3\,\text{F}} = \frac{10}{3}\,\text{V}.$$

Now let's solve for u_B. Observe the following sub-part of our original circuit:



We notice that again we have a capacitive divider. Using the capacitve divider equation we just derived, we can relate

$$u_B = u_A\frac{C_3}{C_4+C_3} = \frac{10}{3}\,\text{V}\frac{6\,\text{F}}{3\,\text{F}+6\,\text{F}} = \frac{20}{9}\,\text{V}.$$

Note the capacitive divider equation we have dervied can only be applied if the capacitors start uncharged!

Alternative method using charge conservation explicitly

Node u_A is a floating node because charge cannot escape or enter. Let us start by writing the equation for conservation of charge at u_A:

$$Q_{C_1} = Q_{C_2} + Q_{C_3}$$

For each capacitor, $Q = CV$ so we can equivalently write this equation for charge conservation in terms of node voltages as

$$(10\,\text{V} - u_A)3\,\text{F} = (u_A - 0)4\,\text{F} + (u_A - u_B)6\,\text{F},$$

which, after simplifying gives

$$30\,\text{V} = 13u_A - 6u_B. \tag{3}$$

Let us then write the charge conservation equation at node u_B; we have

$$Q_{C_3} = Q_{C_4}.$$

As before, we can write this charge conservation equation in terms of the node voltages as

$$(u_A - u_B)6\,\text{F} = u_B 3\,\text{F},$$

which after simplification gives

$$2u_A = 3u_B. \tag{4}$$

Equations 3 and 4 give us two linearly independent equations in two unknowns. Solving the system, we get

$$u_A = 10/3\,\text{V},$$
$$u_B = 20/9\,\text{V}.$$

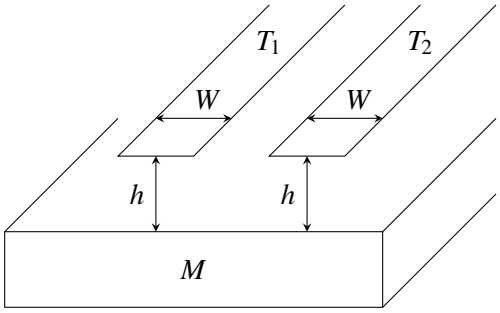
We write the currents across the capacitors again here for reader's convenience:

$$i_{C_1} = i_{C_2} = i_{C_3} = i_{C_4} = 0\,\text{A}$$

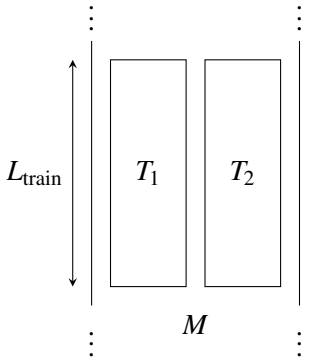
5. Maglev Train Height Control System

One of the fastest forms of land transportation are trains that actually travel slightly elevated from the ground using magnetic levitation (or "maglev" for short). Ensuring that the train stays at a relatively constant height above its "tracks" (the tracks in this case are what provide the force to levitate the train and propel it forward) is critical to both the safety and fuel efficiency of the train. In this problem, we'll explore how maglev trains use capacitors to stay elevated. (Note that real maglev trains may use completely different and much more sophisticated techniques to perform this function, so if you get a contract to build such a train, you'll probably want to do more research on the subject.)

(a) As shown below, we put two parallel strips of metal (T_1, T_2) along the bottom of the train and we have one solid piece of metal (M) on the ground below the train (perhaps as part of the track).



Side View



Top View

We assume that the entire train is at a uniform height above the track, so we can use the simple equations developed in lecture to model the capacitance.

As a function of L_{train} (the length of the train), W (the width of T_1 and T_2), and h (the height of the train above the track), determine the capacitances between T_1 and M and between T_2 and M. *Hint: Note that the area of a capacitor is given by the overlap area between its two plates.*

Solution:

The distance between the plates (T_1 & M or T_2 & M) is h. The area of the parallel plate capacitor is $A = WL_{\text{train}}$. Using the formula for capacitance of a parallel plate capacitor, we get:

$$C = \frac{\varepsilon A}{d}$$

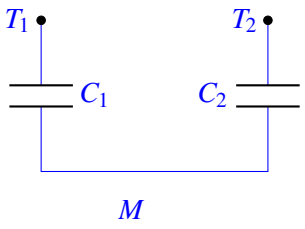
$$C_1 = \frac{\varepsilon W L_{\text{train}}}{h} \text{ (Capacitance between } T_1 \text{ and M)}$$

$$C_2 = \frac{\varepsilon W L_{\text{train}}}{h} \text{ (Capacitance between } T_2 \text{ and M)}$$

(b) Any circuit on the train can only make direct contact at T_1 and T_2. Thus, you can only measure the equivalent capacitance between T_1 and T_2. Draw a circuit model showing how the capacitors between T_1 and M and between T_2 and M are connected to each other.

Solution:

The capacitors C_1 and C_2 are in series. To realize this, let's consider the train circuit that is in contact with T_1 and T_2. If there is current entering plate T_1, the same current has to exit plate T_2. Thus, the circuit can be modeled as follows:



(c) Using the same parameters as in part (a), provide an expression for the equivalent capacitance measured between T_1 and T_2.

Solution:

Since the two capacitors are in series, the equivalent capacitance between T_1 and T_2 is given by:

$$\frac{1}{C_{\text{eq}}} = \frac{1}{C_1} + \frac{1}{C_2}$$

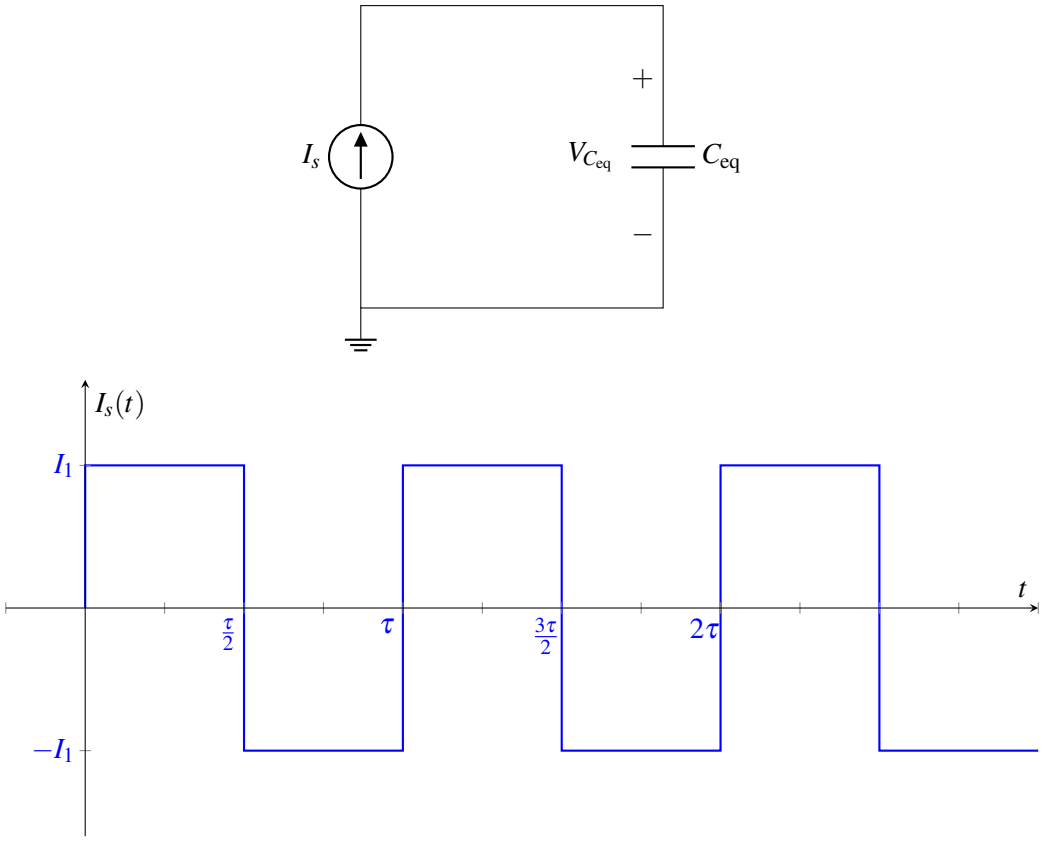
Thus, we get

$$\frac{1}{C_{\text{eq}}} = \frac{h}{\varepsilon W L_{\text{train}}} + \frac{h}{\varepsilon W L_{\text{train}}}$$

$$C_{\text{eq}} = \frac{\varepsilon W L_{\text{train}}}{2h}$$

(d) We want to build a circuit that creates a voltage waveform with an amplitude that changes based on the height of the train. Your colleague recommends you start with the circuit as shown below, where I_s is a periodic current source, and C_{eq} is the equivalent capacitance between T_1 and T_2. The graph below shows I_s, a square wave with period τ and amplitude I_1, as a function of time t.

Find an equation for and draw the voltage $V_{C_{\text{eq}}}(t)$ as a function of time t. Assume the capacitor C_{eq} is discharged at time $t = 0$, so $V_{C_{\text{eq}}}(0) = 0\,\text{V}$.



Solution: We know the rate of change of voltage across a capacitor is related to the the current into the capacitor. That is:

$$I_{C_{eq}}(t) = C_{eq}\frac{dV_{C_{eq}}}{dt}$$

From KCL, we know $I_{C_{eq}}(t) = I_s(t)$. Then:

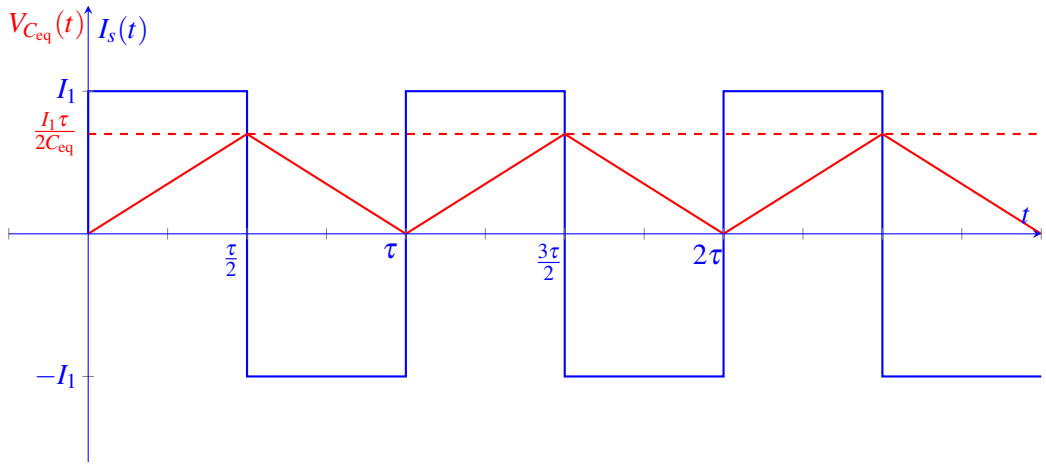
$$I_{C_{eq}}(t) = I_s(t) = C_{eq}\frac{dV_{C_{eq}}}{dt} \implies \frac{dV_{C_{eq}}}{dt} = \frac{I_s(t)}{C_{eq}}$$

Since $I_s(t)$ is periodic and piecewise-constant, we can examine what happens in the first period. We recall that the capacitor is uncharged at $t = 0$ so that $V_{C_{eq}}(0) = 0\,\text{V}$.

$$V_{C_{eq}}(t) = \begin{cases} \frac{I_1}{C_{eq}}t & \text{when } 0 \le t \le \frac{\tau}{2} \\ \frac{-I_1}{C_{eq}}\left(t - \frac{\tau}{2}\right) + \frac{I_1\tau}{2C_{eq}} & \text{when } \frac{\tau}{2} < t \le \tau \end{cases}$$

Since $V_{C_{eq}}(\tau) = V_{C_{eq}}(0) = 0$, we notice this equation for $V_{C_{eq}}(t)$ repeats in subsequent periods (i.e. $[k\tau, (k+1)\tau], k = 1, 2, \cdots$).

Given this equation for the output voltage, $V_{C_{eq}}(t)$, as a function of the current, I_s, we can draw what the output waveform should look like.



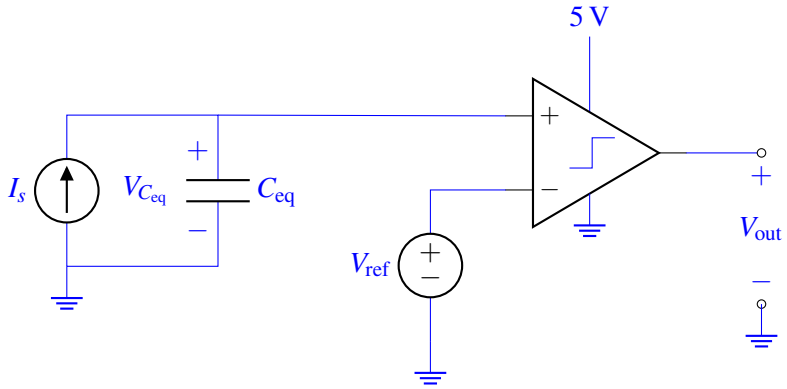
(e) We now want to develop an indicator that alerts us when the train is too high above the tracks. We want to have an output of 5 V (to trigger the alert) when the height of the train h is above 1 cm, and an output of 0 V when h is below 1 cm.

We will assume the train has length $L_{\text{train}} = 100\,\text{m}$ and that the metals, T_1 and T_2, have width $W = 1\,\text{cm}$ and permitivity $\varepsilon = 8.85\text{e}-12\,\text{F}\,\text{m}^{-1}$.

Design a circuit using **a square wave current source (i.e. I_s in part (d)) with period $\tau = 1\,\mu\text{s}$ and pulses of amplitude $I_1 = 1\,\text{mA}$, a comparator, and any number of voltage sources** to implement this function. *Hint: You should use the circuit you analyzed in part (d).*

Solution:

The circuit is shown below:



From the choice of supply voltages, we see that $V_{out} = 5\,\text{V}$ when $V_+ > V_-$.

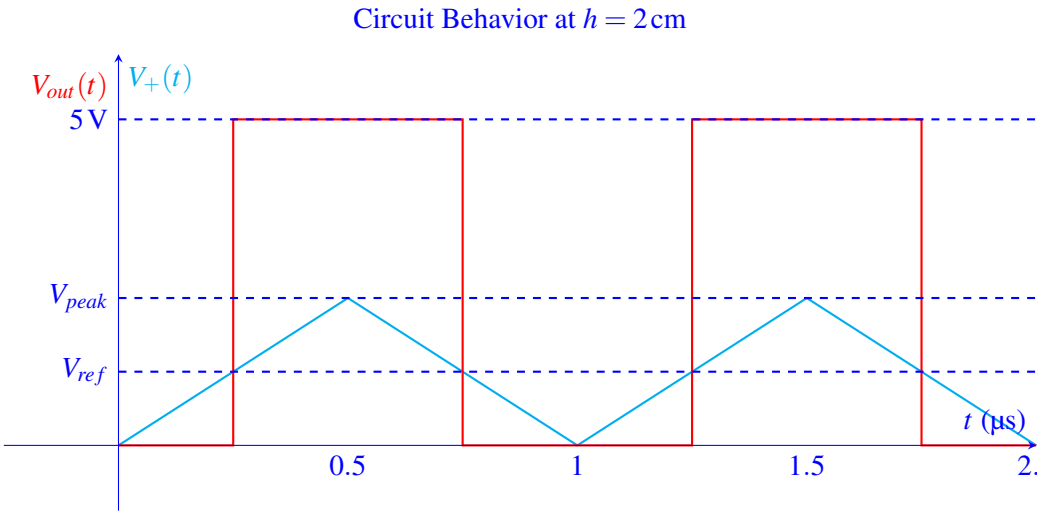
We know the amplitude of $V_{C_{eq}}(t)$ when $h = 1\,\text{cm}$ is:

$$\frac{I_1\tau}{2C_{\text{eq}}} = \frac{1\,\text{mA}\cdot 1\,\mu\text{s}}{2\cdot C_{\text{eq}}} = \frac{1\,\text{mA}\cdot 1\,\mu\text{s}}{2\cdot\frac{\varepsilon W L_{\text{train}}}{2h}} = \frac{1\,\text{mA}\cdot 1\,\mu\text{s}\cdot h}{\varepsilon W L_{\text{train}}} = \frac{1\,\text{mA}\cdot 1\,\mu\text{s}\cdot 1\,\text{cm}}{8.85\text{e}-12\,\text{F}\,\text{m}^{-1}\cdot 1\,\text{cm}\cdot 100\,\text{m}} = 1.13\,\text{V}$$

Thus we can set V_{ref} to this peak value assuming the train is 1 cm above the ground. If the train's height is larger than 1 cm, the peak voltage rises, and we continue to get pulses. If the train's height is below 1 cm, the peak value is less than 1.13 V preventing any pulses from the output of the circuit.

As an example, let's suppose the train's height is 2 cm. Then we would observe the following output for V_{out}. Note that the x-axis is in µs, that $V_{ref} = 1.13\,\text{V}$ as we found before, and that $V_{peak} = 2\cdot V_{ref} =$

2.26 V. The cyan waveform is what we measure at V_+, and the red waveform is the 5 V pulse generated at V_{out}.

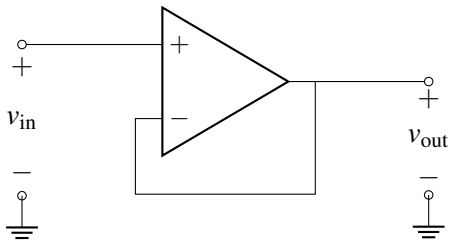


6. Testing for Negative Feedback

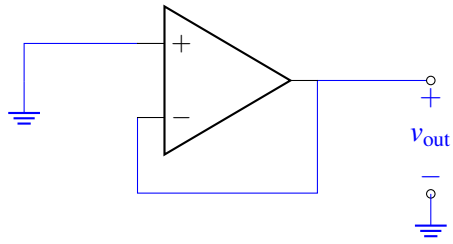
While it is tempting to say "if the feedback voltage is connected to the negative op-amp terminal, then we have negative feedback", this is not always true. Here is a two-step procedure for determining if a circuit is in negative feedback:

- **Step 1: Zero out all independent sources**, replacing voltage sources with wires and current sources with opens as we did in superposition. You do not need to zero out the voltage sources that serve as the power supplies to the op-amp, since they are not treated as signals and are not considered part of the op-amp.
- **Step 2: Wiggle the output and check the loop**. Assume that the output increases slightly. Check the direction of change of the feedback signal and the error signal from the circuit. Any change in the error signal will cause a new change in the output. This change is the feedback loop's response to the initial change.
  - If the error signal decreases, then the output must also decrease. This is the *opposite direction* we initially assumed, i.e. the loop is trying to correct for the change. So the circuit is in negative feedback.
  - If the error signal instead increased, then the output would also increase. This is the *same direction* we initially assume, i.e. the initial increase lead to further increase. We call this positive feedback.

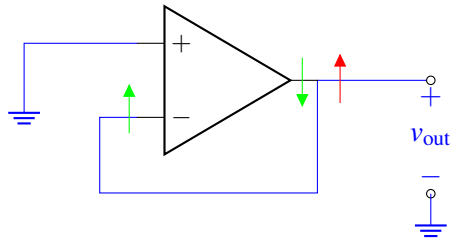
(a) Show that the voltage buffer circuit is in negative feedback. Note that here v_{in} is acting as a voltage source.



Solution: First, zero out all independent sources. For this problem, we just need to tie the input to ground.

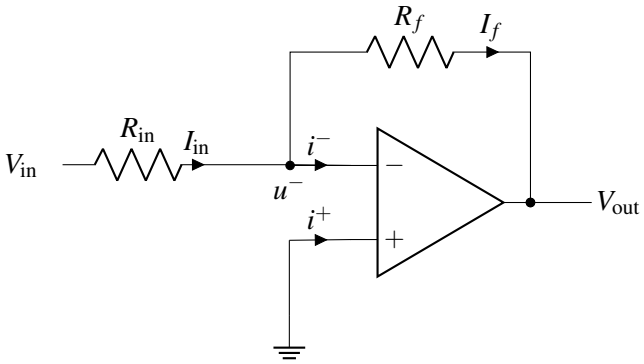


Next, wiggle the output and check the loop. Below, we label the initial change in the output in red and label subsequent changes in green:

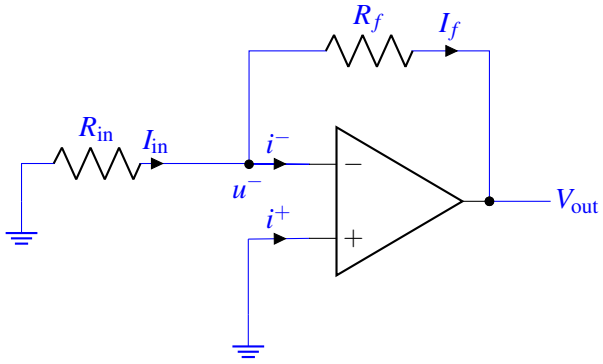


We suppose that the v_{out} increases. Output voltage v_{out} is connected to the negative terminal input u^- so u^- also increases. Our op-amp equation is $v_{out} = A \cdot (u^+ - u^-)$, so increasing u^- will cause v_{out} to decrease. This is the opposite of what initially happened, so we are in negative feedback.

(b) Show that the inverting amplifier circuit is in negative feedback.

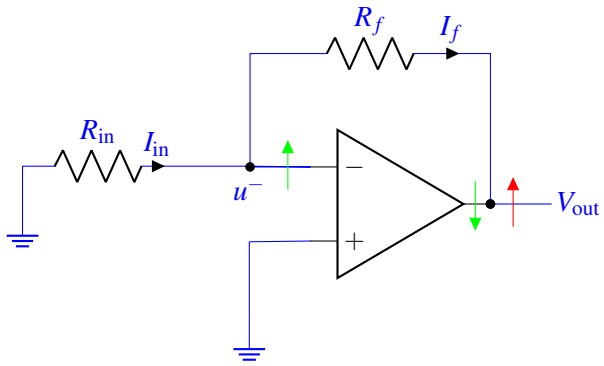


Solution: First, zero out all independent sources. For this problem, we just need to tie the input to ground.



Note that R_f and R_{in} now form a voltage divider.

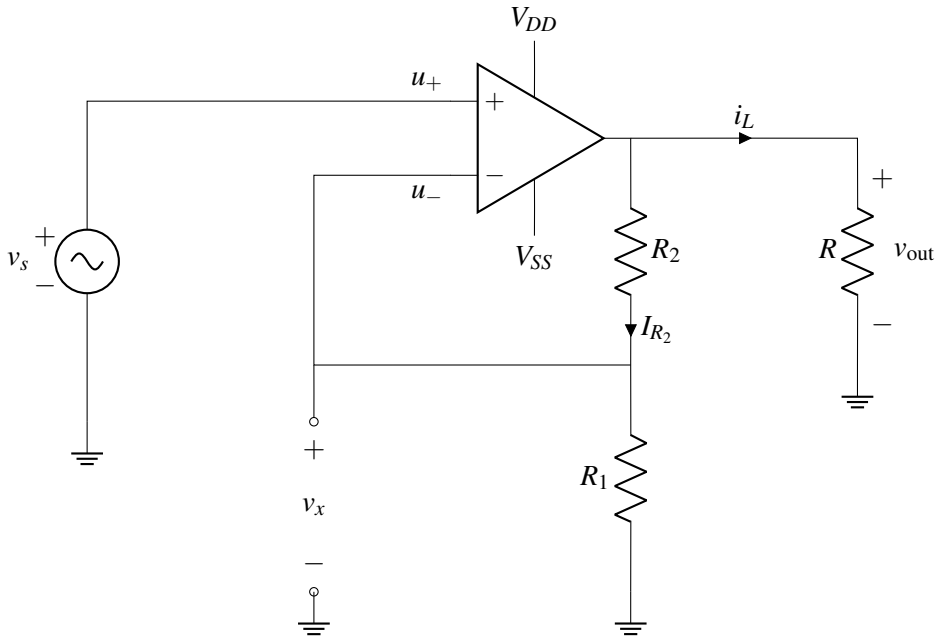
Next, wiggle the output and check the loop. Below, we label the initial change in the output in red and label subsequent changes in green:



We suppose that the v_{out} increases. Output voltage v_{out} is connected to the negative terminal input u^- so u^- also increases. Our op-amp equation is $v_{\text{out}} = A \cdot (u^+ - u^-)$, so increasing u^- will cause v_{out} to decrease. This is the opposite of what initially happened, so we are in negative feedback.

7. Op-Amp in Negative Feedback

In this question, we analyze op-amp circuits that have finite op-amp gain A. We replace the op-amp with an equivalent circuit model with parameterized gain, A, and observe the gain's effect on the terminal and output voltages as the gain approaches infinity. **Note here that $V_{SS} = -V_{DD}$.**



For parts (a) - (e) only, assume that the op-amp is ideal (i.e., $A \to \infty$). We will consider the case of finite gain A in parts (f) - (h).

(a) Consider the circuit shown above and $V_{SS} = -V_{DD}$. What is $u_+ - u_-$?

Solution: For ideal op-amp circuits in negative feedback, the voltage at the two terminals must be equal, so $u_+ - u_- = 0$.

(b) Find v_x as a function of v_{out}. *Hint: What is the current into the negative terminal u_- of the op-amp?*

Solution: Since the current into u_- is zero, the voltage v_x is the middle node of a voltage divider, so $v_x = v_{out}\frac{R_1}{R_1+R_2}$.

(c) What is I_{R_2}, i.e. the current flowing through R_2 as a function of v_s? *Hint: Find the current through R_1 first.*

Solution: The current flowing through R_2 is equal to the current flowing through R_1 since there cannot be current flowing into the op amp input. The current flowing through R_1 is $I_{R_1} = I_{R_2} = \frac{v_x}{R_1}$. We know from part (a) that $u_+ = u_-$, which means $v_x = v_s$. Finally, we can write $I_{R_2} = \frac{v_s}{R_1}$.

(d) Find v_{out} as a function of v_s.

Solution: $v_{out} = v_{R_1} + v_P R_2 = v_s + I_{R_2}R_2$. Using the expressions for I_{R_2} from part(c), $v_{out} = v_s + \frac{v_s}{R_1}R_2 = v_s\left(\frac{R_1+R_2}{R_1}\right)$. Note that v_{out} could have also been found using the voltage divider equation.

(e) What is the current i_L through the load resistor R? Give your answer in terms of v_{out}.

Solution: Using Ohm's Law, the current i_L through the load is $\frac{v_{out}}{R}$.

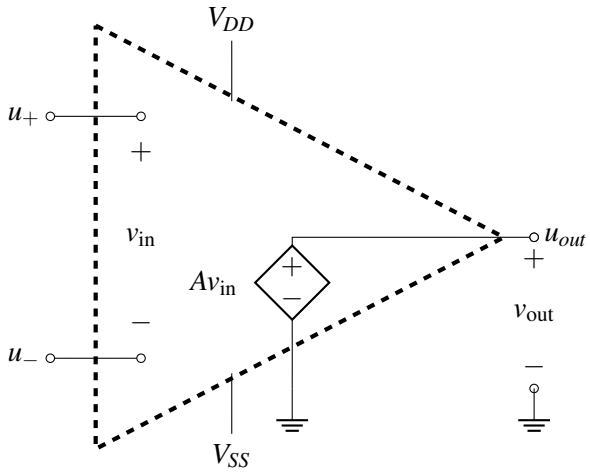


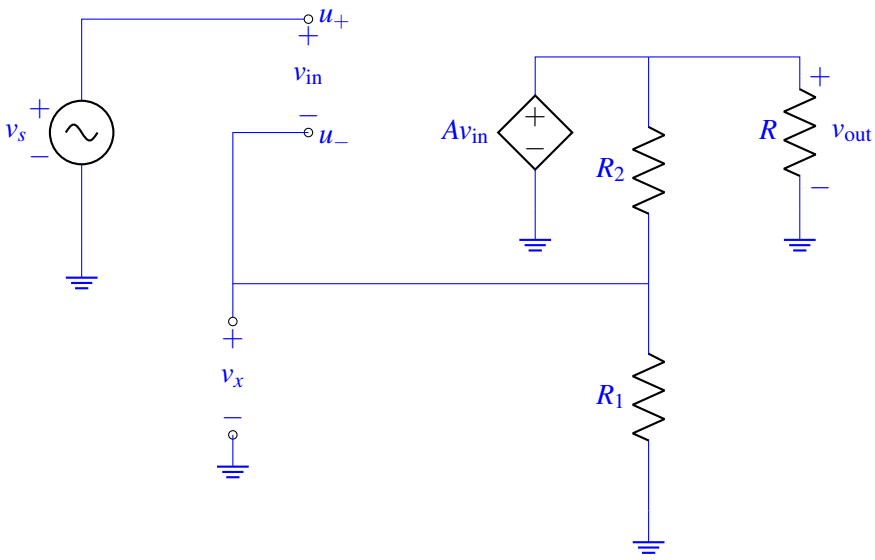
Figure 1: Op-amp model with finite gain, A

(f) We will now examine what happens when A is not ∞. To understand what happens in this case, first draw an equivalent circuit for the first op amp circuit, **by replacing the ideal op-amp in the non-inverting amplifier with the op-amp model shown above.**

Now, using this setup, calculate v_{out} and v_x in terms of A, v_s, R_1, R_2, and R. Is the magnitude of v_x larger or smaller than the magnitude of v_s? Do these values depend on R? *Hint: Note that the first golden rule still applies, i.e. the currents through the input terminals are zero.*

Solution:

This is the equivalent circuit of the op-amp:



Since v_{out} is connected to the output of the op-amp, which is a voltage source, we can determine v_{out}:

$$\begin{aligned} v_{out} &= A \cdot (u_+ - u_-) \\ &= A \cdot (v_s - v_x) \end{aligned}$$

Since there is no current flowing into the op-amp input terminals from nodes u_+ and u_-, R_1 and R_2 form a voltage divider and $v_x = v_{out}\left(\frac{R_1}{R_1+R_2}\right)$. Thus, substituting and solving for v_{out}:

$$v_{out} = A \cdot \left(v_s - v_{out}\frac{R_1}{R_1+R_2}\right)$$

$$v_{out} = v_s\left(\frac{1}{\frac{R_1}{R_1+R_2}+\frac{1}{A}}\right)$$

Knowing v_{out}, we can find v_x:

$$v_x = \frac{v_s}{1+\frac{R_1+R_2}{AR_1}}$$

Notice that v_x is slightly smaller than v_s, meaning that in equilibrium in the non-ideal case, u_+ and u_- are not equal. v_{out} and v_x do not depend on R, which means that we can treat v_{out} as a voltage source that supplies a constant voltage independent of the load R.

(g) Using your solution to the previous part, calculate the limits of v_{out} and v_x as $A \to \infty$. You should get the same answer as in part (d) for v_{out}.

Solution:

As $A \to \infty$, the fraction $\frac{1}{A} \to 0$, so

$$v_{out} = v_s\left(\frac{1}{\frac{R_1}{R_1+R_2}+\frac{1}{A}}\right)$$

converges to

$$v_s\left(\frac{1}{\frac{R_1}{R_1+R_2}+0}\right) = v_s\left(\frac{R_1+R_2}{R_1}\right).$$

Therefore, the limits as $A \to \infty$ are:

$$v_{\text{out}} \to v_s \left(\frac{R_1 + R_2}{R_1} \right)$$
$$v_x \to v_s$$

If we observe the op-amp is in negative feedback, we can apply the fact that $u_+ = u_-$. We get $v_x = v_s$. Then the current i flowing through R_1 to ground is $\frac{v_s}{R_1}$. By KCL, this same current flows through R_2 since no current flows into the negative input terminal of the op-amp (u_-). Thus, the voltage drop across R_2 is $v_{\text{out}} - v_x = i \cdot R_2 = v_s \left(\frac{R_2}{R_1} \right)$. Therefore, $v_{\text{out}} = v_s + v_s \left(\frac{R_2}{R_1} \right) = v_s \left(\frac{R_1 + R_2}{R_1} \right)$. The answers are the same if you take the limit as $A \to \infty$.

8. Transresistance Amplifier

A common use of an op-amp is to convert a current signal into a voltage signal. This configuration is called a *transresistance amplifier*, as shown in Figure 2. (Note: In the real world, we call this a trans*impedance* amplifier. Impedance is just a fancy word to describe resistance as a function of frequency.) Assume that $V_{SS} = -V_{DD}$ for all the parts of this problem.

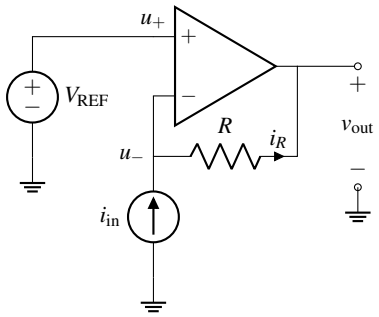


Figure 2: Transresistance amplifier

(a) What is the value of the current i_R in Figure 2? *Hint: Your answer should be in terms of i_{in}.*

Solution: By the Golden Rules, since there is no current flowing into the negative terminal of the op-amp, all the current from the current source flows through the feedback resistor. Therefore, $i_R = i_{\text{in}}$.

(b) What is the voltage at the negative terminal of the op-amp u_- in terms of V_{REF}.

Solution: Note that this op-amp is in negative feedback. Therefore, by the Golden Rules, the voltages at the negative and positive terminals of the op-amp are equal. Thus, the voltage at the negative terminal of the op-amp is V_{REF}.

(c) Using the results from parts (a) and (b), find an expression for v_{out} in terms of V_{REF} and i_{in}.

Solution: We can write a single KCL equation at the negative input terminal of the op-amp as follows:

$$i_{\text{in}} = \frac{V_{\text{REF}} - v_{\text{out}}}{R}$$
$$\implies v_{\text{out}} = V_{\text{REF}} - i_{\text{in}} R$$

(d) If we set $V_{\text{REF}} = 0\,\text{V}$, calculate the gain of the overall circuit $G = \frac{v_{\text{out}}}{i_{\text{in}}}$.

Solution: Note that in this configuration, the input signal is current i_{in} (*aside: contrast this with other op-amp circuit examples that you have seen in which the input is typically a voltage*), and the output signal is voltage v_{out}. Therefore, in this case, you will want to report the gain of this circuit as $\frac{v_{\text{out}}}{i_{\text{in}}}$.

$$\text{Gain} = \frac{v_{\text{out}}}{i_{\text{in}}} = \frac{-i_{\text{in}}R}{i_{\text{in}}} = -R$$

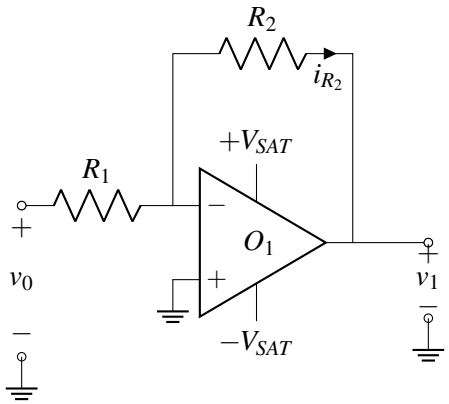
9. Integration using Op-amps

Analog circuits can be used to implement many different mathematical functions. In this problem, we will see how we can use an op-amp to create an integrator. An integrator circuit takes a time-varying voltage input $v_0(t)$ and integrates it over a time period. In other words, we want to build a circuit where the output is of the form

$$v_1(t) = K\int_0^t v_0(\tau)d\tau$$

for some constant K.

(a) Let's analyze the inverting op-amp configuration shown below. For this problem, we will assume that the op-amp is ideal and apply the op-amp golden rules.

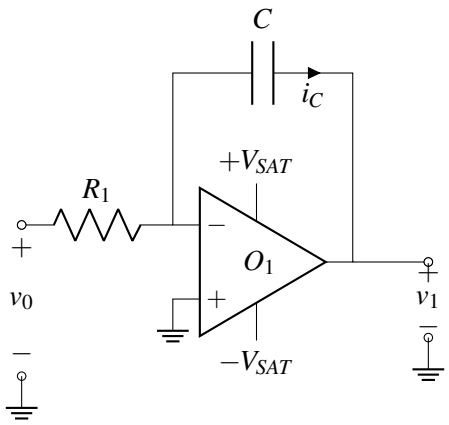


What is the current i_{R_2} flowing through resistor R_2? Write your answer in terms of v_0, R_1, and R_2.

Solution: This is the inverting amplifier we have seen before! We know that this op-amp is in negative feedback (although you may want to check again for youself for practice). Using the op-amp golden rules, we know that $u^- = u^+ = 0$. Furthermore since no current flows into the negative input of the op-amp, we must have $i_{R_1} = i_{R_2}$. We can then use Ohm's law to find

$$i_{R_2} = i_{R_1} = \frac{v_0 - 0}{R_1} = \frac{v_0}{R_1}.$$

(b) What happens if we replace the resistor in feedback R_2 with a capacitor C instead? Analyze the circuit to find the current through the capacitor i_C and express your answer in terms of v_0, R_1, and C. How does this current differ from the previous part?



Solution: In the previous part, we saw that R_2 does not affect i_{R_2}. Instead, i_{R_1} (and thus i_{R_2}) is set by the voltage drop v_0 across R_1. When we replace R_2 with C, i_{R_1} does not change so we must still have

$$i_C = i_{R_1} = \frac{v_0}{R_1}.$$

The current is the same as in part (a)!

(c) Assume that the capacitor starts uncharged at $t = 0$ and that $v_0(t)$ varies with time. Solve for the output voltage $v_1(t)$ as a function of time t. Express your answer in terms of $v_0(t)$, R_1, and C.
Hint: You may leave your answer as an integral of $v_0(t)$ as shown in the initial problem statement.

Solution: We know that $u^- = u^+ = 0$ using the second op-amp golden rule. Letting V_C be the voltage drop across the capacitor, we note that

$$V_C = u^- - v_1 = -v_1$$

since i_C points to the right and we must follow passive sign convention. In part (b), we found that

$$i_C(t) = \frac{v_0(t)}{R_1}.$$

Recall for a capacitor $Q = CV_C$. If we take the derivative with respect to time of both sides, see

$$i_C(t) = \frac{dQ}{dt} = C\frac{dV_C(t)}{dt}.$$

We can now solve this differential equation

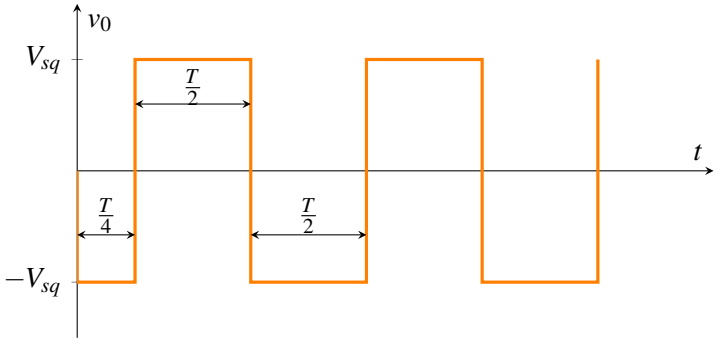
$$\begin{aligned}
C\frac{dV_C(t)}{dt} &= i_C(t) \\
\frac{dV_C(t)}{dt} &= \frac{i_C(t)}{C} \\
\frac{dV_C(t)}{dt} &= \frac{v_0(t)}{R_1 C} \\
V_C(t) - V_C(0) &= \frac{1}{R_1 C}\int_0^t v_0(\tau)d\tau \\
V_C(t) &= \frac{1}{R_1 C}\int_0^t v_0(\tau)d\tau
\end{aligned}$$

where we have used the fact that $V_C(0) = 0$ since the capacitor starts uncharged. Finally we can relate

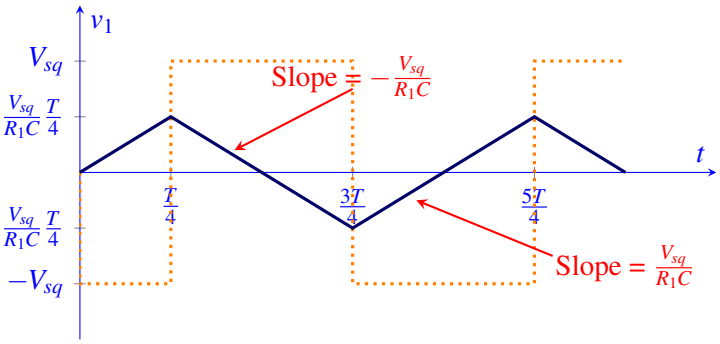
$$v_1(t) = -V_C(t) = -\frac{1}{R_1 C}\int_0^t v_0(\tau)d\tau.$$

We have shown that the output voltage of our op-amp circuit is the integral of the input voltage scaled by the constant $-\frac{1}{R_1 C}$.

(d) If v_0 varies with time as shown in the following diagram, plot v_1 for $t = 0$ to $t = 1.5T$. In your plot indicate an algebraic expression for the slope (as a function of R_1, C and V_{sq}) and add tick marks on the x and y axis indicating the time and voltage values where the ramp slope changes. You may assume again that capacitor C has 0V across it at time $t = 0$.



Solution: When $v_0(t) = -V_{sq}$ the integrator output will increase linearly with slope $\frac{V_{sq}}{R_1 C}$. When $v_0(t) = V_{sq}$ the integrator output will decrease linearly with slope $-\frac{V_{sq}}{R_1 C}$. Thus the integrator will output a triangle wave!



Previously, we saw that we can construct a triangle wave output voltage using an oscillating current source and capacitor. If we only have access to an oscillating voltage source, we can use the op-amp integrator instead!

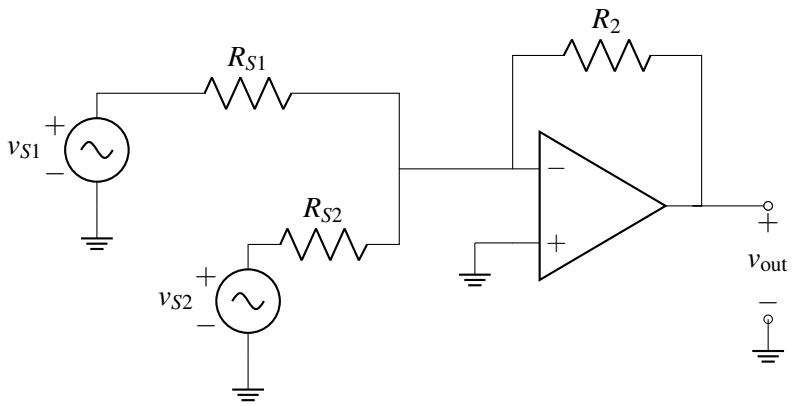
10. Cool For The Summer

You and a friend want to make a box that helps control an air conditioning unit based on both your inputs. You both have individual dials which you can use to control the voltage. An input of 0 V means that you want to leave the temperature as is. A **negative voltage input** means that you want to **reduce** the temperature. (It's hot out, so we will assume that you never want to increase the temperature – so no, we're not talking about a Berkeley summer...)

Your air conditioning unit, however, responds only to **positive voltages**. The higher the magnitude of the voltage, the stronger it runs. At zero, it is off. You also need a system that **sums up** both you and your friend's control inputs.

Therefore, you need a box that acts as an **an inverting summer** – *it outputs a weighted sum of two voltages where the weights are both negative*. The sum is weighted because one room is bigger, so you need to compensate for this.

(a) You suggest the circuit below, essentially an inverting amplifier with two inputs. Find v_{out} in terms of v_{S1}, v_{S2}, R_{S1}, R_{S2} and R_2.
Hint: You can solve this problem using either superposition or our tried-and-true KCL analysis.



Solution:

Method 1: Superposition

First, when considering v_{S1}, we zero out v_{S2}, and therefore we can disregard R_{S2}. The reason why we can disregard R_{S2} is because by the Golden Rules, we know that the voltage at the $-$ terminal of the op-amp must be equal to the voltage at the $+$ terminal. Therefore, both terminals of R_{S2} are at 0 V, and no current flows through R_{S2}. With this insight, we recognize that this is just an inverting amplifier! We apply the inverting amplifier gain equation:

$$v_{\text{out}} = -\frac{R_2}{R_{S1}} v_{S1}.$$

Similarly, when v_{S2} is on and v_{S1} is zeroed out, we disregard R_{S1} by the same argument and again have an inverting amplifier. In this case,

$$v_{\text{out}} = -\frac{R_2}{R_{S2}} v_{S2}.$$

Combining the two v_{out} equations from superposition, we get

$$v_{\text{out}} = -R_2 \left(\frac{v_{S1}}{R_{S1}} + \frac{v_{S2}}{R_{S2}} \right).$$

Method 2: KCL without superposition

According to the Golden Rules, $u_- = u_+ = 0\text{V}$, so we can write a single KCL equation at the u_- node and solve:

$$\frac{v_{S1}}{R_{S1}} + \frac{v_{S2}}{R_{S2}} + \frac{v_{\text{out}}}{R_2} = 0$$
$$v_{\text{out}} = -v_{S1} \left(\frac{R_2}{R_{S1}} \right) - v_{S2} \left(\frac{R_2}{R_{S2}} \right)$$

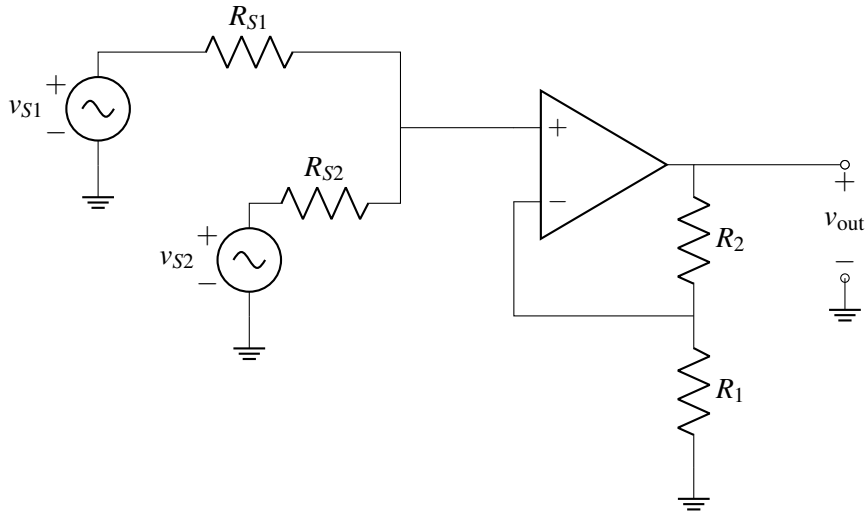
(b) Let's suppose that you want $v_{\text{out}} = -\left(\frac{1}{4}v_{S1} + 2v_{S2}\right)$ where again v_{S1} and v_{S2} represent the input voltages from you and your friend's control knobs. Select resistor values such that the circuit from part (b) implements this desired relationship.

Solution: Using the configuration from the previous part, the conditions which need to be satisfied are:

- $\frac{R_2}{R_{S1}} = \frac{1}{4}$
- $\frac{R_2}{R_{S2}} = 2$

One possible set of values is $R_2 = 2\,\text{k}\Omega$, $R_{S1} = 8\,\text{k}\Omega$, and $R_{S2} = 1\,\text{k}\Omega$, but any combination of resistors which satisfies $R_{S1} = 4R_2 = 8R_{S2}$ are valid solutions.

(c) Your friend has a different circuit idea. He proposes the following circuit below.



Find v_{out} in terms of v_{S1}, v_{S2}, R_{S1}, R_{S2}, R_1, and R_2. Can we also use this circuit to control our AC system? Why or why not?

Hint: How does this circuit relate to the one in question 2?

Solution:

We notice that the op-amp circuit is just the non-inverting amplifier we studied in question 2! If we can find the voltage at the positive op-amp input v_+ in terms of v_{S1} and v_{S2}, then we can use equation we derived:

$$v_{\text{out}} = \frac{R_1 + R_2}{R_1} v_+. \tag{5}$$

Lets again use superposition to find v_+. Turning off v_{S2} gives us a voltage divider where v_+ is the middle node. Thus

$$v_+ = v_{S1} \frac{R_{S2}}{R_{S1} + R_{S2}}.$$

If we turn off v_{S2}, we also get a voltage divider but this time

$$v_+ = v_{S2} \frac{R_{S1}}{R_{S1} + R_{S2}}.$$

We can use superposition which gives

$$v_+ = v_{S1} \frac{R_{S2}}{R_{S1} + R_{S2}} + v_{S2} \frac{R_{S1}}{R_{S1} + R_{S2}}.$$

Now substituting v_+ into equation gives us

$$v_{\text{out}} = v_{S1}\frac{R_1+R_2}{R_1}\frac{R_{S2}}{R_{S1}+R_{S2}} + v_{S2}\frac{R_1+R_2}{R_1}\frac{R_{S1}}{R_{S1}+R_{S2}}.$$

Although this circuit also implements a weighted summer, we see that this one does not invert the output. Namely, the coefficients of v_{S1}, v_{S2} are always positive. In our case we need to convert negative input voltages into a positive output voltage which this circuit cannot do.

11. Homework Process and Study Group

Who did you work with on this homework? List names and student ID's. (In case you met people at homework party or in office hours, you can also just describe the group.) How did you work on this homework? If you worked in your study group, explain what role each student played for the meetings this week.

Solution:

I first worked by myself for 2 hours, but got stuck on problem 5. Then I met with my study group.

XYZ played the role of facilitator ... etc. We were still stuck on problem 5 so we went to office hours to talk about the problem.

Then I went to homework party for a few hours, where I finished the homework.